A Chopper Current-Feedback Instrumentation Amplifier With a 1 mHz $1/f$ Noise Corner and an AC-Coupled Ripple Reduction Loop

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***Abstract*—This paper presents a chopper instrumentation amplifier for interfacing precision thermistor bridges. For high CMRR and DC gain, the amplifier employs a three-stage current-feedback topology with nested-Miller compensation. By chopping both the input and intermediate stages of the amplifier, a 1 mHz $1/f$ noise corner was achieved at an input-referred noise power spectral density (PSD) of 15 nV/$\sqrt{}$Hz. To reduce chopper ripple, the amplifier employs a continuous-time AC-coupled ripple reduction loop. Due to its continuous-time nature, the loop causes no noise folding to DC and hence offers improved noise performance over auto-zeroed amplifiers. The loop reduces chopper ripple by more than 60 dB, to levels below the amplifier's own input-referred noise. Furthermore, a maximum input referred offset of 5 μV and a CMRR greater than 120 dB were measured at a supply current of 230 μA at 5 V.**

***Index Terms*—Chopping, continuous-time, current-feedback, noise efficiency factor (NEF), noise folding, offset, $1/f$ noise, ripple reduction, thermistor.**

I. Introduction

As the critical dimensions of CMOS technology continue to decrease, the requirements on the positioning accuracy of wafer steppers increases. In such machines, thermal expansion is an important source of error, and so control loops are used to stabilize the temperature, and hence, the dimensions of critical mechanical components. Such loops require high resolution (< 1 μK) temperature measurements, which are typically made with thermistor bridges. The absolute accuracy of such measurements is then established by periodic system-level calibrations. To maintain accuracy during the minute-long intervals between calibrations, the thermistors, as well as the instrumentation amplifiers used to read them out, should be characterized by low LF noise, with $1/f$ noise corners in the order of only a few mHz.

More than two decades ago, amplifiers made in bipolar technology achieved low noise (3 nV/$\sqrt{}$Hz) and $1/f$ noise corners around 3 Hz [1]. By using dynamic offset cancellation techniques such as chopping and auto-zeroing, similar performance can be achieved in CMOS technology, despite the fact that MOS transistors exhibit more $1/f$ noise than bipolar transistors. Using these techniques, CMOS amplifiers with $1/f$ noise corners of a few Hz [2], [3] and even a few tens of mHz [4] have been reported. To the authors' knowledge, however, no CMOS amplifiers with $1/f$ noise corners in the order of a few mHz have been reported.

Although $1/f$ noise can be reduced by chopping and auto-zeroing, chopping is preferred over auto-zeroing. This is because auto-zeroing involves sampling, which folds wideband noise back to DC, while chopping employs modulation and thus achieves superior low-frequency noise performance [5]. However, this is at the cost of significant ripple at the amplifier output, due to the up-modulated offset and $1/f$ noise. Since the residual offset is proportional to the chopping frequency, this frequency tends to be rather low, typically in the order of a few tens of kHz. To suppress the resulting chopper ripple, filters with kHz cut-off frequencies are required. Such filters require significant chip area, and so off-chip filters are often used [6]. In many applications, however, this is undesirable and so a variety of on-chip techniques have been devised.

One on-chip technique for reducing chopper ripple involves the use of auto-zeroing to reduce the amplifier's initial offset [7], [8]. However, the increased low-frequency (LF) noise caused by noise folding requires extra power dissipation to meet a given noise specification. This is a serious drawback in precision temperature measurement systems, in which self-heating should be minimized. During auto-zeroing, the noise folding problem can be mitigated by reducing the amplifier's bandwidth to a fraction of the auto-zeroing frequency [9]. However, for quasi-continuous-time operation, a ping-pong topology consisting of two auto-zeroed input stages must be used, which doubles the amplifier's power consumption.

Alternatively, a sample-and-hold filter [10]–[12] can be used to reduce the chopper ripple. However, this still involves sampling, and so still incurs a certain noise folding penalty. More importantly, the extra delay introduced by the sample-and-hold filter complicates the design of the amplifier's frequency compensation network.

This paper describes a chopper current-feedback instrumentation amplifier (CFIA) with a continuous-time (CT) ripple reduction loop (RRL). The loop synchronously demodulates the amplifier's output ripple, and then drives it to zero by canceling the offset of the input stage. Due to the CT nature of the loop, this

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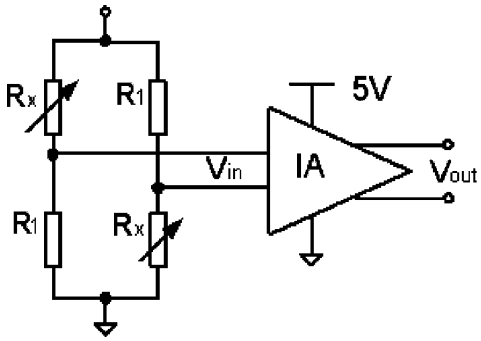

Fig. 1. Readout circuit for a thermistor bridge.

TABLE I
KEY REQUIREMENTS OF AN INSTRUMENTATION AMPLIFIER FOR BRIDGE READOUT

Specifications	Value
Supply Voltage	5V
Gain	45dB
Bandwidth	0-3 Hz
Gain tolerance	0.5%
Input referred noise	15 nV/√Hz
1/*f* corner frequency	< 3 mHz
Offset	5μV
CMRR	>120 dB
Input Common-Mode	0-3 V
Output Common-Mode	2.5 V
Supply current	<250 μA

approach does not suffer from noise folding. By using a three stage nested-Miller topology [13], and chopping the input and intermediate stages, the amplifier achieves a $1/f$ noise corner of 1 mHz at a noise density of 15 nV/$\sqrt{}$Hz.

The paper is organized as follows. In Section II, the application requirements of precision thermistor read-out are given. This is followed, in Section III by a discussion of the proposed amplifier topology. The concept and analysis of the continuous-time ripple reduction loop is described in Section IV. Section V discusses the details of the circuit implementation. The experimental results are presented in Section VI. Section VII concludes the paper.

II. THERMISTOR READ-OUT REQUIREMENTS

In wafer steppers, a temperature control loop is required to stabilize the dimensions of critical mechanical components. The mechanical stability requirements on such components translate into allowable temperature drifts in the order of 100 μK per minute. To measure such slow drifts with sufficient resolution for this application, the temperature sensor's noise should be less than 1 μK (3σ) from 21.1°C to 22.9°C, i.e., a 1.8°C range, when measured in a bandwidth ranging from 3 mHz to 50 mHz.

Since the goal is to prevent short-term temperature drift, the accuracy of the temperature measurement system may be much less than its 1 μK resolution. Overall accuracy is maintained by implementing a system-level calibration every few minutes. Therefore, gain and offset errors are not critical, as long as they are sufficiently stable during the intervals between calibrations.

Compared with other temperature sensors such as transistors and thermocouples, negative temperature coefficient (NTC) thermistors are well suited for high-resolution temperature measurements because they can achieve high sensitivity, low thermal noise, low $1/f$ noise corners (in the mHz range for high quality parts) [14] and good long-term stability (about 1 mK/year) [15]. A dual thermistor bridge (for double the sensitivity) consisting of two thermistors and two metal foil resistors is shown in Fig. 1. In our case, the thermistor's resistance (R_x in Fig. 1) is 11.4 kΩ at 22 °C, as is the resistance of the metal foil resistors (R_1 in Fig. 1). Therefore, the bridge output is zero at a temperature of 22°C. Due to the tolerance of its components, the bridge has a gain error of $\pm 0.5\%$. When biased at a bandgap voltage of 1.22 V, the bridge's common-mode voltage is 0.6 V and its sensitivity is 27 mV/°C. Thus, over the required 1.8 °C range, the bridge's output range is $\pm$24.3 mV.

Being only at the millivolt level, the output of the thermistor bridge should be amplified before it is digitized or processed further. This requires the use of a low-noise instrumentation amplifier (Fig. 1). The design challenges associated with the design of this amplifier are discussed below.

The first challenge is the required resolution: 1 μK in a 1.8 °C range and in a bandwidth ranging from 3 mHz to 50 mHz. Together with the sensitivity of the bridge, this translates into an input-referred noise density requirement of 31 nV/$\sqrt{}$Hz for the whole system. The noise of the thermistor bridge itself is about 14 nV/$\sqrt{}$Hz, and so the amplifier's white noise density was chosen to be at roughly the same level, i.e., 15 nV/$\sqrt{}$Hz. To achieve high power efficiency, the amplifier's noise should be white in the bandwidth of interest, which means that the amplifier's $1/f$ noise corner frequency must be below 3 mHz. To justify such low noise specifications, the amplifier must also have high CMRR and PSRR.

A second challenge involves self-heating, because the amplifier and the thermistor bridge will be located in the vacuum environment of a wafer stepper, where heat sinking is a significant problem. The application requirements limit the amplifier's maximum power consumption to a few milliwatts.

A third challenge is the need for the amplifier to accommodate different input and output common-mode voltages. The former is at 0.6 V, while the latter is at 2.5 V, since the amplifier's output is to be digitized by an analog-to-digital converter (ADC) with a 0 to 5 V input range. To optimally map the output range of the thermistor bridge, i.e., 2 × 24.3 mV, to the 0 to 5 V range of the ADC, the amplifier should have a rail-to-rail output with a gain of 183. The amplifier's target specifications are summarized in Table I.

III. ARCHITECTURE OF THE PROPOSED AMPLIFIER

A. Choice of Amplifier Topology

There are two basic ways to implement an instrumentation amplifier: with voltage feedback via resistors or with current feedback via transconductors.

A traditional instrumentation amplifier using resistive voltage feedback is shown in Fig. 2. The main disadvantage of this topology is that in order to shift the output common-mode voltage relative to the input common-mode voltage, a resistor R_3 is required between the common-mode node and ground. A DC current then flows through the feedback resistors, which, depending on their quality and tolerance, creates some excess

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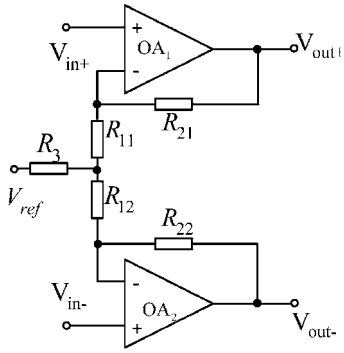

Fig. 2. Bridge instrumentation amplifier realized by two operational amplifiers.

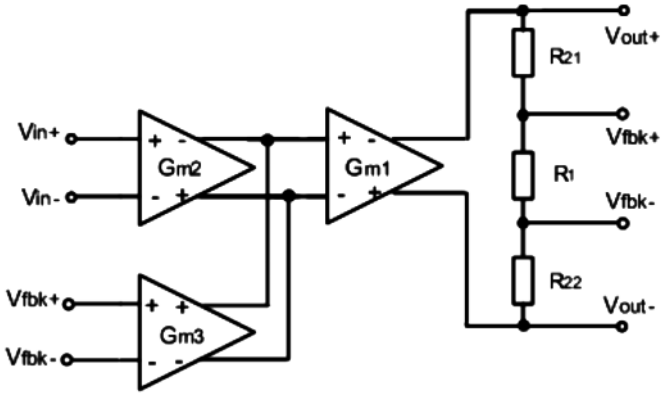

Fig. 3. Current-feedback instrumentation amplifier (CFIA).

$1/f$ noise. Secondly, to obtain high CMRR the feedback resistors need to be well matched. Thirdly, this topology is not very power efficient, as it requires the use of two high-gain low-noise operational amplifiers. However, it exhibits excellent linearity over a wide input and output range.

A current-feedback instrumentation amplifier (CFIA) [16] is shown in Fig. 3. Here, the input transconductor G_{m2} and feedback transconductor G_{m3} convert the input and feedback voltages into corresponding currents. Their difference is then nulled by the gain of G_{m1}. The overall feedback ensures that the output currents of G_{m2} and G_{m3} cancel and thus the amplifier's gain is given by

$$\mathrm{Gain} = \frac{G_{\mathrm{m2}}}{G_{\mathrm{m3}}} \frac{R_1 + R_{21} + R_{22}}{R_1}. \tag{1}$$

For bridge readout, a CFIA is more suitable than a traditional instrumentation amplifier because the CFIA uses both current-source isolation and nulling techniques to achieve a high CMRR [13]. Secondly, it can easily handle independent input and output common-mode voltages. Thirdly, it is more power efficient because the input stages share the current-summing and output stages. Although the linear range of a CFIA is often limited by the transconductors, this is not a problem in a bridge readout application.

From (1), it can be seen that the amplifier's gain accuracy will depend on the open-loop gain of G_{m1} and on the matching between the input and feedback gm-stages G_{m2} and G_{m3}. Since the gain error of the thermistor bridge is about 0.5%, the amplifier's gain accuracy does not need to be much better. For an

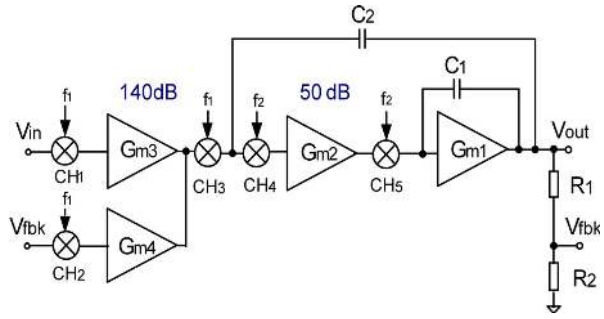

Fig. 4. Three-stage CFIA with chopped input and intermediate stages.

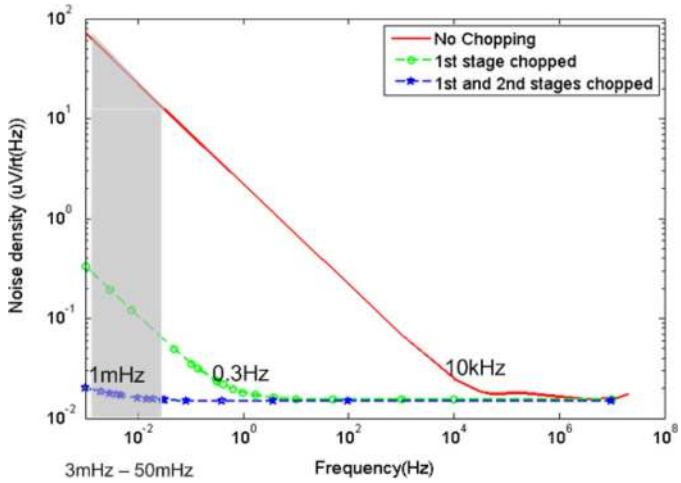

Fig. 5. Simulated input-referred noise spectrum with and without chopping.

accuracy of 0.5% at the intended closed-loop gain of 183, the open-loop gain of G_{m1} must be in excess of 90 dB, which is easily achievable with two stages of amplification. By restricting the input and output common-mode voltages to the 0–3 V range, the transconductors can be realized by pMOS differential pairs. So it should be possible to realize a CFIA that achieves better than 0.5% gain accuracy.

B. Chopping Strategy

The overall topology of the three-stage CFIA is depicted in Fig. 4. G_{m1} is a class-AB output stage to efficiently drive a 50 pF load capacitance. The large signals present in the class-AB stage mean that it is not easily chopped. However, its input-referred $1/f$ noise will be suppressed by the gain of the preceding stages. Simulations show that the preceding (chopped) stages must then have a DC gain of at least 190 dB in order to sufficiently suppress the class-AB stage's $1/f$ noise. Such a high gain can only be obtained with two stages. Thus, a three-stage topology was chosen, in which the $1/f$ noise of the input and intermediate stages is suppressed by chopping. The amplifier's simulated input-referred noise spectrum without chopping, with the input stage chopped and with the input and intermediate stages chopped, is shown in Fig. 5. Without chopping, the $1/f$ noise below 10 kHz is clearly visible. With only the input stage chopped, a $1/f$ noise corner of 0.3 Hz was observed, which is still too high. When both the input and intermediate stages are chopped, the resulting noise spectrum

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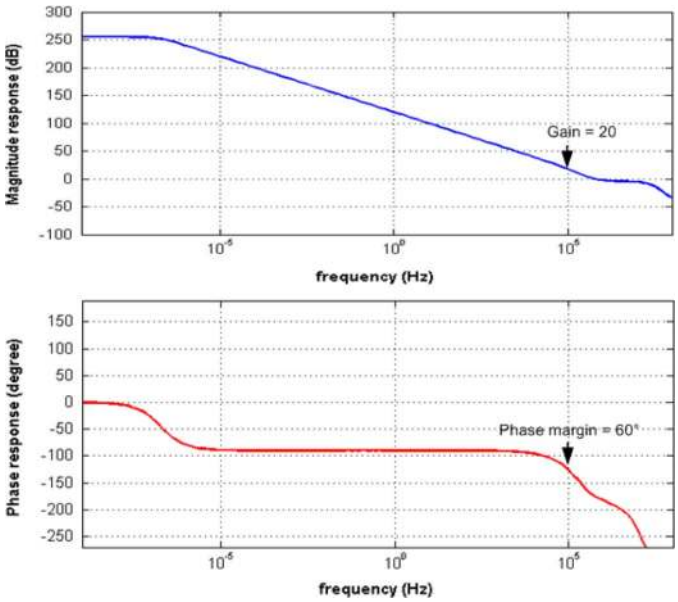

Fig. 6. Simulated open-loop frequency response.

has a $1/f$ noise corner of 1 mHz. The simulations were made with the periodic steady-state (PSS) and periodic noise analysis (PNOISE) tools of Spectre RF [17].

C. Optimum Power Efficiency

To minimize an amplifier's power consumption for a given noise specification, most of the power should be dissipated in the input stage. In this design, the input stage consumes 70% of the power. It also provides high DC gain (140 dB), which helps to suppress the noise and nonlinearity from succeeding stages. The amplifier's nested Miller frequency-compensation network [18] is designed to be stable for closed-loop gains >20, since unity-gain stability is not required in this application. The amplifier's simulated open-loop frequency response is shown in Fig. 6.

IV. Continuous-Time Ripple Reduction Loop

A. Basic Concept

Since chopping shifts the offset and the low frequency noise up to the chopping frequency, it gives rise to output ripple. As shown in Fig. 7, the chopped offset of the input stage is filtered by the main Miller compensation capacitor C_2 and appears as a triangular waveform at the output. The peak-to-peak amplitude of the ripple can then be approximated as

$$V_{\text{out,ripple}} = \frac{V_{\text{os}} \cdot G_{\text{m3}}}{2C_2 \cdot f_{\text{ch1}}}. \tag{2}$$

From (2), ripple amplitude can be reduced by reducing input-stage offset V_{os} with careful layout, by increasing the chopping frequency f_{ch1} or by increasing the size of the Miller compensation capacitor. For a worst-case 20 mV offset, with $G_{\text{m3}} = 250\,\mu$A/V, $C_2 = 80$ pF, and $f_{\text{ch1}} = 40$ kHz, $V_{\text{out,ripple}} = 0.8$ V. This is quite large compared to the amplifier's 5 V output range and thus must be suppressed. In order to do this without incurring the noise folding due to discrete-time sampling, a continuous-time (CT) ripple reduction loop (RRL) is proposed.

As shown in Fig. 7, the RRL consists of sense capacitor C_4, chopper CH_6, integrator G_{m6} with C_{int} and compensation transconductance G_{m5}. The sense capacitor C_4 converts the amplifier's output ripple $V_{\text{out,ripple}}$ into an AC current I_{AC}, whose amplitude is proportional to the derivative of $V_{\text{out,ripple}}$. This current is demodulated by chopper CH_6, and the resulting DC current I_{DC} is integrated by G_{m6} and C_{int} to generate a DC compensation voltage V_{o} that is proportional to the ripple amplitude. This is then fed back via transconductance G_{m5} to the outputs of G_{m3} and G_{m4}, thus injecting a current that compensates for the offset of G_{m3} and G_{m4}. In this manner, the amplifier's offset and hence the amplitude of the chopper ripple is reduced by the loop-gain of the RRL.

The synchronous demodulator formed by the chopper CH_6 and the integrator behaves like a narrowband filter around the chopping frequency. As a result, the RRL has little effect at frequencies near DC, and so little effect on the amplifier's low-frequency response. At frequencies close to the chopping frequency, however, the AC current coupled via C_4 into the synchronous demodulator will be demodulated to DC and feedback to the outputs of G_{m3} and G_{m4}. The result is a notch in the amplifier's forward gain at frequencies around the chopping frequency. The width of the notch is determined by the unity-gain bandwidth of the loop gain in the RRL.

B. Transfer Function Analysis of the RRL

The transfer function of the RRL can be derived with the help of the block diagram shown in Fig. 8. In the forward path between nodes C and D (components enclosed by the dashed lines in Fig. 8), an input current I_C is chopped by CH_3, integrated by C_2, differentiated by C_4, and then chopped by CH_6 again.

For simplicity, the nodes D and E are initially considered to be ideal virtual grounds. The relation between the current I_E flowing into integrator C_2 and the current I_B flowing into CH_6, is then given by

$$K = \frac{I_B}{I_E} = \frac{sC_4}{sC_2} = \frac{C_4}{C_2}. \tag{3}$$

Since this gain factor is not frequency dependent, the operations of the two choppers CH_3 and CH_6 around the integrator C_2 and the differentiator C_4 cancel each other. Hence, the relation between I_{SC4} and I_C is also K:

$$K = \frac{I_{\text{SC4}}}{I_C} = \frac{C_4}{C_2}. \tag{4}$$

It should be noted that if nodes D and E are not ideal virtual grounds, there will be a small error in the value of K expressed by (4), which will be neglected.

Let $H(s) = V_0/I_{\text{SC4}}$ be the transfer function of the integrator built around G_{m6} and C_{int} (Fig. 8). If G_{m6} has a finite DC voltage gain of A_{06}, node D is no longer an ideal virtual ground, and then

$$V_0 = -A_{06}V_{\text{i}}. \tag{5}$$

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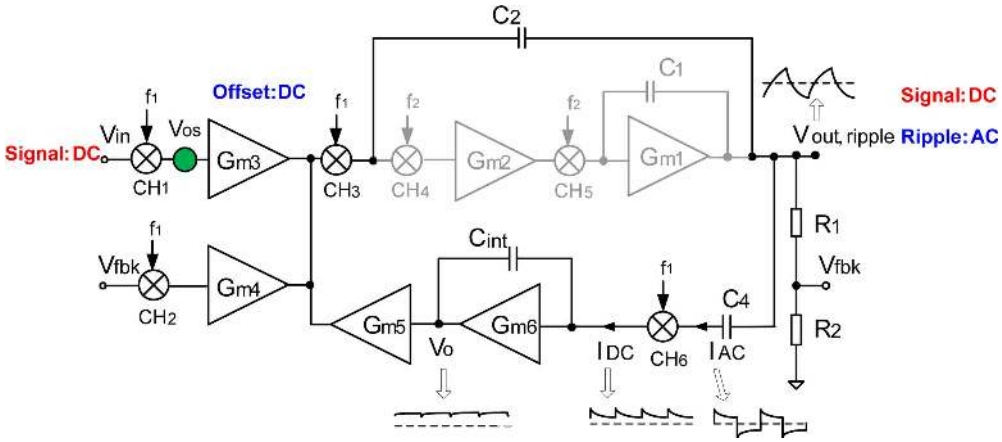

Fig. 7. Simplified block diagram of a three-stage CFIA with an AC-coupled ripple reduction loop (RRL).

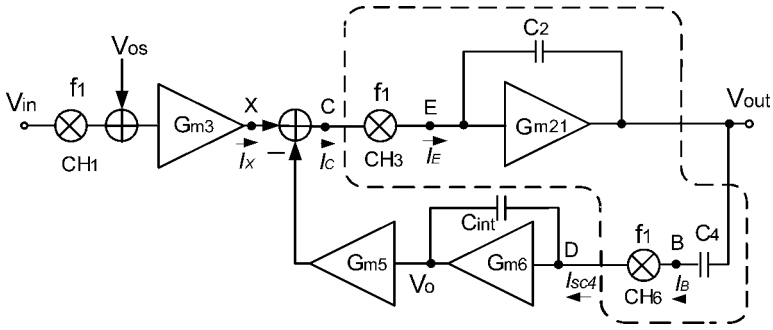

Fig. 8. Simplified block diagram of a CFIA with an AC-coupled RRL.

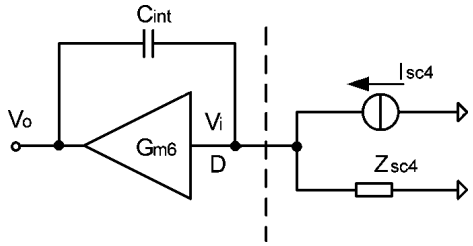

Fig. 9. Equivalent circuit of the integrator G_{m6} and C_{int}.

Since C_4 is chopped by CH_6, the switched-capacitor impedance Z_{SC4} looking into the chopper from the integrator's non-ideal virtual ground (node D) is given by

$$Z_{SC4} = 1/f_{ch1}C_4 \tag{6}$$

where f_{ch1} is the chopping frequency of CH_6 and the output V_{out} is assumed to be a virtual ground. The action of C_4 and CH_6 can then be modeled by the Norton equivalent circuit shown in Fig. 9.

From Fig. 9, the input voltage V_i can be derived as

$$V_i = I_{SC4}Z_{SC4} + (V_o - V_i)sC_{int}Z_{SC4} \tag{7}$$

By substituting (5) into (7), the transfer function $H(s)$ of the integrator can be calculated:

$$H(s) = \frac{V_0}{I_{SC4}} = -\frac{Z_{SC4}A_{06}}{1 + sZ_{SC4}(1 + A_{06})C_{int}}. \tag{8}$$

The loop gain $L(s)$ of the RRL can be expressed as

$$L(s) = K \cdot H(s) \cdot G_{m5}. \tag{9}$$

Substituting (4) and (8) into (9), the loop gain becomes

$$L(s) = \frac{C_4}{C_2} \cdot \frac{Z_{SC4}A_{06}}{1 + sZ_{SC4}(1 + A_{06})C_{int}} G_{m5}. \tag{10}$$

If $A_{06} \gg 1$, (10) can be simplified to

$$L(s) = \frac{C_4}{C_2} \cdot \frac{Z_{SC4}A_{06}}{1 + sZ_{SC4}A_{06}C_{int}} G_{m5}. \tag{11}$$

The loop gain $L(s)$ is plotted in Fig. 10(a). It is a first-order low-pass function with a dominant pole that is related to the chopping frequency by

$$f_{dominant,pole} = \frac{1}{2\pi A_{06}C_{int}Z_{SC4}} = \frac{f_{ch1}C_4}{2\pi A_{06}C_{int}}. \tag{12}$$

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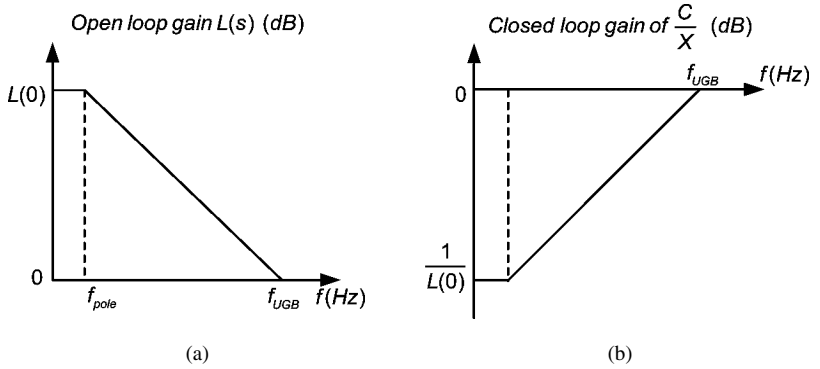

Fig. 10. Transfer function of the loop gain of the RRL.

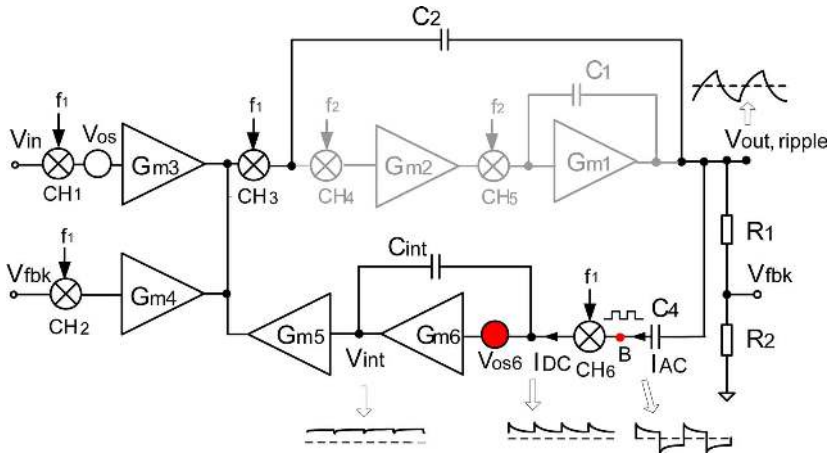

Fig. 11. Simplified block diagram of a three-stage CFIA with an AC-coupled RRL.

The DC loop gain $L(0)$ corresponding to the ripple reduction ratio is given by

$$L(0) = A_{06} G_{m5} \frac{C_4}{C_2} Z_{\mathrm{SC4}} = \frac{A_{06} G_{\mathrm{m5}}}{C_2 f_{\mathrm{ch1}}}. \tag{13}$$

The phase shift within the loop mainly originates from three blocks: integrator G_{m21} and C_2, a differentiator C_4 and an integrator C_{int}. In this design, $C_4 = 5$ pF, $C_{\mathrm{int}} = 80$ pF, $f_{\mathrm{ch1}} = 40$ kHz, A_{06} is about 114 dB, so the dominant pole is at around 0.8 mHz. Since the phase shift of the first two blocks cancel, the feedback loop is a first-order system having a phase margin close to 90°.

The closed-loop gain C/X between nodes C and X in Fig. 8 is plotted in Fig. 10(b). The transfer function is given by

$$\frac{C}{X} = \frac{1}{1 + L(s)} \approx \frac{1 + s Z_{\mathrm{SC4}} A_{06} C_{\mathrm{int}}}{s Z_{\mathrm{SC4}} A_{06} C_{\mathrm{int}} + \dfrac{C_4 Z_{\mathrm{SC4}} A_{06} G_{\mathrm{m5}}}{C_2}}. \tag{14}$$

This result indicates that the RRL high-pass filters the offset and $1/f$ noise of the input stage.

In this design, the DC loop gain is about 114 dB, which, neglecting other contributors to output ripple, means that even the worst-case ripple amplitude of 0.8 V should be reduced to microvolt levels. From (2) and (13), the ripple amplitude with the RRL is given by

$$V_{\mathrm{out\ ripple,RRL}} = V_{\mathrm{out,ripple}} / L(0) = \frac{V_{\mathrm{os}} \cdot G_{\mathrm{m3}}}{2 A_{06} \cdot G_{\mathrm{m5}}}. \tag{15}$$

The unity-gain bandwidth f_0 of the loop can be derived from (11) by setting $L(s) = 1$

$$L(s) = \frac{C_4}{C_2} \cdot \frac{Z_{\mathrm{SC4}} A_{06}}{1 + 2\pi f_0 Z_{\mathrm{SC4}} A_{06} C_{\mathrm{int}}} G_{m5} = 1 \tag{16}$$

$$f_0 = \frac{G_{\mathrm{m5}} C_4}{2\pi C_2 C_{\mathrm{int}}}. \tag{17}$$

In this design, $C_4 = 5$ pF, $C_{\mathrm{int}} = 80$ pF, $C_2 = 80$ pF and $G_{\mathrm{m5}} = 14$ μA/V, and so the unity-gain bandwidth is 1.74 kHz. Since the RRL functions as a narrowband notch-filter at the chopping frequency f_{ch1}, the notch bandwidth should be roughly equal to $2f_0$, i.e., about 3.5 kHz.

C. Cascode Buffer Isolation

As shown in Fig. 11, the offset of the integrator's amplifier G_{m6} determines the amount of residual ripple. This can be explained as follows: the offset of the transconductance stage G_{m6}, being chopped by CH_6, appears as a square wave voltage at node B. This square wave appears across C_4, and cannot be distinguished from the output ripple. As a result, the ripple will not be completely cancelled.

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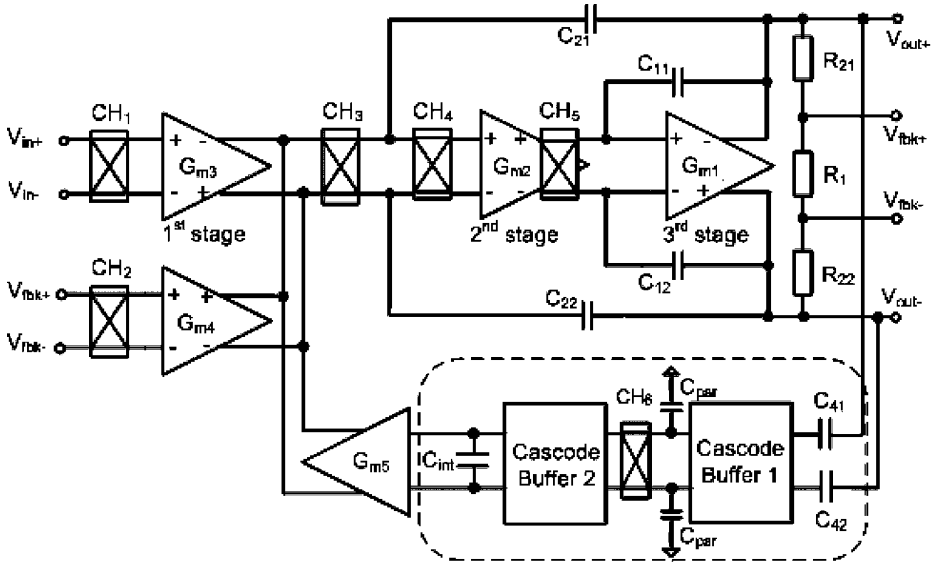

Fig. 12. Block diagram of the implemented fully differential CFIA.

This problem can be mitigated by chopper-stabilizing G_{m6}, or by using a gain-boosted cascode buffer 1 (CB1) to isolate $\mathrm{CH_6}$ from C_4, as shown in Fig. 12. The latter solution is chosen here, and as a result a much smaller C_{par} is obtained compared with C_4. C_{par} is now around 0.6 pF, while C_4 is 5 pF, which results in 8 times more ripple reduction. To minimize the effect of common-mode interference, the CFIA was implemented in a fully differential manner. The RRL's integrator was realized as a passive integrator, built around a second cascode buffer (CB2), because this only requires half the capacitor area required by an active integrator.

D. $1/f$ Noise Performance With RRL

The introduction of the RRL does not significantly affect the noise performance of the amplifier. This is because the CB2 and G_{m5} are located between the choppers $\mathrm{CH_3}$ and $\mathrm{CH_6}$ (Fig. 12), and so their $1/f$ noise contributions are chopped out. Although CB1 is not chopped, its $1/f$ noise is modulated to the chopping frequency by $\mathrm{CH_6}$, and then filtered by C_{int}. As a result, the amplifier still maintains its extremely low $1/f$ noise corner of 1 mHz.

E. Chopper Ripple From the Intermediate Stage

The ripple caused by the chopped offset of the intermediate stage is only weakly affected by the presence of the RRL. This is because it originates within the frequency compensation network, and so, compared to the chopped offset of the input stage, is filtered by a different low-pass filter. Therefore, the ripple associated with the intermediate stage was suppressed by chopping it at a much higher frequency (510 kHz) than the input stage. Although the increased frequency of the associated charge injection spikes will increase the offset of the intermediate stage, its impact on the overall amplifier's input-referred offset is mitigated by the gain of the input stage.

V. Detailed Circuit Implementation

A. The Cascode Buffers

The detailed implementation of the cascode buffers (dashed line in Fig. 12) is shown in Fig. 13(a). Transistors M_{25} and M_{26} act as CB1, while M_{23}, M_{24} act as CB2. To increase the output impedance of CB2, a gain-boosting topology was employed.

As discussed in Section IV-C, CB1 isolates $\mathrm{CH_6}$ from C_4 to enhance the ripple reduction. However, another significant source of residual ripple exists: the chopped offset of the booster amplifier $\mathrm{GB_n}$ which induces an AC current in the drain capacitances $C_{\mathrm{par1,2}}$ of the cascode transistors M_{25}, M_{26}. To reduce this, the position of the chopper was modified [Fig. 13(b)] so that these drain capacitances are located at the virtual grounds established by the gain-boosting amplifiers [19]. Now the offset of $\mathrm{GB_n}$ appears as a square wave at nodes 1 and 2 [Fig. 13(b)]. This square voltage charges and discharges $C_{\mathrm{par3,4}}$ and generates an AC current. To reduce this AC current, both $\mathrm{CH_6}$ and M_{23}, M_{24} were implemented with minimum size devices. The residual ripple caused by the chopped offset of $\mathrm{GB_p}$ was mitigated in the same manner. Any residual AC current is then filtered out by the integration capacitor C_{int}. It should be noted that mismatch in the current sources or between the resistors R_1 and R_2, also gives rise to residual ripple.

B. The Input Stage

Since the gain error of the thermistor bridge is 0.5%, the amplifier's gain accuracy was designed to be at the same level. This requires that the transconductances G_{m3} and G_{m4} be well matched. In consequence, the dimensions, bias currents and drain-source voltages of the input transistors should also be as well matched as possible.

As shown in Fig. 14, the input and feedback transconductances employ a folded cascode gain-boosted topology with 140 dB gain. The CM voltages of the two transconductances may differ, and so for good matching their $\mathrm{G_m}$ should be insensitive to CM voltage variations. Therefore, the drain-source voltages of the input transistors M_1, M_2, M_7 and M_8 were kept

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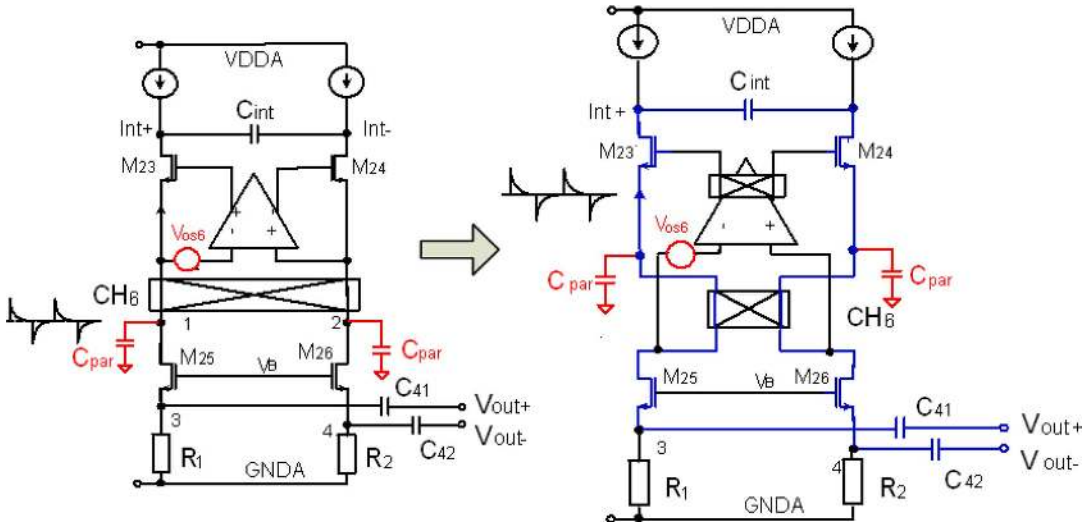

Fig. 13. Implementation of the gain-boosted cascode buffer.

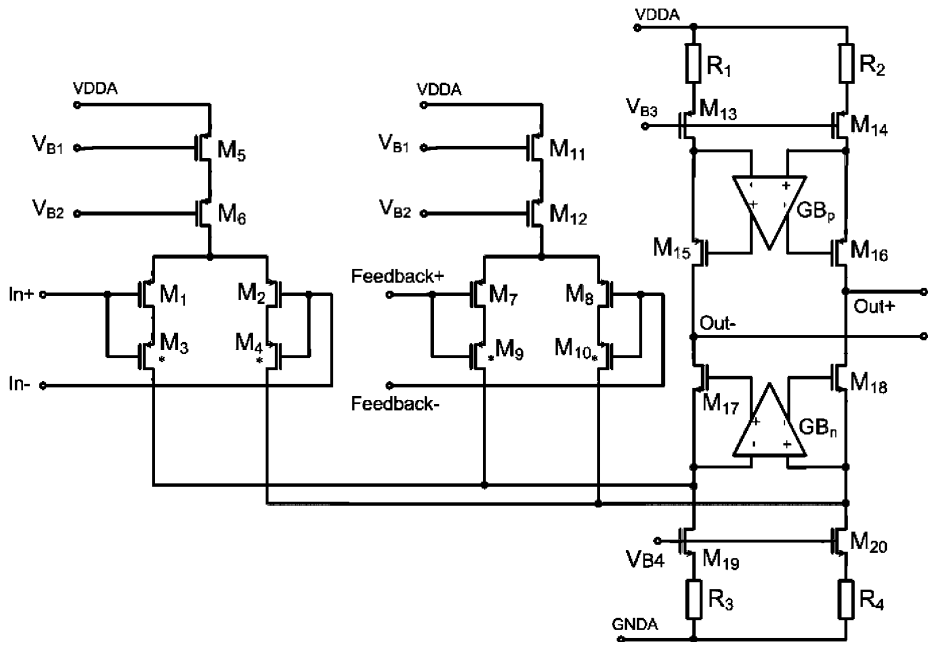

Fig. 14. Schematic of the input stage amplifier.

constant by low-threshold cascode transistors M_3, M_4, M_9 and M_{10}. For the same reason, the current sources M_5 and M_{11} are also cascoded. The transconductance of the input and feedback stages is 250 μA/V, corresponding to a noise-equivalent resistance of 4 kΩ. To reduce their noise contribution, the various current sources in the input stage were resistively degenerated.

C. The Intermediate and Output Stages

The schematic of the intermediate and output stages is shown in Fig. 15. The intermediate stage was implemented using a folded-cascode topology. A class-AB output stage was implemented to achieve rail-to-rail output. To save power, the class-AB mesh structures M_5–M_{12} were incorporated into the output branch of the intermediate stage [13]. The class-AB mesh was also cascoded to reduce the variation of the drain-source voltages of M_5, M_9, M_8, M_{12}. To achieve better settling, the demodulation choppers CH_{51} and CH_{52} should be located at the non-dominant poles of the intermediate stage. Therefore, choppers CH_{51} and CH_{52} were located at the "quiet" sources of the cascode transistors M_3 and M_4. Since the thermal noise of the intermediate stage is suppressed by the gain of the input stage, the differential pair was biased at only 4 μA, resulting in a G_m of 20 μA/V. The unchopped cascode transistors $\mathrm{M}_3, \mathrm{M}_4, \mathrm{M}_{34}, \mathrm{M}_{36}$ are the main source of residual $1/f$ noise. However, this is suppressed by the gain of the preceding stages.

VI. Measurement Results

The current-feedback instrumentation amplifier was realized in a 0.7 μm CMOS process with low-threshold transistors, linear

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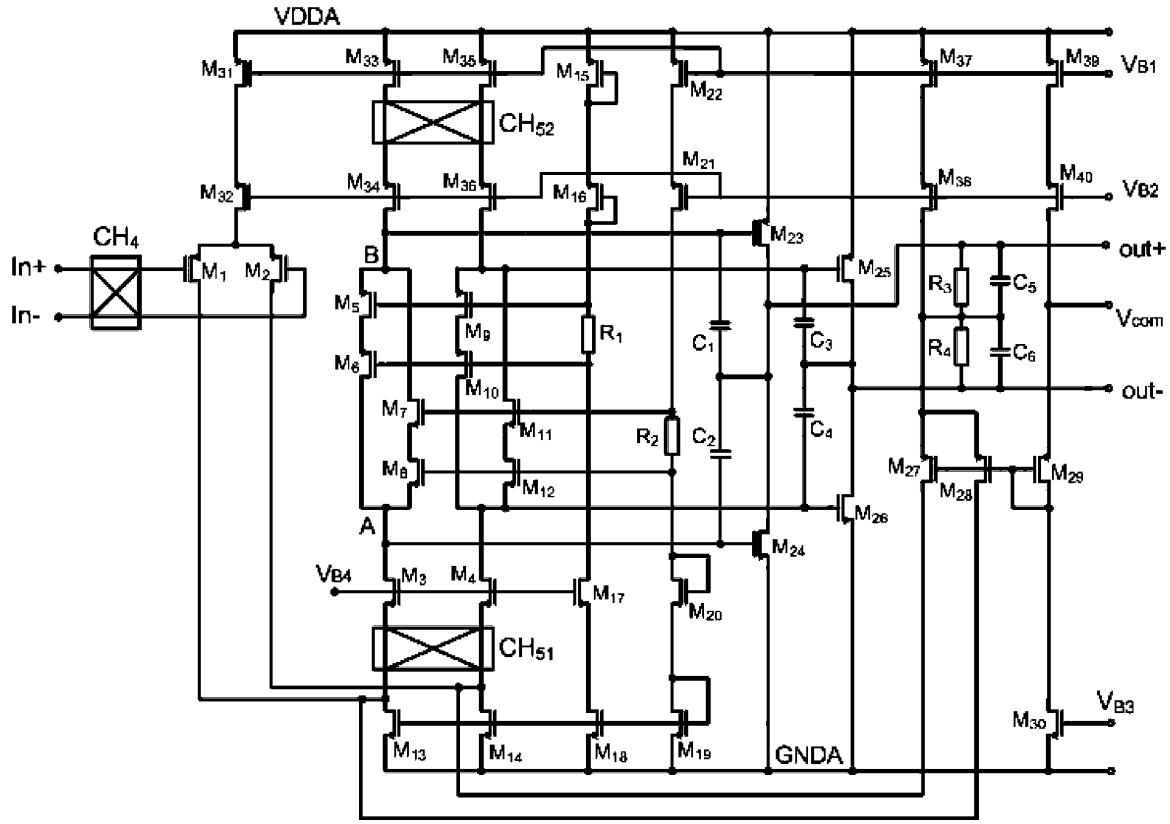

Fig. 15. Schematic of the intermediate and output stages.

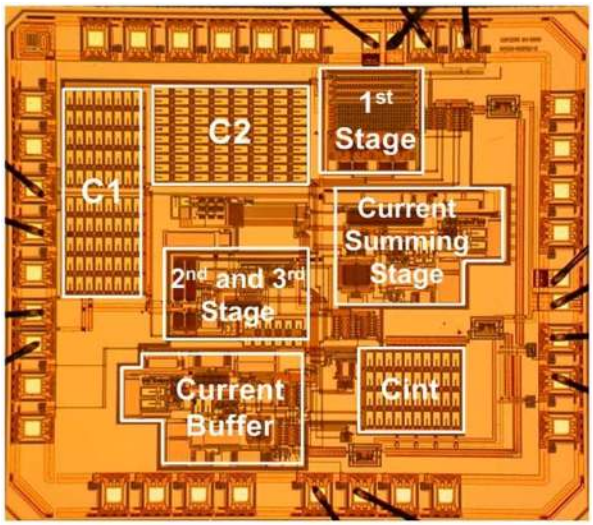

Fig. 16. Chip micrograph of the implemented CFIA.

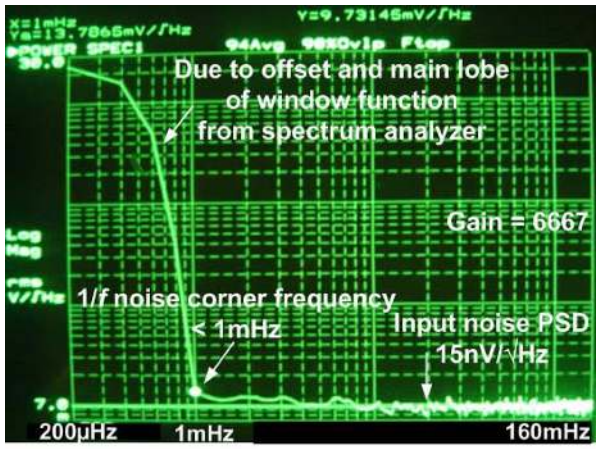

Fig. 17. Measured output noise spectrum from 200 μHz to 160 mHz.

capacitors and high-resistivity poly resistors. The active chip area is 4.8 mm^2 (Fig. 16). To ensure that the CFIA's $1/f$ noise is dominant, the noise measurements were made with the CFIA configured for a closed-loop gain of 6667 and followed by a low-noise amplifier with a gain of 100. Thus, the contribution of the LNA and the HP3562A spectrum analyzer to the measured $1/f$ noise is negligible. Without chopping, the amplifier has a white noise floor of 15 nV/$\sqrt{\text{Hz}}$ and a $1/f$ noise corner of 3 kHz. Chopping only the input stage resulted in a $1/f$ noise corner of 0.1 Hz. After chopping both the input and intermediate stages, however, the measured noise spectral density remained flat to 1 mHz. Since the amplifier's offset is smeared out by the window function of the spectrum analyzer (HP3562A), the $1/f$ noise corner could not be accurately measured, but it is clearly below 1 mHz, as shown in Fig. 17. This agrees well with the simulation results.

As stated in Section IV, the RRL acts like a notch filter at the chopping frequency. Since the notch is quite narrow, it has little effect on the amplifier's measured closed-loop response (Fig. 18). The closed-loop response around the chopping frequency is shown in Fig. 19. The measured width of the notch,

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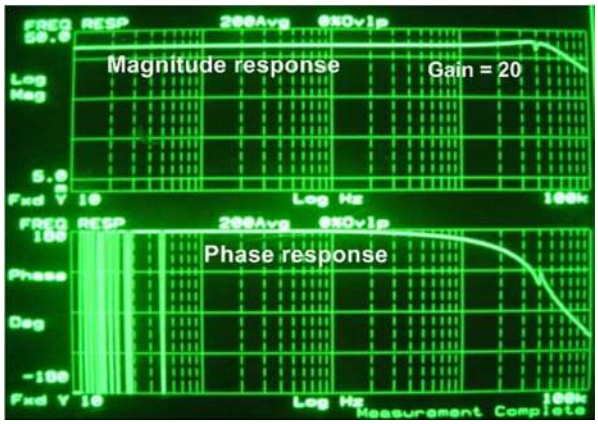

Fig. 18. Measured frequency response of the CFIA (gain of 20, $f_{ch1} = 40$ kHz, $f_{ch2} = 510$ kHz).

Fig. 19. Measured frequency response of the CFIA around the chopping frequency.

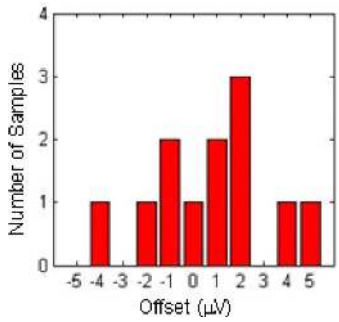

Fig. 20. Measured offset histogram of 12 samples.

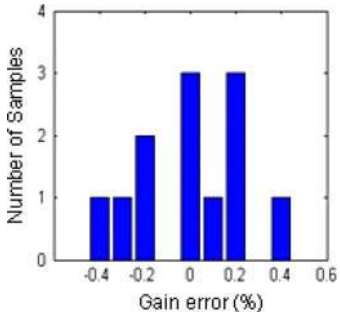

Fig. 21. Measured gain error histogram of 12 samples.

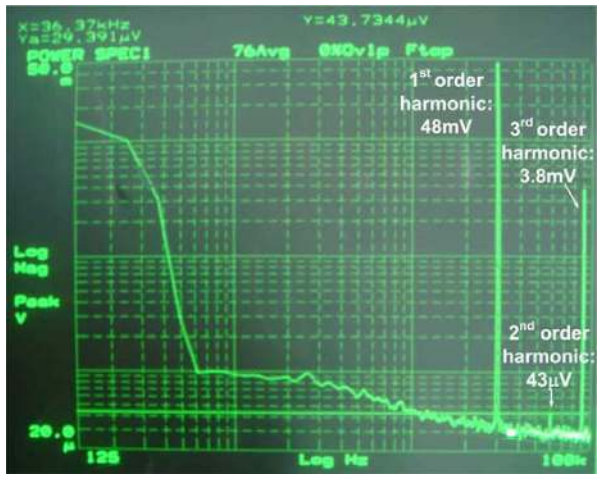

Fig. 22. Measured chopper ripple with the RRL "off".

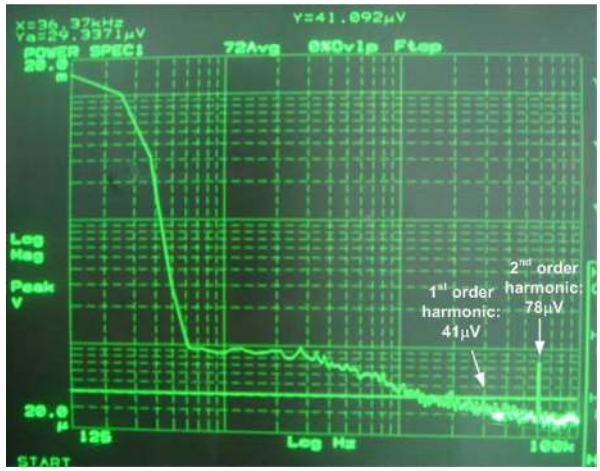

Fig. 23. Measured chopper ripple with the RRL "on".

roughly 3.4 kHz wide at a gain of 20 and $f_{ch1} = 40$ kHz, agrees well with the calculations presented in Section IV-B.

Without chopping, the initial offset of the CFIA is less than 1.7 mV. Chopping only the input stage results in a measured offset of less than 1 μV. Chopping both the input and intermediate stages increases the offset to 5 μV, mainly due to the relatively high chopping frequency (510 kHz) used in the intermediate stage. The measured offset of 12 samples is shown in Fig. 20. Their measured gain accuracy is shown in Fig. 21, and was less than $\pm 0.5\%$ at a nominal gain of 200.

The spectrum of the chopper ripple with and without the RRL is shown in Figs. 22 and 23. Since the frequency range of the HP3562A spectrum analyzer was limited to 100 kHz, the input choppers CH_1, CH_2, CH_3, CH_6 were clocked at $f_{ch1} = 30$ kHz in order to observe the 3rd harmonic of the chopping frequency. Measurements show that the amplitude of the output ripple at f_{ch1} was reduced by about 60 dB: from 48 mV to 41 μV. However, a larger second harmonic (78 μV) is also visible. This is due to the chopped mismatch of the

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TABLE II
PERFORMANCE COMPARISON OF LOW-POWER CHOPPER AMPLIFIERS

	This work	[3]	[2]	[10] in two opamp IA	[4] in two opamp IA
Year of publication	2009	2008	2007	2006	2002
1/*f* noise corner	1mHz	3Hz	1Hz	-	30mHz
Noise PSD	15nV/√Hz	55.8nV/√Hz	94nV/√Hz	76nV/√Hz	9.2nV/√Hz
Offset	5μV	-	--	6μV	8μV
GBW	800kHz Stable Gain > 20	350kHz	20kHz	350kHz	5MHz
Chopping frequency	40k,510kHz	-	4kHz	125kHz	200kHz
CMRR	>120dB	> 120dB	100dB	130dB	---
PSRR	>120dB	90dB	---	113dB	120dB
Supply current	230μA	2.3μA	1.2μA	34μA	3.6mA
NEF[20]	8.8	4.1	4.6	18.4	21.6

current sources M_{25}, M_{26} and the offset of the booster amplifiers [Fig. 13(b)], which CH_3 then up-modulates to the even harmonics of f_{ch1}. However, at the closed-loop gains for which the amplifier was designed (> 20), the amplifier's bandwidth is low enough to effectively filter out such harmonics. At a gain of 200, the amplifier's bandwidth is 4 kHz and the measured input-referred output ripple and noise are 0.55 μV(rms) and 0.95 μV(rms), respectively. Depending on the offset in the intermediate stage, the amplitude of the corresponding output ripple (at 510 kHz) varies from 0 to 70 μV.

In Table II, the performance of this instrumentation amplifier is compared with the state of the art. It achieves a 1 mHz $1/f$ noise corner at a noise PSD of 15 nV/$\sqrt{\text{Hz}}$. This extremely low $1/f$ noise and thermal noise have been achieved with low power consumption (230 μA from a 5 V supply): the amplifier's noise-efficiency factor [20] is 8.8, which is quite respectable [2]–[4], [10].

VII. CONCLUSION

To interface a precision thermistor bridge intended for high-resolution temperature measurements in wafer-steppers, a three stage current-feedback instrumentation amplifier has been designed. The goal of the design was to achieve low thermal noise and low $1/f$ noise, and simultaneously, the low power dissipation required to reduce self-heating errors. By chopping both the input and intermediate stages, their $1/f$ noise was effectively suppressed, while the $1/f$ noise of the output stage was suppressed by the gain of the preceding stages. A continuous-time ripple reduction loop was applied to reduce chopper ripple without any noise aliasing, which, compared to the use of auto-zeroing, results in a very power efficient solution.

The performance of the CFIA was evaluated by measurements on a test chip realized in a standard 0.7 μm CMOS process. The amplifier achieves 5 μV offset and a $1/f$ noise corner of 1 mHz at a thermal noise PSD of 15 nV/$\sqrt{\text{Hz}}$, while only drawing 230 μA supply current. To the authors' knowledge, this represents the best LF noise performance ever reported for a CMOS amplifier.

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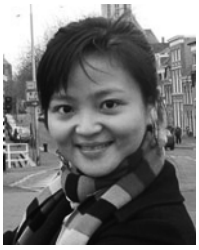

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In 1992 Dr. Huijsing initiated the International Workshop on Advances in Analog Circuit Design, which he co-organized yearly until 2003. He was a member of the program committee of the European Solid-State Circuits Conference from 1992 until 2002. He was Chairman of the Dutch STW Platform on Sensor Technology and of the biannual National Workshop on Sensor Technology from 1991 until 2002. He is a Fellow of IEEE, and was awarded the title of Simon Stevin Meester by the Dutch Technology Foundation.

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