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A Circuit Based Behavioral Modeling of Continuous-Time Sigma Delta Modulators

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Abstract—In evaluating Continuous-Time Sigma Delta ($\Sigma\Delta$) Modulators, the generation of highly accurate results requires long simulation time due to the nonlinear nature of the system. In most cases, a compromise has to be made to trade off precision for speed [2]. This paper presents a circuit-based high level model implemented in the MATLAB SIMULINK environment so as to achieve a faster speed of simulation. Designed in a differential manner, the model provides good visualization of the actual circuit at the early stage of design. To maintain simulation accuracy, circuit nonidealities such as system clock jitter, integrator noise, opamp finite gain, bandwidth and slew rate as well as the digital to analog converter (DAC) mismatches are included in the model. For demonstration purpose, a 4th order CT $\Sigma\Delta$ modulator with NRZ (Non-Return to Zero) architecture is implemented. With the proposed models, key design specifications for the functional building blocks are derived.

Index Terms— Analog-to-digital (A/D) conversion, behavioral modeling, continuous-time (CT), sigma-delta ($\Sigma\Delta$) modulation

I. INTRODUCTION

Sigma Delta ($\Sigma\Delta$) Modulators had been extensively used in applications where a high resolution is required over a moderately small signal bandwidth. Classified broadly as oversampling converters, there are in general two classes of $\Sigma\Delta$ modulators, namely the discrete time (DT) switched capacitor (SC) and the continuous time (CT) family. In recent years, the CT $\Sigma\Delta$ modulator has been gaining popularity, attributing mainly to characteristics such as its inherent anti-aliasing property and the possibility of achieving lower power consumption as a result of less stringent requirements on the speed of the CT integrators [1].

Due to the non linear nature of the sampling process at the internal quantizer, the analysis of CT $\Sigma\Delta$ modulators is a tedious process. This often translates to lengthy time domain simulations especially when evaluating high performance CT $\Sigma\Delta$ modulators. It is therefore necessary to have a high level model that can be used to determine the performance of the modulator under the influence of circuit level nonidealities. In the aim to improve the speed of simulations, the accuracy of simulations is often sacrificed.

This work proposes a high level circuit based fully differential model for the CT $\Sigma\Delta$ modulator implemented entirely in the MATLAB SIMULINK environment. In preserving the accuracy of the simulations, detailed modeling

of circuit level nonidealities is included. The model allows comprehensive time domain analysis of the modulator nonlinear system at a much faster rate compared to SPICE simulations.

The paper is organized as follows. Section II describes the modeling concepts for the individual blocks with nonidealities. In section III, the implementation of the 4th order CT $\Sigma\Delta$ modulator is discussed. Section IV discusses the simulations obtained before concluding the paper.

II. MODELING CONCEPTS

A. MATLAB Physical Domain Modeling

In SIMULINK, it is possible to place physical components such as resistors and capacitors for simulations. These components reside in the physical domain. For implementation purpose, the basic resistor and capacitor required in the proposed model is taken from the SIMULINK SimPowerSystems toolbox [3]. An interface has to be inserted between the normal SIMULINK data signal domain and the physical domain. These interfaces are required when signals propagate to and fro the two domains. A controlled voltage source is required when moving from the signal to the physical domain. Conversely, transiting in the reverse direction from the physical domain back to the signal domain needs a voltage measurement block. Fig. 1 illustrates the propagation of signals between the two domains.

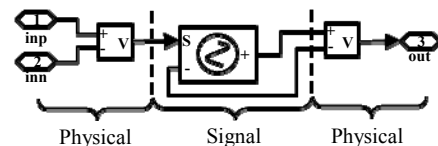


Figure 1. Transition of data between the signal and physical domains

B. $\Sigma\Delta$ Modulator Nonidealities

A typical single loop single bit CT $\Sigma\Delta$ modulator may consist of a continuous time RC integrator as the first stage, transconductor (gmC) cells as the subsequent stages, a quantizer and a single bit feedback digital-to-analog converter (DAC). This section focuses on the modeling of nonidealities

of the functional blocks within the CT $\Sigma\Delta$ modulator. The main non-idealities that are considered include the following:

1. System Clock Jitter;
2. Thermal and Flicker noise of first integrator;
3. Finite gain and bandwidth of first opamp;
4. Slew rate of first opamp;
5. Linearity and distortion of first opamp;
6. Saturation voltage of first opamp;
7. DAC mismatches.

C. System Clock Jitter

Clock jitter has always been the fundamental performance limitation for CT $\Sigma\Delta$ modulators. Variations from ideal clock edges vary the feedback pulse length and hence the total effective feedback charge. This behavior increases the noise floor across the frequency band. This phenomenon is especially critical when occurring at the feedback DAC. It is because this noise cannot be shaped by the system when injected at that point. Independent clock jitter approximation is the most widely used model for performance prediction in high level simulations. In this approach, clock jitter is modeled as an additive timing error on the ideal clock edges. A SIMULINK model has been proposed by [4]. Alternatively, phase noise modulation can be applied to an ideal clock. However, such approaches produces time domain simulations that are extremely time consuming due to small timing variations. A more efficient method would be to transform pulse width variance to pulse amplitude variation. In [5], the author proposed a jitter model specifically for NRZ feedback pulse. A jitter model for the NRZ feedback pulse is shown in Fig. 2.

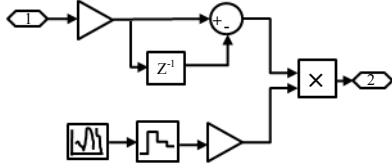


Figure 2. Jitter Model for Non-Return to Zero (NRZ) Implementation

It is to be mentioned here that the amplitude modulation only ensure first order accuracy since pulse position jitter is not considered. However, since pulse position variation is at least first order noise shaped, its effect is relatively insignificant. Specifically speaking, for feed forward structures, only one feedback path is used, thus this model is particularly suitable for FF implementation.

D. Thermal and Operational Amplifier Noise

The dominant noise source in an active RC integrator comprised of the white noise contributed by both the input and feedback resistors in addition to the input referred amplifier noise which consists of input flicker (1/f) noise, wide band thermal noise and amplifier dc offsets. These values are obtained through SPICE simulation. Subsequently, all the individually input referred noise power spectral density

attributed to all the noisy devices are summed together before integrated across the signal bandwidth in concern.

According to [1], the total input-referred noise power is given by equation (1):

$$V_{noise}^2 = 16KTf_B(R_{in} + R_{fb}) + \frac{128KTf_B n_{e,th}}{3g_{m,OTA}} + \frac{8K_f n_{e,th}}{C_{ox}^2 WL} \ln\left(\frac{f_B}{f_u}\right) \quad (1)$$

The total RMS noise voltage, V_{noise} is superimposed to the input signal leading to equation (2):

$$V_{out}(t) = V_{in}(t) + V_{noise} \cdot n(t) \quad (2)$$

where $n(t)$ denotes a Gaussian random process with unity standard deviation. Equation (2) can be implemented by the SIMULINK model shown in Fig. 3.

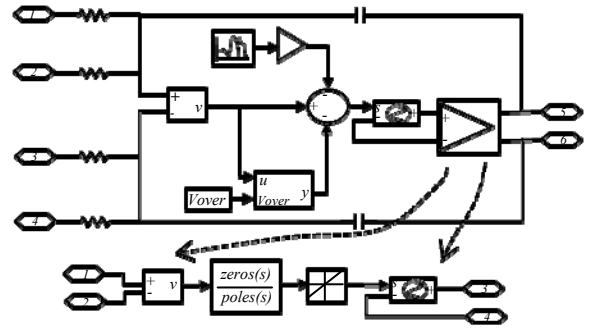


Figure 3. First RC nonidealities modeling including opamp 1/f noise, resistors thermal noise, finite opamp linearity, finite dc gain and GBW, slew rate and saturation voltage

E. Operational Amplifier and its Nonidealities

The integrator circuit implementation deviates from the ideal behavior due to several non ideal effects such as the finite op-amp gain and bandwidth, slew rate and saturation voltage. To make it as realistic as possible, an amplifier with a two poles and one zero transfer function has been adopted. The non dominant amplifier second pole and amplifier zero are chosen such that it results in a practical amplifier with a phase margin of approximately 60° . Modeling of such a real integrator with all non idealities is shown in fig. 3.

The finite gain bandwidth product (GBW) of the opamp can be model as some form of 'leakage' whereby only a fraction of the previous output is added to each new input sample. Hence, the transfer function of a real op amp is given by equation (3):

$$H(s) = \frac{\sqrt{A_V}}{\left(\frac{s}{\omega_1} + 1\right)} \cdot \frac{\sqrt{A_V}}{\left(\frac{s}{\omega_2} + 1\right)} \cdot \left(\frac{s}{\omega_Z} + 1\right) \quad (3)$$

where A_V denotes the op amp dc gain; $\omega_1, \omega_2, \omega_3$, represents the first, second amplifier pole and zero respectively.

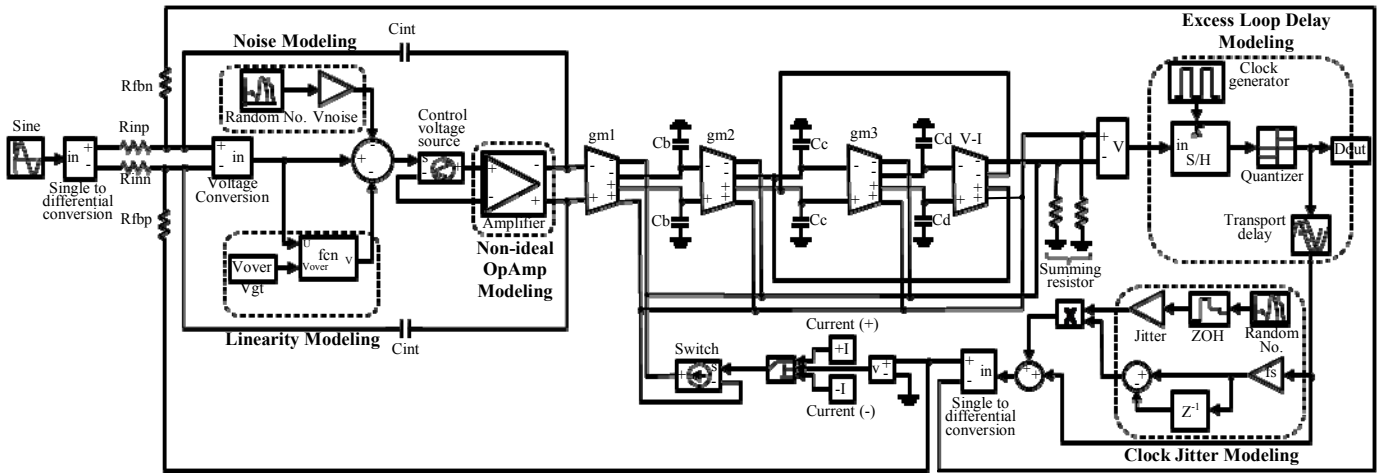


Figure 4. Entire differential model for the 4th Order Non-Return to Zero (NRZ) CIFF CT $\Sigma\Delta$ modulator

The op-amp slew rate limitation and the saturation levels are modeled in SIMULINK using the slew rate and saturation blocks, placed in series with the integrator as shown in Fig. 3. According to [6], the 3rd harmonics distortion of the $\Sigma\Delta$ modulator is given by equation (4),

$$HD3 = \frac{g_3}{16g_1^4} \cdot \left(\frac{1}{R_{in}} + \frac{1}{R_{fb}} \right) \cdot \left(\frac{\hat{v}_{in}}{R_{in}} \right)^2 \quad (4)$$

Using the square-law model of a MOS transistor, the non-linear transconductance of the opamp input pair can be derived from transistors operating in the strong inversion as given region by equation (5):

$$g_1 = \frac{I_D}{V_{GT}} = \frac{g_m}{2}; \quad g_3 = \frac{I_D}{8V_{GT}^3} = \frac{g_m^3}{64I_D^2} \quad (5)$$

where V_{GT} is the effective gate-source voltage and g_m is the transconductance of the input transistors.

F. Transconductor (gmC) Modeling

In the design of higher order CT $\Sigma\Delta$ modulators, the more power efficient transconductor (gmC) structure is usually considered from the second integrator onwards. The S-domain transfer function for a generic transconductor based integrator (gmC) is given by $H(s)=gm/sC$. Fig. 5 illustrates the model for the gmC cell.

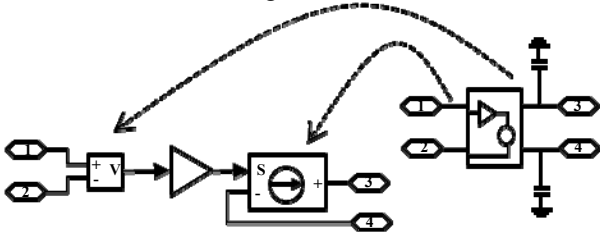


Figure 5. Transconductor (gmC) cell Model

The input voltage signal is converted into a current signal that charges the load capacitor. Since the nonidealities of the integrators beyond the first do not generate significant degradation in the performance of the

CT $\Sigma\Delta$ modulator, [5], [6], its nonidealities are often neglected when considering the high level model.

III. IMPLEMENTATION EXAMPLE

To illustrate some key design insights and to validate the modeled non-idealities, this section demonstrates the design of a 4th-order CT $\Sigma\Delta$ modulator in the NRZ (Non-Return to Zero) architecture. As such, the top level design target specifications for the implementation examples are summarized in Table. I.

TABLE I. DESIGN SPECIFICATIONS SUMMARY

Design Parameters	Design Summary for NRZ Implementation
Architecture	Cascade Integrators Feed Forward (CIFF)
Order	4
Input Signal Bandwidth	25kHz
Oversampling Ratio (OSR)	64
Peak SNR	85dB

The proposed modeling technique will be used to simulate for the key functional blocks requirements for this fourth order CT $\Sigma\Delta$ modulator needed to fulfill the above specifications. The RC integrator is chosen for the first integrator for linearity reasons. The second, third and fourth integrators are realized with transconductors (gmC) structures so as to conserve power. The modeling is done in a fully differential fashion, hence allowing a closer visualization of the actual circuit. In particular, the first integrator design specifications will be fully derived.

A. Non-Return to Zero (NRZ) Implementation

In the NRZ implementation, the DAC feedback pulses are held constant for each entire sampling period without being returned to the common mode voltage as like the Return-to-Zero (RZ) case. The coefficients for the loop filter are used to calculate for the physical design values of the resistors and charge storing load capacitors. Fig. 4 shows the structure for the NRZ architecture. The feed forward output currents from the gmC cells are summed across a resistor as accordance to the CIFF structure. This technique is seen in

[7] to convert the current back into a voltage signal for comparison by the single-bit voltage comparator. The excess loop delay is compensated by having a direct path across the loop filter. In order to model this compensation feedback path, it should be noted that the path can be thought of as a single-bit feedback DAC that feeds back a scaled current signal back into the summing resistor whose value is decided by the quantizer output signal. Each key component specification was then simulated against the design requirements to find out the least stringent value necessary.

IV. RESULTS

The implemented modulator was simulated to evaluate the maximum tolerance of the architecture on the modeled non-idealities while fulfilling the specifications presented in section III. Table II summarized the minimum functional blocks requirements needed to achieve the targeted specifications with the non-idealities modeled.

TABLE II. MINIMUM DESIGN REQUIREMENTS

Modulator Non-idealities	Value
Input referred noise	150 μ Vrms
Linearity (HD3) with Vgt of the op-amp input devices	0.14V
Finite gain bandwidth (GBW)	4.9MHz
Finite DC gain	75dB
Slew rate (positive & negative slew)	1.2V/ μ s
Saturation voltages	\pm 0.5V
Clock jitter	0.005%Ts
Excess loop delay	Ts

Fig.6 shows the PSD plots for the implemented modulator. The input frequency is chosen to be at 7 kHz for the simulations so that the third harmonics falls within the signal bandwidth. To evaluate the peak Signal to Noise Ratio (SNR), the input range was swept across the entire dynamic range. A plot of the SNR was then plotted against the input values as shown in Fig.7.

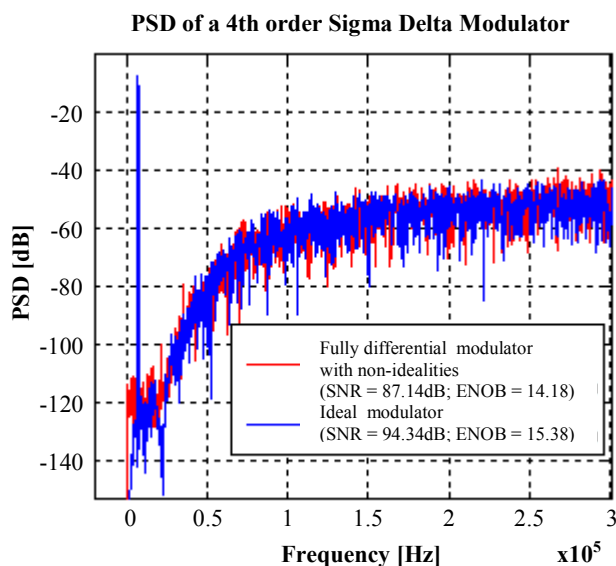


Figure 6. Power Spectral Density (PSD) plot

Input Dynamic Range of 4th order Sigma Delta Modulator

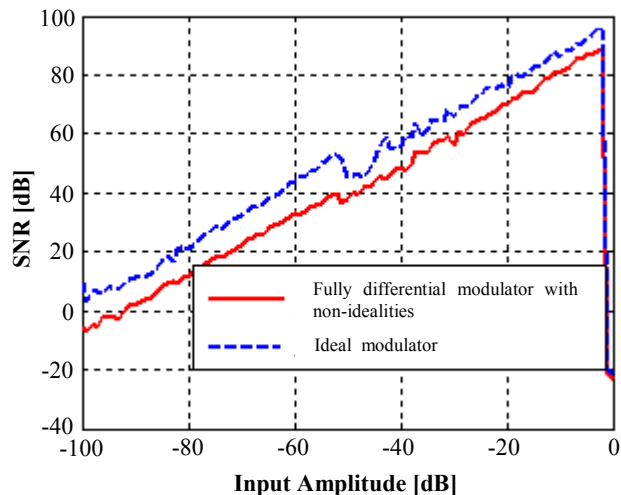


Figure 7. Input dynamic range Plot

V. CONCLUSION

In this paper, a high level circuit based fully differential model for the CT $\Sigma\Delta$ modulator implemented in SIMULINK has been proposed. To ensure accurate simulations, various non-ideal effects have been discussed and incorporated into the proposed model. The fully differential structure enables realistic and intuitive modeling. A 4th order CT $\Sigma\Delta$ modulator was implemented using the proposed modeling. Results indicating the minimum requirements for the functional blocks were presented. This modeling technique can be included as a high level evaluation step within the design flow and hence improving the design time for CT $\Sigma\Delta$ modulators.

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