01 Dec 2008

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Recommended Citation

B. Seol et al., "A Circuit Model for ESD Performance Analysis of Printed Circuit Boards," *Proceedings of the 2008 Electrical Design of Advanced Packaging and Systems Symposium, 2008*, Institute of Electrical and Electronics Engineers (IEEE), Dec 2008.
The definitive version is available at https://doi.org/10.1109/EDAPS.2008.4736014

A Circuit Model for ESD Performance Analysis of Printed Circuit Boards

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***Abstract*— This paper provides a SPICE-compatible circuit model for characterizing electrostatic discharge (ESD) clamping performance of protection devices mounted on printed circuit boards (PCBs). An equivalent circuit model for a commercial ESD generator is introduced and a simulation methodology of an ESD protection device with non-linear resistance characteristic using voltage controlled current source is described. These models combined to create a full circuit model with a PCB model in a SPICE-like circuit simulator. Comparison results between the simulated and measured are presented to verify the accuracy of the proposed circuit model. A trade-off analysis between the ESD clamping performance and signal integrity with the ESD protection device in high-speed applications is also presented as a case study.**

I. INTRODUCTION

Electrostatic discharge (ESD) is a critical design and regulation assurance issues in modern electronic products, especially portable products including MP3 player, digital camera, camcorder and cellular phone. When an ESD occurs on an electronic product, a current is induced on the printed circuit board (PCB) within the product. This induced current can lead to malfunction of the product. In order to determine the robustness against ESD, manufactures test their product to the IEC standard [1], and typically this performed up to 8 kV contact discharge, although some products are tested up to 15 kV or higher. ESD generators are used for testing the immunity of electronic products based on the IEC standard. The IEC standard requires the ESD generator to apply a pulse of about 60 ns width through a 330 Ω resistor and a 150 pF capacitor, producing a peak current of over 25 A for a 8 kV discharge.

Most of circuit or system designers of modern electronic products typically solve ESD problems by trial and error approach with existing hardware. However, this is time-consuming and increasing development costs by iterating design cycle times. A suitable alternative is moving ESD problem-solving processes into an early design phase by applying simulation without hardware. ESD simulation helps circuit and system designers to consider a wide range of alternative designs by evaluating their performance quickly. There are two approaches that circuit and system designers can take to protect their products against ESD. One is mechanical enclosure or chassis design and the other is electrical circuit design on the PCB. This paper will focus on methods for simulating ESD clamping performance to support electrical circuit design of the PCB at early design phase.

There are two factors in ESD simulations using electro-magnetic field solvers that limit investigations to relatively simple structures: most of real PCBs are too complex to be simulated and ESD generator needs to be simulated using relatively high degree of detail. This leads a strong interest in ESD simulations using circuit simulators such as SPICE-like simulator. This paper describes a new methodology to develop the building blocks for circuit simulations of signal paths on PCBs with non-linear ESD protection devices that can be reused in future designs. The model proposed here is a combined model between a circuit simulator and a PCB simulator. The ESD generator is simulated here in a SPICE-compatible circuit model and optimized to match the measured results. The complete geometry of the PCB is simulated using a commercial PCB simulator, which uses the full-wave finite-element computation algorithm. These simulation models are integrated in a commercial SPICE-like circuit simulator for ESD performance simulations. This model can be used to simulate ESD clamping performance of PCBs in an early design phase.

II. CIRCUIT MODEL

A. ESD Generator

ESD generator modeling and simulation have been the research topic of multiple groups. A variety simulation methodologies proposed by the research groups can divided them into equivalent circuit models using SPICE-like circuit simulators [2]-[4] and full-wave models using electromagnetic field solvers [4]-[6].

In this paper, an ESD generator modeled based on the equivalent circuit model proposed in [3] as shown Fig. 1 and the component values in the circuit model was optimized to fit the simulated current to the measured current injected at the discharge tip of a commercial ESD generator. The circuit model cannot predict radiated or transient field coupling to the

circuit, however, in a small device like an MP3 player the injected current will dominate the currents in the device relative to the fields radiated from the ESD generator. The accuracy of the ESD generator model is verified with the measured data.

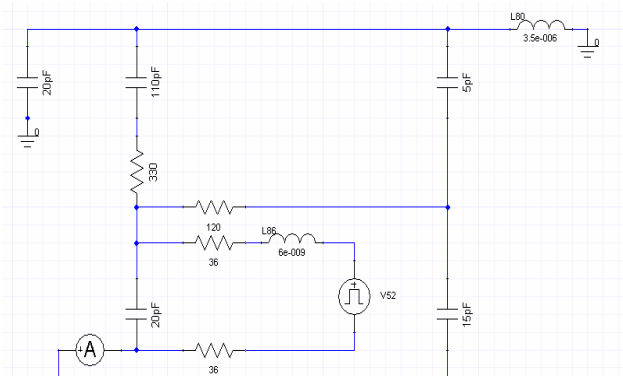


Fig. 1 Equivalent circuit model of the ESD generator

B. Printed Circuit Board

Signal paths on PCBs are modeled by a commercial PCB simulator using full-wave finite-element computation algorithm. This tool can extract frequency-dependent circuit models of complex PCBs directly from physical CAD layout with relatively short computational times. Such circuit models can be imported into SPICE-compatible circuit simulators for time- and frequency-domain analyses. Fig 2 shows an example of model for simulating a test PCB having a simple geometry.

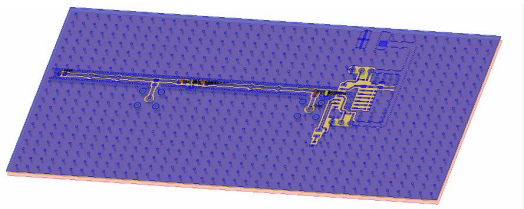


Fig. 2 Simulation model of the printed circuit board

C. ESD Protection Device

There are a variety of ESD protection devices. We can distinguish these devices into two important classes, linear and non-linear devices. Linear devices include capacitors, resistors, ferrite beads and combination of them. Non-linear devices include varistors, transient voltage suppressor (TVS) diode, spark gaps, non-linear polymers and combination of linear and non-linear devices.

A modeling methodology of varistors with non-linear resistance characteristic is described here as a case study. A varistor or voltage-dependent resistor is a non-linear resistor. Its resistance is high when the magnitude of the voltage across it is low and its resistance is low when the magnitude of the voltage across it is high [7], [8].

A varistor circuit model can be created using SPICE components. The accuracy and simulation time of the varistor model in a SPICE-like circuit simulator will be restricted by the non-linear block expressed in polynomial equation with several coefficients [9]. In order to model a non-linear resistance characteristics of the proposed model in this paper, the non-linear block is created using a polynomial expression in the SPICE voltage controlled current source 'G' command. The polynomial is generated using the theoretical equations and measured the clamping voltage and current flowing through the varistor to improve the accuracy of circuit simulation.

The non-linear resistance characteristics of the varistor can be expressed in exponential function $Iv = KVc^{\alpha}$. Here, Vc is the clamping voltage on the varistor and Iv is the current flowing on the varistor for given clamping. The Vc and Iv can be measured using a specially designed test PCB with the varistor mounted. We can put the measured Vc and Iv values for two different source voltages into the following equation to get the value of α:

$$\alpha = \log(Vc2/Vc1) / \log(Iv2/Iv1)$$

After we got the value of α, we can calculate the value of K using the V-I curve equation. The capacitance of the varistor is placed in parallel to the controlled source.

Fig 3 shows a specially designed test PCB with the varistor mounted in order to measure the Vc and Iv. For the measurement of the Iv, a 50 ohm coaxial cables is connected to the embedded loop probe structure on the bottom layer of the PCB. The loop probe is located right under the signal trace and consists of two through-hole vias and two traces. One trace is in the second layer and the other is in the bottom layer. The other end of the coaxial cable is connected to a digital oscilloscope. An attenuator protects the oscilloscope. It may be necessary to add ferrite beads onto the coax cable. Two 50 ohm coaxial cables connect via SMA connection on the test PCB to the oscilloscope, which is not visible in the figure, in order to measure the Vc for two different source voltages. A measured Vc-Iv curve of an 18 V, 40 pF varistor is shown in Fig. 4.

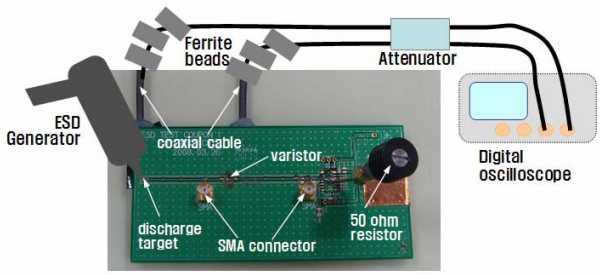


Fig. 3 Test PCB with the varistor mounted

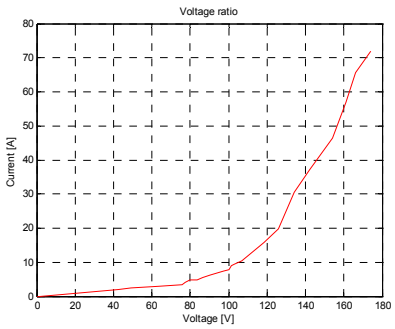


Fig. 4 Voltage vs. current of a varistor

The varistor model is described by using SPICE-compatible parameters, which the designers can access in the model library available with many commercial SPICE-like circuit simulator. The basic response of the varistor can be modeled by a non-linear resistor parallel connected with a capacitor as shown in Fig. 5. The non-linear resistor can be expressed by a voltage controlled current source in the circuit model. The relation between voltage and current of the controlled source can be described mathematically by the following equation:

$$Iv = 1.47 \times 10^{-11}\, Vc^{7}$$

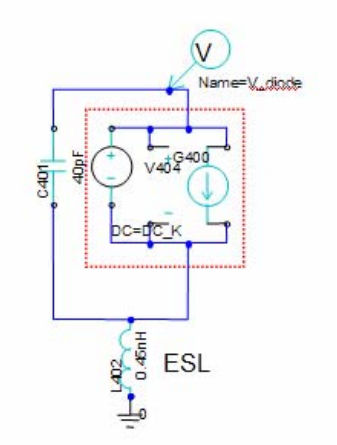


Fig. 5 SPICE circuit model for an 18V, 40pF varistor

D. Full Circuit Model

Circuit models described in previous sections are combined in a full circuit model to be simulated in a commercial SPICE-like circuit simulator as shown Fig. 6. This full circuit model includes the ESD generator, PCB and varistor and simulation result is shown in Fig. 7. The voltage is set to 1 kV and the discharge current is injected approximately 4 A into the trace of PCB (red line). The simulated data in Fig. 7 shows current flow of 3.4 A to ground through the varistor (blue line). Circuit or PCB designer can use this circuit model to characterize the ESD clamping performance at the early design phase.

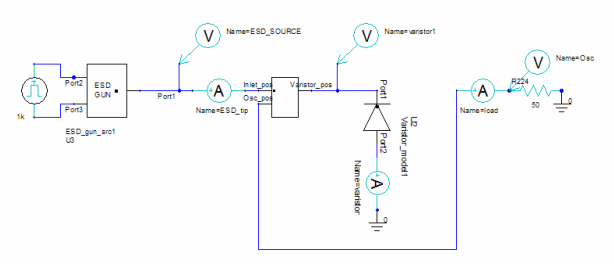


Fig. 6 Full circuit model of a PCB with the ESD generator and varistor

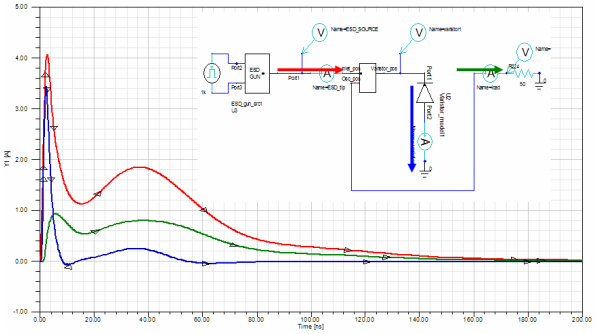


Fig. 7 Simulated ESD current waveform with the varistor

III. Experimental Verification

The discharge current injected by the ESD generator and clamping voltage across the varistor are measured to validate the proposed equivalent circuit model. The injected current and clamping voltage waveforms are measured using the test PCB with the varistor mounted shown in Fig. 3. The ESD generator is discharged in contact mode at 1 kV.

Fig. 8 shows the simulation result (red line) for ESD current waveform compared with the measurement result (blue line). The component values in the equivalent circuit model proposed in [3] was modified based on comparing the simulation result for the injected current with measurement result for many versions to achieve better match. As seen from Fig. 8, the first and second peak currents match well with the measured data.

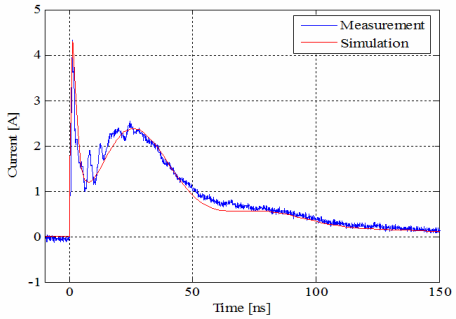
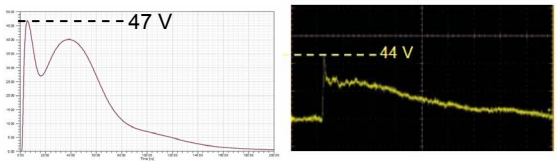


Fig. 8 ESD current waveform comparison

Fig. 9 shows a comparison result between the simulated and measured clamping voltage waveform across the varistor.

From the figure, we can see that the circuit model simulates the first peak voltage well. But we also can see that the magnitude of the second peak voltage is larger than the measurement result. The circuit model still needs to be improved to get better matched simulation result. The simulated voltage waveform was computed using the circuit model shown in Fig. 6.



(a) (b)

Fig. 9 Voltage waveform comparison: (a) simulated; (b) measured

IV. Applications

High-speed data interface technologies such as USB and HDMI used in modern electronic products are becoming more sensitive to ESD because these interface ports are subject to human contact. There are a number of protection devices available that can protect against ESD, but an amount of capacitance of the protection device can affect signal integrity of high-speed signals. There can be trade-off issues between the ESD clamping performance and signal integrity, with the ESD protection device in high-speed applications.

The ESD clamping performance and signal integrity can be characterized using a circuit model proposed in this paper. Fig. 10 shows an example of ESD protection circuit for USB signal interfaces. Eye diagrams of two different ESD protection devices with different capacitance values were simulated and compared with the USB2.0 mask. Comparing the eye diagrams shown in Fig. 11 demonstrates the signal degradation caused by the large capacitance value.

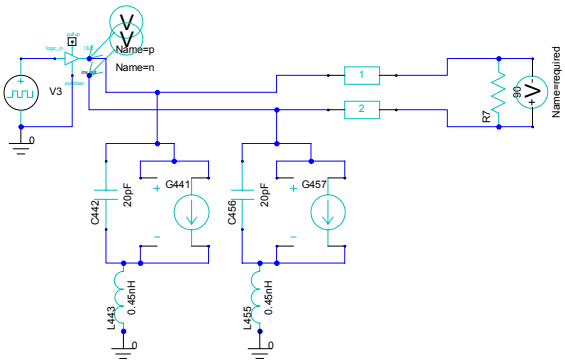
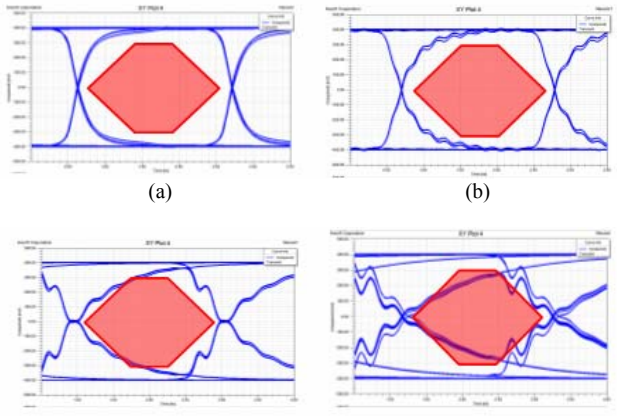


Fig. 10 Circuit model for signal integrity simulations with varistors



(a) (b) (c) (d)

Fig. 11 Simulated eye-diagram : (a) without varistor; (b) with 4 pF varistor; (c) with 20 pF varistor; (d) with 40 pF varistor

V. Conclusions

A simple and efficient circuit model for simulating ESD clamping performance in a SPICE-like circuit simulator is proposed. The proposed circuit model allows circuit or system designers to evaluate ESD characteristics of their PCB design quickly and at very little cost. This helps designers to improve electrical performance at the early design phase and reduce design cycle times in their product designs.

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