

A Class of Analog CMOS Circuits Based on the Square-Law Characteristic of an MOS Transistor in Saturation

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Abstract—A class of accurate analog CMOS circuits is presented which relies on the square-law characteristic of MOS transistors operating in the saturated region. This class of circuits includes voltage multipliers, current multipliers, linear $V-I$ convertors (LVIC's), linear $I-V$ convertors (LIVC's), current squaring circuits (CSC's), and current divider circuits (DIVC's). Typical for these circuits is an independent control of the sum as well as the difference between two gate-source voltages. As direct use is made of the basic device characteristics, only a small number of transistors is required in the presented circuits.

I. THE PRINCIPLE

RECENTLY several papers on analog MOS circuits have been published with transistors operating in the saturated region [1]–[3]. It will be shown here that these circuits belong to a class of circuits not only composed of linear $V-I$ convertors, but also of linear $I-V$ convertors and a large number of computational circuits in the current domain. Examples of such computational circuits are squaring circuits, divider circuits, and multiplier circuits. The basic principle on which these circuits rely will be explained at the hand of a basic subcircuit characterizing this class of circuits.

In this section we are concerned with the ideal relationships between the input and output signals of these circuits. The square-law behavior for the current-voltage relationship of the MOS transistor in saturation is assumed as

$$I_d = K(V_{gs} - V_t)^2 \quad (1)$$

Consider the circuit of Fig. 1, consisting of two identical MOS transistors $M1$ and $M2$. The gate-source voltage of $M1$ is equal to V_a and the gate-source voltage of $M2$ is equal to V_b . The sum of the gate-source voltages is kept constant via a voltage source V_2 . Using (1) we may write the circuit equations as

$$I_1 = K(V_a - V_t)^2 \quad (2)$$

$$I_2 = K(V_b - V_t)^2 \quad (3)$$

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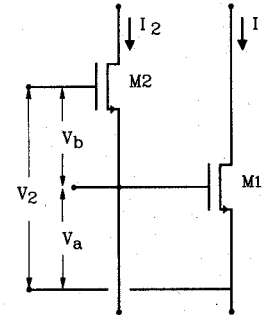


Fig. 1. The basic two-transistor circuit.

and

$$V_b = V_2 - V_a. \quad (4)$$

Using simple algebra we may write for the output current difference

$$I_1 - I_2 = K(V_2 - 2V_t)(V_a - V_b). \quad (5)$$

With (2)–(5), the sum of the output currents may be written as

$$I_1 + I_2 = \frac{1}{2}K(V_2 - 2V_t)^2 + \frac{(I_1 - I_2)^2}{2K(V_2 - 2V_t)^2}. \quad (6)$$

The basic two-transistor circuit of $M1$ and $M2$ is typical for the class of circuits to be considered. It exhibits a linear relationship between $I_1 - I_2$ and $V_a - V_b$ for constant V_2 . Section II-A describes a linear $V-I$ convertor based on this relationship. Moreover, as

$$V_a - V_b = V_2 - 2V_b = 2V_a - V_2 \quad (7)$$

$I_1 - I_2$ is also linear with V_a or with V_b , for constant V_2 . The current difference $I_1 - I_2$ and the sum $I_1 + I_2$ are independent variables if I_1 and I_2 are independent. Hence (6) may be considered to describe the current $I_1 + I_2$ as the sum of a constant current and a square function of the independent variable $I_1 - I_2$. In Section II-C it will be shown how this feature of the basic two-transistor circuit can be used to build a current squaring circuit.

In the next sections the basic two-transistor circuit of Fig. 1 is applied in a number of functional circuits.

II. THE BASIC FUNCTIONAL CIRCUITS

The essential underlying condition in the six functional basic circuits described in this section is the constant sum of two gate-source voltages, as explained in the previous section.

To simplify the expressions, a current-controlled biasing circuit (Fig. 2) is introduced which supplies the sum voltage V_2 . The relation between the control current I_0 and the voltage V_2 is given by

$$I_0 = \frac{1}{4} K (V_2 - 2V_t)^2 \quad (8)$$

under the condition $V_2 > 2V_t$. In the current domain, biasing of the functional circuits will be expressed in terms of I_0 , whereas in the voltage domain V_2 will be considered as the biasing parameter.

All transistors in the circuits described in this section have the same geometry.

A. The Linear V - I Convertor (LVIC)

Consider the circuit of Fig. 3. Assume that all transistors operate in saturation. In $M1$ and $M2$ the basic two-transistor circuit of Fig. 1 is recognized and (2)–(4) hold. An extra transistor $M3$ controls the current I_2 via the input voltage V_{in} . The gate-source voltage V_b of $M2$ will equal V_{in} . Substitution of (7) in (5) yields

$$I_1 - I_2 = K(V_2 - 2V_t)(V_2 - 2V_{in}). \quad (9)$$

For constant V_2 , the output current difference $I_1 - I_2$ is a linear function of V_{in} , and a linear V - I convertor (LVIC) is obtained.

Equation (9) is valid if all devices are in the ON state, operating in the saturated region. This requires for V_{in} :

$$V_t < V_{in} < (V_2 + V_t)/2 \quad (10)$$

while

$$V_2 > 2V_t. \quad (11)$$

B. The Linear I - V Convertor (LIVC)

Let us start again from the basic two-transistor circuit of Fig. 1. By connecting the drain of $M1$ to its gate, the circuit of Fig. 4 is obtained. The common node of $M1$ and $M2$ is now considered as input. An input current I_{in} flowing into the circuit causes a voltage V_{out} on this node as indicated in Fig. 4. Equations (2)–(4) hold again, and in terms of the symbols used in Fig. 1, the input current may be written as

$$I_{in} = I_1 - I_2 \quad (12)$$

and the output voltage as

$$V_{out} = V_a. \quad (13)$$

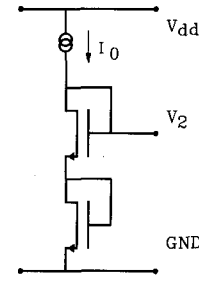


Fig. 2. The biasing circuit.

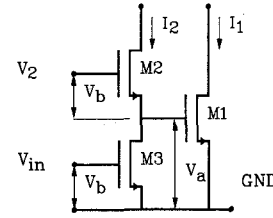


Fig. 3. The linear V - I convertor.

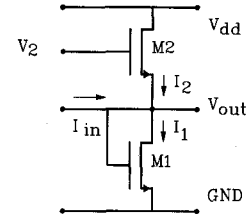


Fig. 4. The linear I - V convertor.

Substitution of (7), (12), and (13) in (5) yields

$$I_{in} = 2K(V_2 - 2V_t)(V_{out} - V_2/2). \quad (14)$$

Defining $V'_{out} = V_{out} - V_2/2$ yields

$$\frac{V'_{out}}{I_{in}} = \frac{1}{2K(V_2 - 2V_t)}. \quad (15)$$

This describes the behavior of a linear resistor of $1/(2K(V_2 - 2V_t)) \Omega$ connected between the input and a constant voltage $V_2/2$. The circuit performs as an I - V convertor.

In order for (15) to remain valid, all devices have to be in the ON state and operate in the saturation region. This requires

$$V_t < V_{out} < V_2 - V_t \quad (16)$$

and

$$2V_t < V_2 < V_{dd} - V_t. \quad (17)$$

C. The Current Squaring Circuit (CSC)

As has been mentioned in Section I, the two-transistor circuit of Fig. 1 provides an output sum current $I_1 + I_2$, which is a quadratic function of the difference $I_1 - I_2$, apart from a constant term. The current difference $I_1 - I_2$ was in (12) defined as an input current in the linear I - V

converter circuit (LIVC) (Fig. 4), with I_1 flowing in $M1$ and I_2 in $M2$.

By copying of I_1 via transistor $M3$ and adding it to current I_2 as shown in Fig. 5, the sum current $I_1 + I_2$ is available as output current I_{out} and

$$I_{out} = I_1 + I_2. \quad (18)$$

Substitution of (12) and (18) in (6) yields

$$I_{out} = \frac{1}{2}K(V_2 - 2V_t)^2 + \frac{I_{in}^2}{2K(V_2 - 2V_t)^2} \quad (19)$$

which describes a current squaring function. Using the bias circuit of Fig. 2 and by substitution of (8) in (19), a simpler expression is obtained:

$$I_{out} = 2I_0 + \frac{I_{in}^2}{8I_0}. \quad (20)$$

Biasing with a current has the additional advantage of making the transfer function (in first-order approximation) independent of process parameters and operating temperature.

In order to keep all devices in the ON state the input current must be restricted within the range

$$|I_{in}| < 4I_0. \quad (21)$$

D. The Divider Circuit (DIVC)

Equation (20) shows that if the bias current I_0 in Fig. 2 is considered as being an input current, the circuits of Figs. 2 and 5 behave as a divider circuit (DIVC). In that case, however, the term $2I_0$ has to be cancelled. This is done by subtracting two times the bias current from the output current. Now a circuit is obtained (Fig. 6) which may be used both as a current squaring circuit (CSC) and as a DIVC. Here the bias current input is considered as a second input current I_{in2} whereas the input current is now called I_{in1} . The relation between output and input currents now becomes

$$I_{out} = \frac{I_{in1}^2}{8I_{in2}}. \quad (22)$$

In order to remain a proper operation, the following relations between the input currents have to be valid:

$$|I_{in1}| < 4I_{in2} \quad (23)$$

and

$$I_{in2} > 0. \quad (24)$$

E. The Current Invertor (CI)

In this section a current invertor (CI) is described which can handle both positive and negative input currents. It also has a linear input resistance.

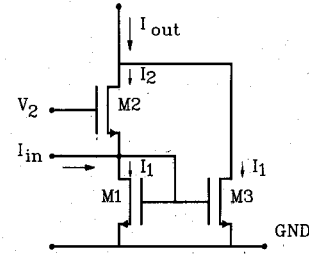


Fig. 5. The current-squaring circuit.

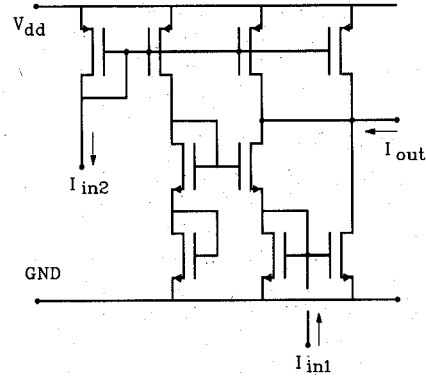


Fig. 6. The divider/squaring circuit.

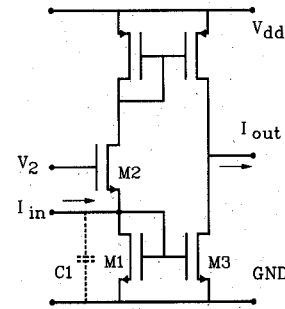


Fig. 7. The current invertor ($< I$).

Let us consider Fig. 7. In the subcircuit formed by $M1$ and $M2$, the LIVC described in Section II-B (Fig. 4) is recognized. The current I_2 is mirrored to the output node by means of a PMOS current mirror. $M3$ copies I_1 and subtracts this current from I_2 coming from the PMOS mirror. The output current I_{out} is now

$$I_{out} = I_2 - I_1 \quad (25)$$

and, together with (12), the input-output relation becomes

$$I_{out} = -I_{in}. \quad (26)$$

In order to remain a proper operation, the input current is restricted to the range

$$|I_{in}| < K(V_2 - 2V_t)^2 \quad (27)$$

or, if biased with the circuit of Fig. 2

$$|I_{in}| < 4I_0. \quad (28)$$

F. A Current-Domain Low-Pass Filter (CDLFP)

The linear input resistance of the inverter (CI) can be exploited for the realization of a current-domain low-pass filter (CDLFP). By adding a capacitor at the input of the circuit, as is shown in Fig. 7 by the dashed lines, the input impedance is made complex, but still linear. For low frequencies, the transfer is described by (26). As a function of frequency, however, the transfer function becomes

$$H(s) = I_{out}/I_{in} = -1/(1 + sRC) \quad (29)$$

with R according to (15) given by

$$R = 1/2K(V_2 - 2V_T). \quad (30)$$

This circuit can be used as a basic building block for filter implementations in the current domain.

III. MORE ELABORATE CIRCUITS

The basic functional circuits from Section II can be applied in more elaborate circuits. In this section a few examples are presented. They show the versatility of the principle described in Section I in general and of the basic functional circuits in Section II in particular.

A. A Four-Quadrant Analog Voltage Multiplier (4QAVM)

A two-quadrant analog voltage multiplier can be obtained using the linear voltage-controlled $V-I$ convertor circuit of Section II-A (Fig. 3) by duplicating the circuit and cross coupling the outputs. The four-quadrant analog voltage multiplier (4QAVM) is obtained by again duplicating this circuit and cross coupling the output currents. This circuit and its performance have been treated extensively in [1].

B. A Four-Quadrant Analog Current Multiplier (4QACM)

The CSC of Section II-C (Fig. 5) can be used to build a current multiplier in the following way. Take two of these circuits, both biased by the same voltage V_2 , and apply the following currents to the inputs of the CSC's:

$$I_{in1} = I_a + I_b \quad (31)$$

$$I_{in2} = I_a - I_b. \quad (32)$$

The output currents of these CSC's are calculated making use of (19). The output current of the total circuit (Fig. 8) is, by action of the current mirror, equal to the difference of the output currents of the CSC's and obeys the following expression:

$$I_{out} = \frac{2I_a I_b}{K(V_2 - 2V_T)^2}. \quad (33)$$

As both I_a and I_b may be positive as well as negative, the circuit shown in Fig. 8 represents a four-quadrant analog current multiplier (4QACM). The CI of Section II-E could

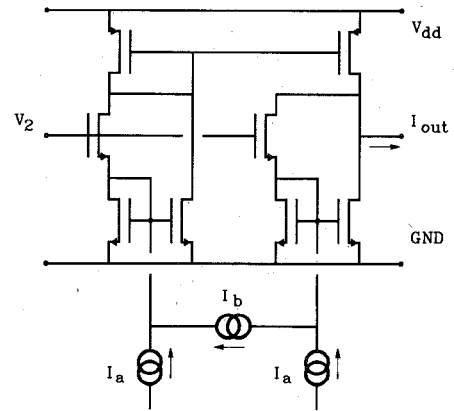


Fig. 8. The four-quadrant analog current multiplier.

be used to get duplicates of the currents I_a and I_b and to obtain the sum and difference of these currents according to (31) and (32). Again using the bias circuit of Fig. 2 to supply the voltage V_2 , (33) may be rewritten by substitution of (8) into

$$I_{out} = \frac{I_a I_b}{2I_0}. \quad (34)$$

Equation (34) shows that this compound circuit, besides as a current multiplier, also can be used as a current divider if I_0 is considered as an input current.

Here again the input currents are restricted to a maximum. Each CSC imposes a restriction according to (25). Substitution of (31) and (32) in (25) leads to two inequalities:

$$|I_a + I_b| < 4I_0$$

and

$$|I_a - I_b| < 4I_0$$

which is equivalent to

$$|I_a| + |I_b| < 4I_0. \quad (35)$$

C. A Floating Input Linear $V-I$ Convertor (FILVIC)

In Section II-A a three-transistor LVIC was described. A drawback of that circuit is that it does not have a floating input. The dc level of the input signal is simultaneously a bias voltage of the circuit. In this section, a circuit will be described with independent biasing and differential floating input. We will start from the well-known differential pair in Fig. 9, with a current mirror to provide a single-ended output current. The voltage-to-current conversion of this simple differential pair is

$$I_{out} = KV_{in} \sqrt{2I_t/K - V_{in}^2}. \quad (36)$$

A technique to achieve a LVIC starting from such a differential pair has been described in [2]. The key is a tail current I_t that obeys the function

$$I_t = I_0 + KV_{in}^2. \quad (37)$$

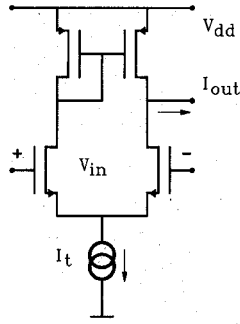


Fig. 9. A differential pair.

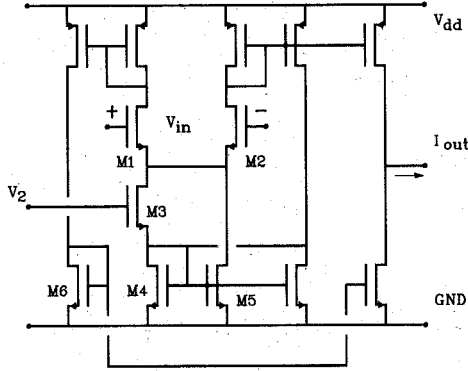


Fig. 10. A floating input LVIC.

Substitution of (37) in (36) results in the following expression for the output current:

$$I_{out} = K V_{in} \sqrt{2I_0/K}. \quad (38)$$

For realization of a LVIC following this approach, a voltage squaring circuit is required to perform the function of (37). This might be obtained by cascading a LVIC and the CSC of Section II-C (Fig. 5). The LVIC described in Section II-B, however, is not suitable because it has no floating input. The LVIC which we are designing just now would do the job much better. So anticipating its proper functioning and applying its output current to the CSC, the tail current is then supplied as required by (37).

Fig. 10 shows the complete circuit in which current mirrors have been added to obtain a single-ended output. In this configuration the output current can be written as

$$I_{out} = K(V_2 - 2V_t)V_{in}. \quad (39)$$

Here again the input voltage is restricted to

$$|V_{in}| < (V_2 - 2V_t) \quad (40)$$

in order to fulfill the conditions for operation in the saturation region. This circuit configuration is very similar to a simple single-stage CMOS op amp; only four extra transistors are required to linearize this stage. Moreover, as the tail current increases with increasing input voltage, the maximum output current is larger compared to the simple single-stage CMOS op amp. The maximum output current is

$$|I_{outmax}| = 2I_0 \quad (41)$$

which is reached for

$$|V_{in}| = V_2 - 2V_t. \quad (42)$$

Using two of these floating input LVIC (FILVIC) circuits with opposite input voltages V_{in} and $-V_{in}$ and bias voltages V_2 and V_2' , respectively, leads to the following expression for the sum of the output currents:

$$I_{sum} = K(V_2 - V_2')V_{in}. \quad (43)$$

This describes the operation of a 4QAVM.

Another use of this FILVIC circuit is a conversion from floating voltage input to purely differential voltage output on top of a fixed common-mode voltage. If the gate-source voltages of $M1$ and $M2$ are, respectively, V_a and V_b , then by simple deduction it can be shown that the gate-source voltages of $M3$ and $M6$ are equal to V_a and the gate-source voltages of $M4$ and $M5$ are equal to V_b . As $V_{in} = V_a - V_b$, the input voltage is copied between the gates of $M4$ and $M6$. As $V_a + V_b = V_2$, the common-mode voltage on these nodes is fixed and signal independent.

IV. HAND CALCULATIONS, SIMULATIONS, AND MEASUREMENTS

In this section the performance of the circuits presented in the preceding sections will be discussed. Analytical calculations, SPICE simulations, and measurements will be compared for the simple LVIC (Fig. 3). Measured results will also be shown of the more elaborated circuits of Section III.

A. Second-Order Effects

There are several second-order effects causing deviations from the ideal square-law behavior of (1). We will discuss these second-order effects as they apply to the performance of the simple LVIC of Section II-A.

Consider the circuit of Fig. 3 again. Assume a constant voltage V_2 applied to the gate of $M2$ and an input signal V_{in} , consisting of a sinusoidal signal superposed on a dc bias voltage V_{DC} , applied to the gate of $M3$. We define the effective dc gate voltages as

$$V_{2e} = V_2 - 2V_t \quad (44)$$

and

$$V_{DCe} = V_{DC} - V_t. \quad (45)$$

The input voltage V_{in} may now be written as

$$V_{in} = V_t + V_{DCe} + V_{AC} \sin(\omega t) \quad (46)$$

with V_{AC} being the magnitude of the sine wave.

The effect of mobility reduction, channel-length modulation, and mismatch between the transistors of the circuits will be considered. It will be shown that mobility reduction is the most important effect.

1. *Mobility Reduction*: Mobility reduction in an MOS transistor may be modeled by

$$\mu = \mu_0 / (1 + \theta(V_{gs} - V_t)) \quad (47)$$

where

μ_0 zero field mobility,
 θ $1/(d_{ox} \cdot E_{cr})$,
 d_{ox} oxide thickness, and
 E_{cr} critical field.

Under the assumption

$$\begin{aligned} & \theta^2 [V_{AC}(V_{2e} - 2V_{DCe}) - V_{AC}^2] \\ & \ll 1 + \theta V_{2e} + \theta^2 V_{DCe}(V_{2e} - V_{DCe}) \end{aligned} \quad (48)$$

the second- and third-order distortions may be calculated as

$$\begin{aligned} HD2 &= \frac{3}{2} \theta V_{AC} \\ & \times \frac{V_{2e} - 2V_{DCe}}{2V_{2e} - \theta [V_{2e}^2 - 6V_{2e}V_{DCe} + 6V_{DCe}^2 + 3V_{AC}^2/2]} \end{aligned} \quad (49)$$

$$\begin{aligned} HD3 &= \frac{1}{2} \theta V_{AC}^2 \\ & \times \frac{1}{2V_{2e} - \theta [V_{2e}^2 - 6V_{2e}V_{DCe} + 6V_{DCe}^2 + 3V_{AC}^2/2]} \end{aligned} \quad (50)$$

Although (49) and (50) give us insight into the dependence of the harmonic distortion on the various parameters of the circuit, more accurate numerical results are obtained using SPICE. Fig. 11 shows the hand-calculated, the simulated, and the measured second and third harmonic distortion of the circuit of Fig. 3 as a function of the magnitude of the sine wave V_{AC} . Fig. 12 shows the hand-calculated, the simulated, and the measured second and third harmonic distortion as a function of V_2 . Both figures are obtained using a 1-kHz sine wave. These figures show a good agreement between simulations and measurements and confirm the behavior of the dependence of the harmonic distortion on V_{AC} and V_2 as predicted by (49) and (50). Fig. 11 clearly shows a linear dependence of the second harmonic distortion on V_{AC} and a quadratic dependence of the third harmonic distortion on V_{AC} . The absolute value of the hand-calculated distortion tends to be higher than the measured and simulated distortion. This is due to approximation (48). Calculations without approximation (48) show a much closer agreement but do not yield simple expressions.

2. *Channel-Length Modulation*: Channel-length modulation causes the drain current to be dependent on the drain voltage. This will cause mainly second- and third-order distortion components. The distortion due to channel-

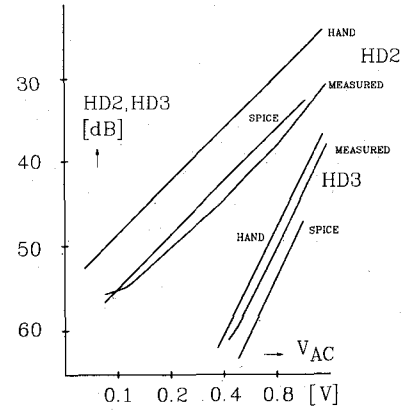


Fig. 11. The hand-calculated, measured, and simulated harmonic distortion of the LVIC of Fig. 3 as a function of V_{AC} , with $V_2 = 6.0$ V, $V_{DC} = 2.0$ V, $W = 40$ μ m, $L = 10$ μ m, and $f = 1$ kHz.

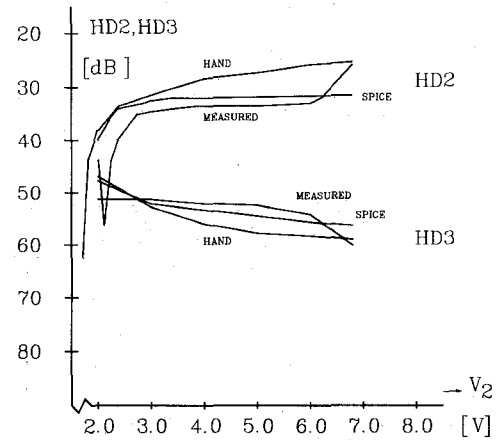


Fig. 12. The hand-calculated, measured, and simulated harmonic distortion of the LVIC of Fig. 3 as a function of V_2 , with $V_{AC} = 400$ mV, $V_{DC} = 0.8$ V, $W = 40$ μ m, and $L = 20$ μ m.

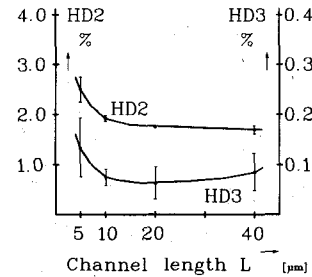


Fig. 13. The measured harmonic distortion of the LVIC of Fig. 3 as a function of the channel length L , with $V_2 = 5.0$ V, $V_{DC} = 1.0$ V, $V_{AC} = 312$ mV, and $W = 40$ μ m.

length modulation can be reduced by increasing the channel length of the devices. To determine the channel length above which no further significant improvement of the distortion can be achieved, simulations and measurements have been performed on the simple LVIC of Fig. 3. The results are shown in Fig. 13 and show that in our process a channel length of 10 μ m is sufficient to make the effect of channel-length reduction on the total harmonic distortion negligible with respect to the effect of mobility reduction.

3. *Mismatch*: Mismatch in threshold voltage does not give rise to distortion, it merely shifts the biasing.

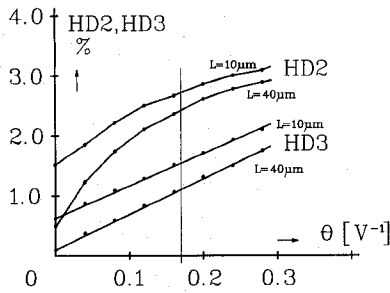


Fig. 14. SPICE simulation results of distortion of the LVIC of Fig. 3 as a function of the mobility reduction parameter θ , with $V_2 = 6.0$ V, $V_{DC} = 0.8$ V, $V_{AC} = 0.4$ V, $W = 40$ μm , and $f = 1$ kHz. The vertical line indicates the θ value used in the circuit simulations.

Mismatch in geometrical parameters can be evaluated via the K factors.

Consider the circuit of Fig. 3 and assume that the three transistors have the different values $K1$, $K2$, and $K3$ for the K factor. Let the relation between these factors be given by

$$K1 = K2 + dK2 \quad (51)$$

$$K3 = K2 + dK3 \quad (52)$$

where $dK1$ and $dK3$ are the deviations between $K1$ and $K2$ and between $K3$ and $K2$, respectively. It can be shown that this kind of mismatch gives rise to only second harmonic distortion. Applying a sine wave to the input of this circuit and using (44)–(46) we may obtain

$$HD2 = \frac{1}{4} V_{AC} \frac{dK1 + dK3}{K_2 V_{2e}} \quad (53)$$

In general this distortion level is much lower than the distortion caused by mobility reduction described by (49). By that, the SPICE simulations of Figs. 11 and 12 show a good agreement with measurements, although no mismatch has been included in the simulation.

From the previous results we may conclude that mobility reduction is the major cause of distortion in the LVIC of Fig. 3. To confirm this conclusion SPICE simulations have been performed to show the dependence of the second and third harmonic distortion of the LVIC on the mobility reduction parameter θ . Fig. 14 shows the results. At a channel length of $L = 10$ μm the predicted distortion becomes smaller if mobility reduction is diminished but not as much as an order of magnitude. This is because at this small channel length the channel-length modulation is no longer negligible. At a channel length of 40 μm , however, the predicted distortion drops an order of magnitude if mobility reduction is neglected. Since the mobility reduction is a process parameter, it is not a tool for the designer. The channel-length modulation, however, can be decreased by using long-channel devices. This makes mobility reduction the most fundamental cause of distortion in this circuit.

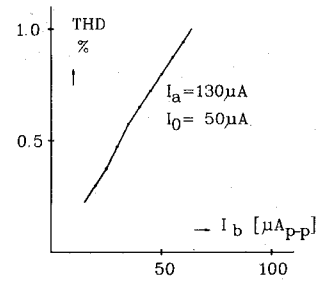


Fig. 15. The THD of the current multiplier as a function of I_b , with $I_a = 130$ μA , $I_0 = 50$ μA , and $f = 1$ kHz.

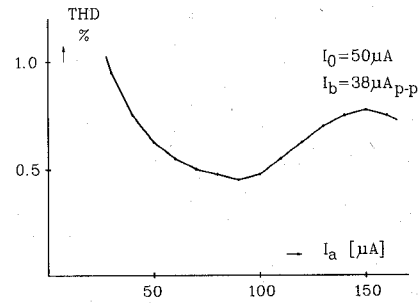


Fig. 16. The THD of the current multiplier as a function of I_a , with $I_b = 38$ μA_{p-p} , $I_0 = 50$ μA , and $f = 1$ kHz.

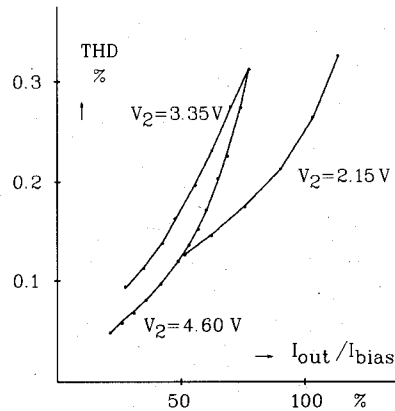


Fig. 17. The THD of the FILVIC (Fig. 10) as a function of I_{out}/I_{bias} , with $f = 1$ kHz.

B. Measured Distortion

The circuits discussed in Section III have been fabricated in the IC processing facility at the University of Twente using a retrograde twin-well CMOS process [4]. This process has isolated n-wells, and the circuits have been realized with p-channel transistors with sources connected to the wells. N-channel transistors have only been used as current mirrors.

Measured results of the four-quadrant voltage multiplier of Section III-A have been presented in [1]. Figs. 15 and 16 show the performance of the 4QACM; I_a is a dc current whereas I_b is a 1-kHz sine wave. In Fig. 15 the total harmonic distortion (THD) of the output signal is plotted against the magnitude of the sine wave with $I_a = 130$ μA and $I_0 = 50$ μA . In Fig. 16 the THD is shown versus the magnitude of the dc current with I_b being a 1-kHz sine wave of 38 μA_{p-p} .

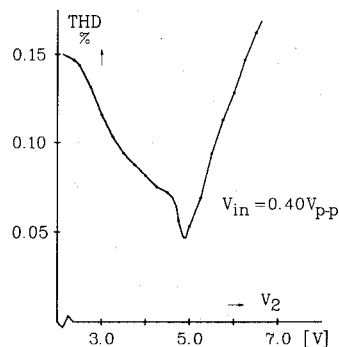


Fig. 18. The THD of the FILVIC (Fig. 10) as a function of V_2 , with $V_{in} = 0.4 V_{p-p}$ and $f = 1$ kHz.

Figs. 17 and 18 show the performance of the FILVIC. In Fig. 17 the THD is plotted against the magnitude of the input sine wave for various values of V_2 , and in Fig. 18 the THD is shown as a function of V_2 with V_{in} being a sine wave of $0.4 V_{p-p}$.

C. Measured Frequency Behavior

The -3 -dB bandwidth of all previously discussed circuits has been measured and, depending on bias current and the size of the devices, amounted to a few megahertz. As all internal nodes have a relatively low impedance, a much higher bandwidth was expected initially. The reason for this discrepancy was found in the well capacitance of the devices with floating n-well. PMOS transistors were used with sources connected to the well substrates in order to reduce the body effect. This well, however, has a large capacitance to substrate. For a transistor with $W = 40 \mu\text{m}$ and $L = 20 \mu\text{m}$ and a well-to-substrate voltage of 3 V this capacitance is 3.8 pF. In Fig. 1 this capacitance is situated at the source of transistor $M2$. This node was found to determine the dominant pole in every circuit. Transistor $M2$ with a gate-source voltage of 2.5 V has a g_m of about 10^{-4} [A/V]. The pole determined by this RC combination lies at a frequency of 4.2 MHz.

V. DISCUSSION

As mobility reduction has such a strong effect ($\theta = 0.17$ V^{-1} for the PMOST in our process) it is remarkable that the performance of the circuits belonging to this class of circuits is that good. The range where the I_d versus V_{gs} characteristic is really quadratic is rather restricted; in most processes this range does not exceed one decade. However, it lies in the nature of the described class of circuits that the signal is obtained from the difference between the drain currents of two devices both operating well in the quadratic range. It is this property that makes the dynamic range much larger than expected at first sight. Moreover, in many cases the circuit is symmetrical, cancelling every even-order harmonic distortion. Remaining even-order distortion is then caused by mismatch of the devices.

The frequency range of the presented circuits can be extended by an order of magnitude by disconnecting the well substrates from the sources of the devices and connecting all well substrates to the supply voltage. In this way the internal capacitances at these nodes are much smaller. Moreover, an NMOS device can be used which has a larger mobility and a lower mobility reduction effect. The effect on distortion of the body effect has to be investigated. Simulations of the circuits with NMOS devices in the core yield better results for the voltage multipliers. Measured data is not yet available.

The temperature dependence of the presented class of circuits can in many cases be minimized using the control terminal V_2 . In the current domain circuits this is done via the biasing circuit of Fig. 2. This makes the function of the circuits independent of temperature in first-order approximation.

VI. CONCLUSION

A new class of accurate analog CMOS circuits has been proposed which relies on the square-law characteristic of MOS transistors operating in the saturated region. The versatility of a set of basic circuits has been shown by a number of elaborate designs, i.e., analog voltage multipliers, a current squaring circuit, a current divider circuit, a current multiplier, and a linear $V-I$ convertor. The distortion level ranges between 0.1 and 1 percent. The distortion is predominately caused by mobility reduction and in our case may be improved by choosing the NMOS transistor as main device. This would also improve the speed of the circuits by an order of magnitude.

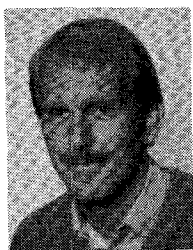
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