A Closed-Loop Selective Harmonic Compensation for Active Filters

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***Abstract*—This paper proposes a control algorithm for parallel active power filters, based on current-controlled pulsewidth-modulated converters, which allows precise compensation of selected harmonic currents produced by distorting loads. The approach is based on the measurement of line currents and performs the compensation of the selected harmonics using closed-loop synchronous frame controllers. Thanks to the closed-loop operation, full compensation of the desired harmonics is achieved even in the presence of a significant delay in the current control. Thanks to the selective approach, active filter interactions with possible dynamic components of the load are minimized. Moreover, the complexity of the synchronous frame controllers is overcome using equivalent stationary frame controllers. Experimental results confirm the theoretical expectations.**

***Index Terms*—Active filters, current control, harmonic filtering, pulsewidth-modulated power converters.**

I. Introduction

ACTIVE power filters (APFs) are powerful tools for the compensation not only of current harmonics produced by distorting loads, but also of reactive power and unbalance of nonlinear and fluctuating loads. Design and control of active filters have been deeply investigated in several papers [1]–[13], [17]–[25], covering different issues such as selection of compensation strategies, modulation techniques, electromagnetic interference (EMI) filters, and active filter topologies.

In conventional load current detection methods [1], [2], the generation of the active filter current reference is usually based on the harmonic detection of load currents, using the well-known instantaneous power theory [1], time-domain correlation techniques [5], etc. Using this solution, however, due to the time-domain approach, the delay of the APF current control causes incorrect compensation and unwanted remaining harmonics in the line currents. This effect is dramatic, especially when a fully digital control implementation is used, since the achievable performance may decrease below an acceptable level [6], [7]. For this reason, the high-performance hysteresis control [7] has been almost a mandatory choice for the achievement of a satisfactory harmonic compensation.

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Besides the current control delay, conventional supply current detection and load current detection methods [8] are also prone to instability when the load includes capacitive and/or resonant elements, as reported in many papers [8]–[13]. Instead, compensation strategies based only on voltage detection methods [10]–[12] are not affected by the aforementioned instability, but their application implies an increased interaction with the supply voltage harmonics.

In order to cope with the delay of the voltage-source inverter (VSI) current loop, it is possible to use a selective compensation achieved by means of bandpass filters on load currents whose frequency response has a leading phase equal to the delay introduced by the VSI current loop. For such purpose, several solutions have been proposed, such as low-pass filters in the harmonic reference frames [18], [19], discrete-Fourier-transform-based algorithms [17], and so on. With these solutions the delay of the VSI current control is theoretically compensated, but the approach, essentially based on feedforward open-loop compensation, is sensitive to parameter mismatches and relies on the ability to accurately predict the VSI current control performance.

In this paper, instead, a closed-loop compensation of selected line current harmonics is proposed. As in any selective approach, it is assumed that the harmonics produced by distorting loads are *slowly varying* and, thus, also the active filter control can be realized so as to perform only a *slow*, but very precise, harmonic compensation. This concept has been applied using a closed-loop regulation of line current harmonics which includes a synchronous reference frame controller for each harmonic (both for the positive-sequence and negative-sequence components) and uses the detection of line currents instead of load currents. A related approach applied to hybrid shunt filters can be found in [21]–[23], where only specific negative-sequence harmonics (i.e., the 5th) and positive-sequence harmonics (i.e., the 7th) are considered.

The proposed solution, which is particularly suited for a fully digital implementation, presents the following advantages.

- The control is selective for the harmonic compensation, giving numerous benefits, since the filter rating and bandwidth requirements can be strongly reduced.
- The control is insensitive to the delay of the VSI current control and each selected harmonic can be completely eliminated (almost 100% compensation) because of the closed-loop operation; moreover, the control is not sensitive to parameter mismatches.
- Oscillations and interactions, which may occur between the active filter and load [8]–[13] due to presence of

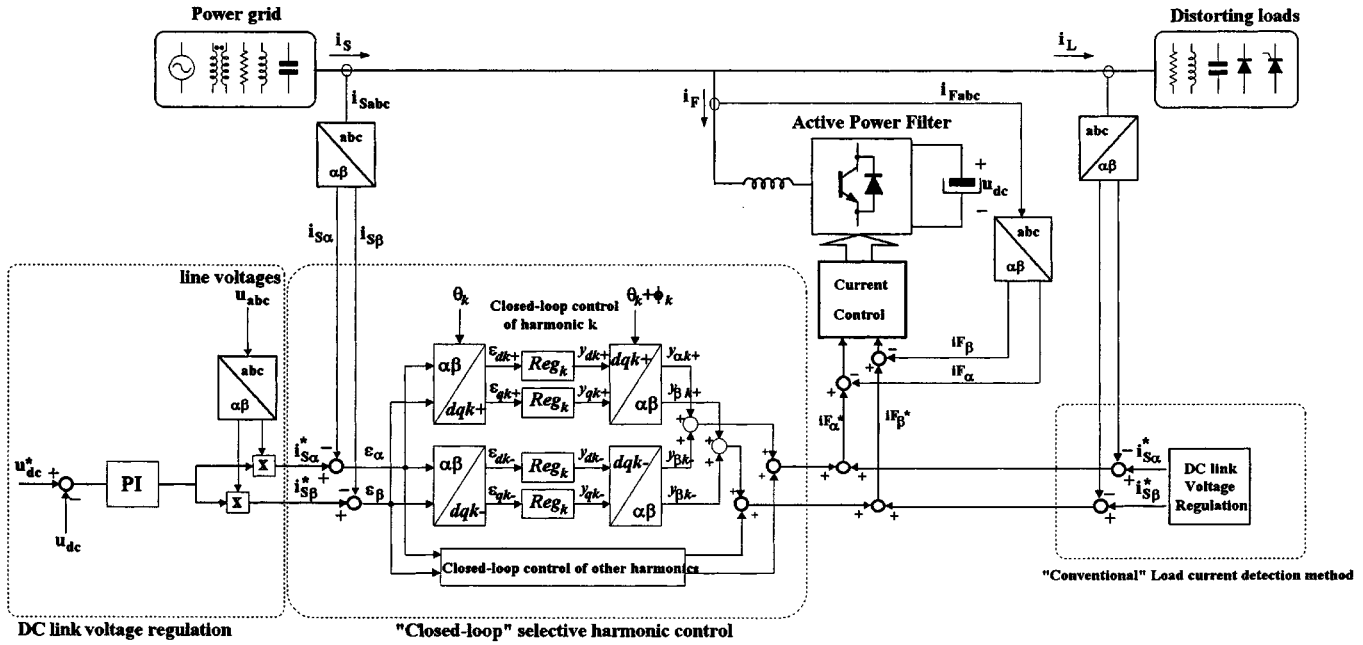

Fig. 1. Active filter control (left side) suppressing particular harmonics using closed-loop synchronous frame controllers.

capacitive or resonant component in the load impedance, are minimized.

In the practical digital signal processor (DSP) implementation, the complexity traditionally associated to synchronous frame controllers has been overcome by using equivalent stationary frame controllers. The equivalency is obtained extending the approach suggested earlier in [14] and then in [15] and [16].

II. Proposed Selective Compensation

The block diagram of the compensation strategy is outlined in Fig. 1 and in Fig. 2(a), where the three-phase system is assumed to be without neutral wire, so that all three-phase quantities are expressed in α–β coordinates; note, however, that the forthcoming description can be easily extended also to three-phase four-wire systems. Following the scheme of Fig. 1, line current references ($i^*_{S\alpha}$, $i^*_{S\beta}$) are obtained by multiplication of (possibly filtered) line voltages with the output of the dc-link voltage regulator. Then, a selective closed loop control on line currents is realized, so that the proposed solution belongs to the so-called supply current detection methods [8]. Thus, line current errors $\vec{\varepsilon}_{\alpha\beta}$ ($\vec{\varepsilon}_{\alpha\beta} = \varepsilon_\alpha + j\varepsilon_\beta$) in ($\alpha\beta$) coordinates are firstly converted into synchronous reference frame quantities $\vec{\varepsilon}_{k+}$ ($\vec{\varepsilon}_{k+} = \varepsilon_{dk+} + j\varepsilon_{qk+}$), $\vec{\varepsilon}_{k-}$ ($\vec{\varepsilon}_{k-} = \varepsilon_{dk-} + j\varepsilon_{qk-}$) using both positive-sequence ($dqk+$) and negative-sequence transformations ($dqk-$) rotating at angular frequency $\theta_k = k\omega_S$ (i.e., $\vec{\varepsilon}_{k+} = e^{j\theta_k}\vec{\varepsilon}_{\alpha\beta}$, $\vec{\varepsilon}_{k-} = e^{-j\theta_k}\vec{\varepsilon}_{\alpha\beta}$) where k is the order of the generic harmonic to be compensated and ω_S is line angular frequency. All synchronous reference frame errors (ε_{dk+}, ε_{qk+}, ε_{dk-}, ε_{qk-}) are then compensated by regulators Reg_k, which ensure zero steady-state errors for each harmonic component. The output of each regulator (y_{dk+}, y_{qk+}, y_{dk-}, y_{qk-}) is then converted back to the stationary reference frames, possibly adding a leading angle ϕ_k which compensates for the delay of the remaining process. The current references ($i^*_{F\alpha}$, $i^*_{F\beta}$) for the active filter current control are finally obtained by adding together all the contributions of closed-loop regulators for the selected harmonics. The APF current control is kept outside the synchronous reference frame controller (unlike [21]–[23]) for overcurrent protection purposes.

Note that, although the proposed algorithm is suited mainly for loads that do not fluctuate very rapidly, it can also be extended to fast varying loads when used in addition to what I will refer to as conventional load current detection method [8], shown in the right side of Fig. 1. In this way, the conventional control path acts as a feedforward in the control loop while the proposed solution corrects only the remaining errors. This combined approach allows fast dynamic response and precise harmonic tracking in steady state at the expense of the loss of harmonic selectivity and of an increased interaction with the load dynamics.

The block diagram shown in Fig. 1 represents only a general solution which ensures compensation of selected harmonics independently of any hypothesis on load symmetry. For specific loads, such as diode or thyristor rectifiers, simplifications can be adopted [22] since, for example, the 5th harmonic has only negative-sequence components and the 7th harmonic has only positive components. Moreover, both harmonics derive from the sixth harmonic in the dq fundamental reference frame, so that only one regulator in the dq fundamental positive-sequence reference frame could be used for both harmonics. Such simplifications, that are not suited for generic applications to distribution lines, are not considered here.

Even for the generic case, some simplifications of the theoretical scheme of Fig. 2(a) are possible. Firstly, the compensation of both positive sequence and negative sequence harmonic components for a generic harmonic k is equivalent to the synchronous demodulator of the $\alpha\beta$ components, shown in Fig. 2(b), as long as all regulators Reg_k in Fig. 2(a) and (b)

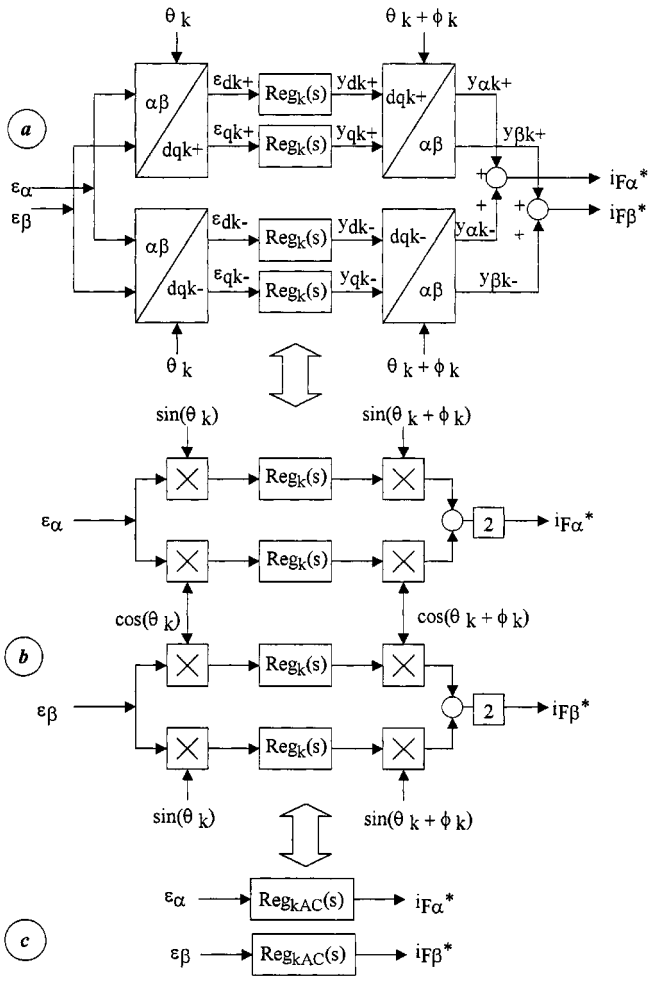

Fig. 2. Review of equivalency between stationary and reference frame controllers.

have the same transfer function. Secondly, even the scheme of Fig. 2(b) can be further simplified when implemented in DSPs since it is equivalent [15], [16] to the scheme of Fig. 2(c) with stationary frame regulators Reg_{kAC}

$$\begin{aligned} &Reg_{kAC}(s) \\ &\quad = \cos\phi_k[Reg_k(s - jk\omega_s) + Reg_k(s + jk\omega_s)] \\ &\qquad + j\sin\phi_k[Reg_k(s - jk\omega_s) - Reg_k(s + jk\omega_s)]. \end{aligned} \quad (1)$$

The advantage of this transformation in DSP implementation is that the resultant controller requires less signal processing. The theoretical scheme of Fig. 2(a) and (b) is, however, useful for deriving criteria for designing regulators Reg_k, as discussed hereafter.

III. Design Criteria

A. Design Criteria for Regulator Parameters

Different regulator structures can be used. A simple, but effective, choice is a simple integrator with finite dc gain, i.e.,

$$Reg_k(s) = \frac{K_{Ik}T_k}{1 + sT_k} \quad (2)$$

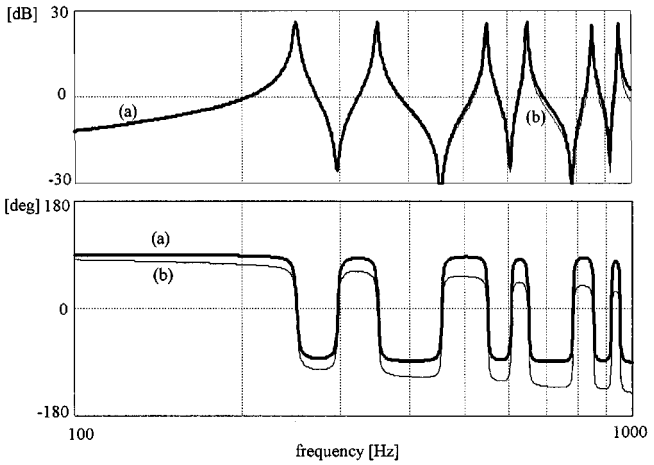

Fig. 3. *(a):* Frequency response of regulators Reg_k ($k = 5, 7, 11, 13, 17, 19$) using $n_{pk} = 0.5$, $A_k = 0.05$, and ϕ_0. *(b):* Open-loop gain which includes the delay of VSI current control.

where T_k is representing the effect of the finite integral gain in dc and K_{Ik} is designed based on the bandwidth specification. With this choice, integrator gain K_{Ik} can be designed as

$$K_{Ik} = \frac{2.2}{n_{pk}T_S} \quad (3)$$

where $(n_{pk}T_S)$ is desired response time (evaluated between 10%–90% of a step response) for the generic harmonic k and n_{pk} is the number of supply periods T_S. Instead, the pole time constant T_k is simply given by

$$T_k = \frac{1}{K_{Ik}A_k} \quad (4)$$

where A_k is the desired attenuation of the k harmonic, which directly determines the loop gain at frequency k. Of course, similar considerations can be done for more complex regulators, if needed, although the choice of (2) allows a straightforward design of harmonic regulators once the desired speed of response (for example in terms of n_{pk}) and the desired attenuation A_k have been specified. Finally, the leading angle ϕ_k can be set equal to the delay at frequency k of the transfer function between the active filter references and filter output currents. Whatever the choice, stability analysis of the closed-loop systems is needed, especially in the presence of a high speed of response where the interaction between different harmonic filters is high.

The module and the phase diagram of the resulting transfer function using $n_{pk} = 0.5$, $A_k = 0.05$, $\phi_k = 0$ and compensating the 5th, 7th, 11th, 13th, 17th, and 19th harmonics are reported in Fig. 3. We note that the gain of the regulators at the selected frequencies is, of course, 20 (i.e., $1/A_k$) while it is attenuated outside these frequencies. The open-loop gain, assuming that the VSI current control is simply modeled as a first-order pole with a delay (τ_{delay}) equal to 200 μs, is reported in the trace *(b)* of Fig. 3. Note that the system is always stable, although the phase margin decreases for high order harmonics. The effect of changing the speed of response of the active filter is reported in Fig. 4, where trace *(a)* refers to $n_{pk} = 0.25$ and trace *(b)* to $n_{pk} = 1$. It is evident that the lower the transient response, the

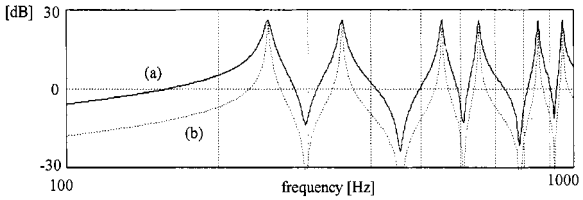

Fig. 4. Frequency response of regulators Reg_k ($k = 5, 7, 11, 13, 17, 19$) using $A_k = 0.05$, $\phi_k = 0$, and *(a):* $n_{pk} = 0.25$ or *(b):* $n_{pk} = 1.00$.

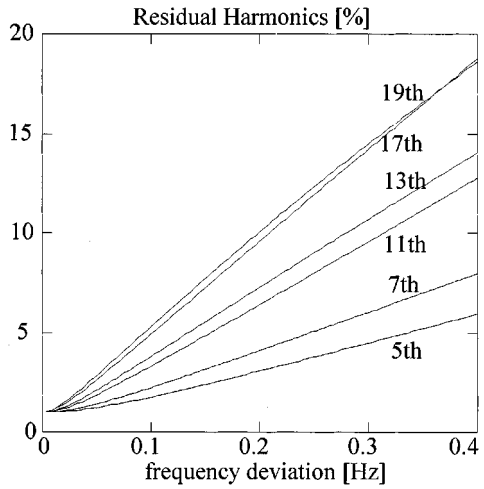

Fig. 5. Residual harmonics (%) in the line currents in presence of line-frequency deviation using $A_k = 0.01$ and $n_{pk} = 0.5$.

more selective is the active filter compensation which requires narrower passband filters.

The proposed control is, of course, sensitive to supply frequency variations due to the presence of narrow passband filters as reported in Fig. 5. As expected, the compensation performance decreases in presence of supply frequency deviation. For example, using half-cycle response ($n_{pk} = 0.5$) the desired attenuation moves from the nominal value, which has been set to 1% ($A_k = 0.01$) in this case, to almost 6% for the 5th harmonics and 18% for the 19th for a frequency deviation equal to 0.4 Hz. Even if such performance is still very good for active filter applications, a phase-locked loop (PLL) that precisely tracks supply-frequency variations is advisable in practical implementations.

B. Interaction with the Supply Grid

The speed of response of the proposed compensation strategy is related not only to the time-varying behavior of the distorting loads but also to the possible presence of capacitors or resonant elements in the compensated load. We recall [8]–[13], in fact, that conventional supply current detection and load current detection methods [8] are prone to give unstable operation in the presence of capacitive or resonant components at the load side, even if very small. With our approach, instead, it is possible to reduce this interaction at the expense of a slower dynamic response. As an example, Fig. 6 reports the open-loop gain of the system using conventional load current detection [trace *(a1)*] and the proposed selective control based on line current detection [trace *(b)*]. The stability analysis is carried out, as depicted in Fig. 7, assuming that the supply network is represented by an internal voltage e_s with a series impedance Z_s, the active filter by a current generator i_F driven (with a delay τ_{delay}) by a current reference i_F*. Instead, the load is represented by a Norton equivalent circuit, where the current generator indicates the purely distorting load and impedance Z_L the passive components of the load. Including a capacitive component in the load impedance, even if quite small (0.05 pu), Fig. 6 [trace *(a1)*] shows that the conventional control strategy, which tries to impose harmonics opposite to those of the load, is inherently unstable at frequencies closed to the oscillation frequency between the capacitive component of the load and the inductive component of the line. Indeed, the active damping control function [8], [24], [25], which means that a term proportional to the line voltage harmonics, beside the one already present in Fig. 1, is added to the active filter reference, can improve the stability margin of the system. However, it does not always solve the interaction problem, as highlighted in the trace *(a2)* of Fig. 6, which represents the load current detection method with a damping equivalence conductance of 4 pu at the harmonic frequencies. Note that, in these conditions, the system is still unstable.

Instead, in this example, the proposed approach is stable, as shown by the Bode diagram of Fig. 6 [trace *(b)*], since the loop

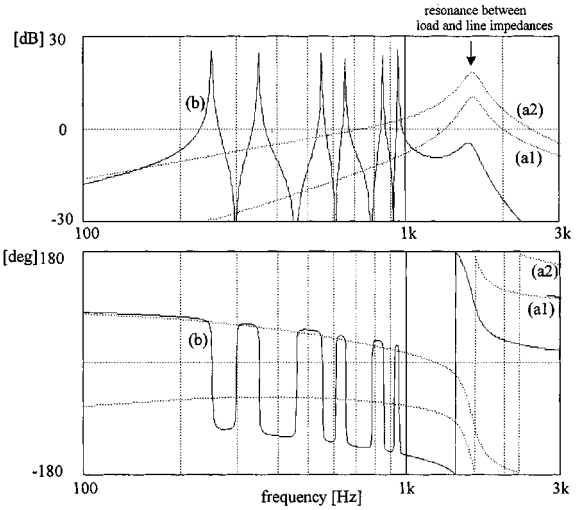

Fig. 6. Open-loop gain with $Z_s = R_s + sL_s$, $Y_L = G_L + sC_L$; $L_s = 0.02$ pu, $L_s/R_s = 5$, $C_L = 0.05$ pu, $G_L = 0.2$ pu, $\tau_{\text{delay}} = 200$ μs and *(a1):* conventional load current detection without active damping, *(a2):*: conventional load current detection with active damping ($G_{eq} = 4$ pu). *(b):*Proposed selective control based on line current detection ($A_k = 0.05$, $n_{pk} = 0.5$, and $\phi_k = 0$).

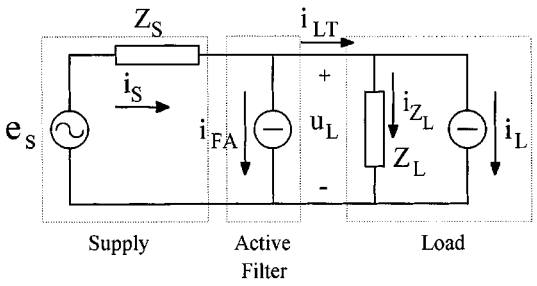

Fig. 7. Simplified configuration of a parallel active filter compensating loads with a generic impedance Z_L.

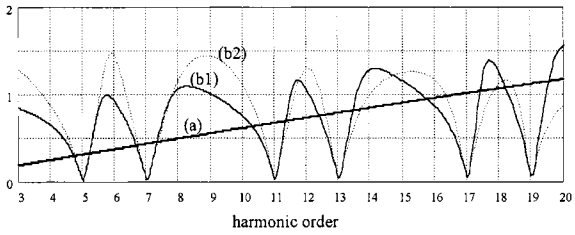

Fig. 8. Module of the transfer function between load current and line current harmonics using *(a):* load current detection method [see (5)], *(b):* proposed solution [see (6)] with Reg_k (k = 5, 7, 11, 13, 17, 19) using $A_k = 0.05$, $n_{pk} = 0.25$ and (b1) $\phi_k = 0$ or *(b2):* $\phi_k = k\omega_s\tau_{\rm delay}$. ($\tau_{\rm delay} = 200\ \mu$s).

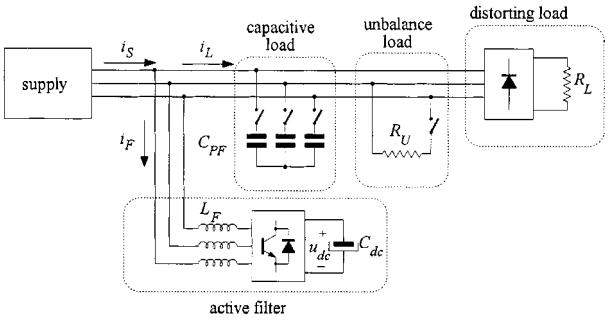

Fig. 9. Scheme of the experimental setup.

gain is strongly attenuated outside of the selected frequencies. From Fig. 6, it is easy to understand that the stability condition can be ensured as long as all the compensated harmonics are below the resonance frequency between the line and load impedance. Instead, if such resonance falls within the selected frequencies, instability conditions may still appear. For such cases, the maximum harmonic order to be compensated must be limited to the value which is not going to cause unstable operations. Moreover, the more selective the active filter compensation, the larger is the phase margin of the system in presence of line and load parameter uncertainties. Therefore, the design of parameter n_{pk} comes from a tradeoff between the speed of response, the harmonic selectivity, and the interaction with the supply grid. We have seen experimentally that values between 0.5–1 give good results.

C. Comparison with Load Current Detection Method

In order to highlight the properties of the proposed solution, a comparison with the so-called load current detection method, shown also in Fig. 1, is reported in terms of transfer function between the load current harmonics and the line current harmonics. For such purpose, the scheme of Fig. 7 can be used [3]; in order to highlight the effect of the VSI delay, the passive impedance at the load side is now neglected ($Y_L = 0$). Thus, for the load current detection method the aforementioned transfer function is

$$\frac{I_{Sk}}{I_{Lk}}(s) = 1 - e^{-s\tau_{\rm delay}} \tag{5}$$

while for the proposed solution is

$$\frac{I_{Sk}}{I_{Lk}}(s) = \frac{1}{1+GH(s)} \tag{6}$$

TABLE I
CON VERTER AND CONTROL PARAMETERS

DC Link Voltage	450 V
Filter Inductor L_F	1.8 mH
Switching Frequency f_{sw}	10 kHz (unless specified)
Power factor Correction Capacitor C_{PF}	20 μF
Line voltage (phase-to-phase)	220 V_{rms}
Nominal Load Power	5 kVA
Selected frequencies (k)	1st,5th,7th,11th,13th,17th,19th
Attenuation for each selected harmonic	0.005 (for all selected k)
Response time (number of line periods)	1 (for all selected k)
Leading angle ϕ_k	$k\omega_S 2/f_{sw}$(unless specified)

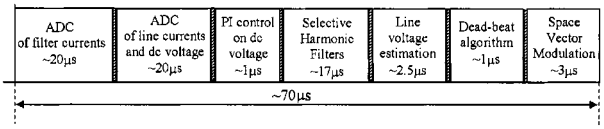

Fig. 10. Timing of the proposed algorithm using the ADSP21020 and ADMC200.

where $GH(s)$ is the open-loop gain shown in Figs. 3 and 4. The results are also reported in Fig. 8, where both transfer functions are depicted. We note that, due to the feedforward action, the conventional load current detection method is able to compensate only part of the load current distortion, e.g., only 69% of the 5th harmonic component, 54% of the 7th harmonics (when $\tau_{\rm delay} = 200\ \mu$s), and even worse for higher order harmonics. Instead, the proposed solution imposes a high open-loop gain at selected frequencies, ensuring a high rejection of any disturbance at those frequencies and, therefore, a good compensation for the selected harmonics, as highlighted also in Fig. 8.

D. Equivalence in the Stationary Reference Frame

Using transformation (1), regulators Reg_k given in (2) can be expressed in the stationary reference frame as

$$Reg_{k\rm AC}(s) = K_{Ik}T_k\left(2\frac{\xi_k}{\omega_{ok}}\frac{s+\dfrac{1}{T_k}-\dfrac{\sin(\phi_k)}{\cos(\phi_k)}k\omega_S}{\left(\dfrac{s}{\omega_{ok}}\right)^2+2\dfrac{\xi_k}{\omega_{ok}}s+1}\cos(\phi_k)\right) \tag{7}$$

where

$$\omega_{ok} = \sqrt{(k\omega_S)^2 + 1/T_k^2}$$
$$\xi_k = \frac{1}{\omega_{ok}T_k}. \tag{8}$$

Note that (7) is a *simple second-order passband filter* [15], [16] where the gain at the center angular frequency $k\omega_S$ is given by $K_{Ik}T_k$. The implementation on DSP requires the discretization of (7) into a difference equation. Using a first-order-hold (FOH) method [26], the transfer function (7) becomes

$$Reg_{k\rm AC}(z) = \frac{b_{0k}+b_{1k}z^{-1}+b_{2k}z^{-2}}{1+a_{1k}z^{-1}+a_{2k}z^{-2}} \tag{9}$$

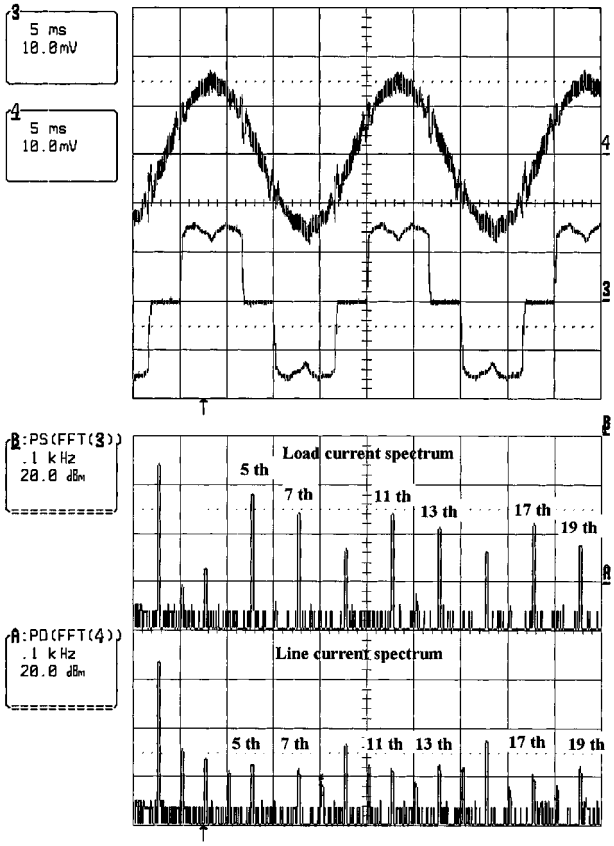

Fig. 11. Line current i_S (5 A/div) and load current i_L (5 A/div) waveforms (top) and their spectra (bottom) using the proposed solution ($f_{sw} = 10$ kHz).

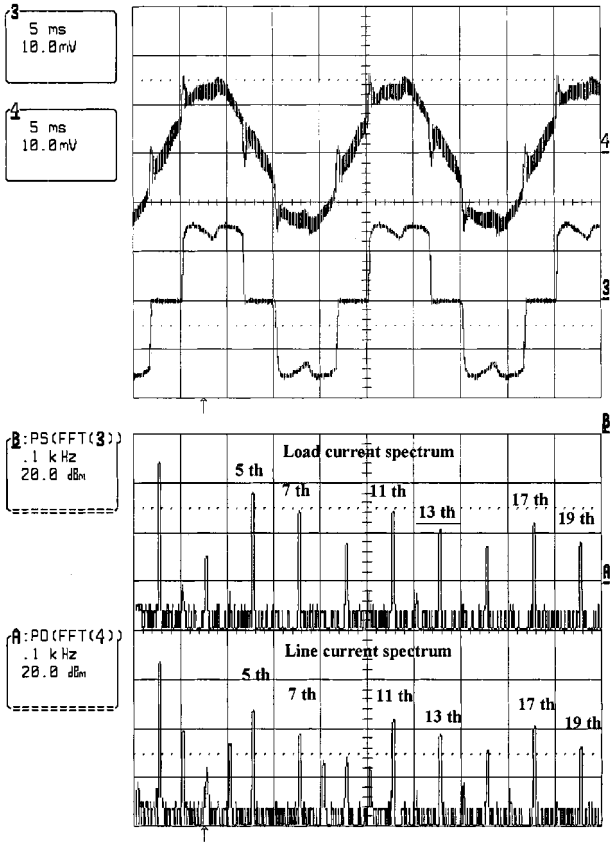

Fig. 12. Line current i_S (5 A/div) and load current i_L (5 A/div) waveforms (top) and their spectra (bottom) using conventional solutions ($f_{sw} = 10$ kHz).

where filter coefficients are derived from the FOH discretization method [26]. Finally, due to the inherent integral action at the selected harmonics, an *anti-windup protection* algorithm is necessary. This has been easily implemented saturating the output of each second-order filter (and, thus, also its internal state variable) to the maximum compensation level foreseen at the design stage.

IV. Experimental Results

The system of Fig. 1 has been experimentally tested using the configuration shown in Fig. 9 and the parameters of Table I. As far as the VSI current control is concerned, the deadbeat algorithm [27] has been chosen because it gives the highest speed of response among the digital controllers and thus gives also the best performance for a fully digital implementation of conventional techniques. Moreover with the deadbeat algorithm line voltages have been estimated avoiding their sensing. Finally, a simple proportional–integral (PI) control has been used for the dc-link voltage regulation, as depicted in Fig. 1, designed with 10-Hz bandwidth and 60° phase margin.

The proposed compensation strategy has been practically implemented by means of a floating-point 33-MHz DSP (ADSP21020) and the ADMC200 motion control board. The timing of the algorithm is reported in Fig. 10. Note that, beyond the ADC conversions, space-vector modulation (SVM) routine, and deadbeat and line voltage estimation algorithms, the control of each selective harmonic (with the above-mentioned anti-windup protection) takes less than 2.5 μs, even if implemented using a *nonoptimized* assembly code. This allows the compensation of a large number of harmonics.

The first verification was done on the harmonic compensation of an uncontrolled rectifier in steady-state conditions. Fig. 11 shows line current i_S and load current i_L with their corresponding spectra. As theoretically foreseen, the selected frequencies have been fully compensated and all of them are 40 dB below the fundamental component, close to the noise level of the experimental setup. Instead, Fig. 12 shows the results obtained using the conventional load current detection method where the effect of the two-cycle delay of the deadbeat control is evident and causes only a small attenuation of the desired harmonics. It is worth noting that the residual harmonic distortion in Fig. 12 is mainly due to the delay of the current control and not due to inverter saturation since the di/dt capability of the inverter could be able to perform the required compensation. Fig. 13(a) reports the comparison between these two conditions, highlighting the great potentiality of the proposed approach in terms of harmonic compensation. Moreover, Fig. 13(b) reports the same experiment, but using a switching frequency of 5 kHz instead of 10 kHz, emulating a high-power application. In this way, the insensitivity of the proposed approach to the VSI current control delay is clearly demonstrated. It is quite impressive to see that, in spite of a 5-kHz switching, the system is still able to achieve more than 20-dB attenuation on selected harmonics up to 1 kHz. Finally,

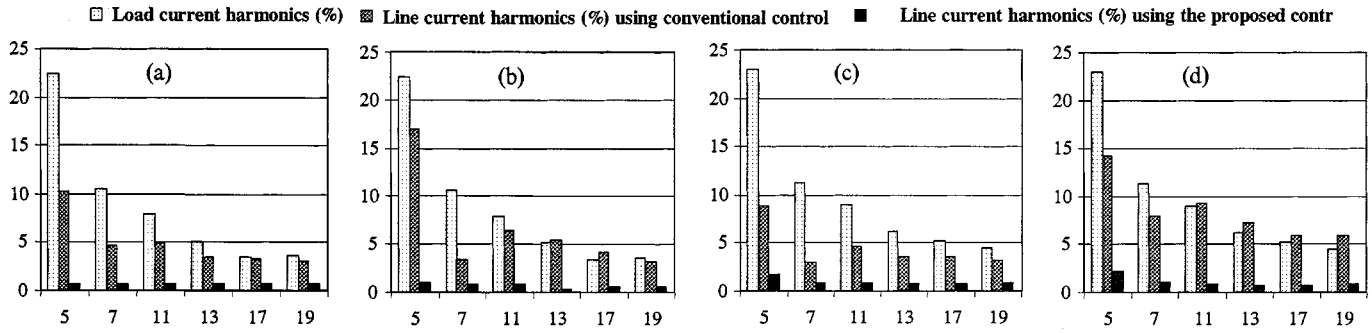

Fig. 13. Comparison between the proposed and conventional solutions (all harmonics are relative to the fundamental component). (a) Using $f_{sw} = 10$ kHz. (b) Using $f_{sw} = 5$ kHz with an uncontrolled rectifier. (c) Using $f_{sw} = 10$ kHz. (d) Using $f_{sw} = 5$ kHz with a thyristor rectifier ($\alpha = 40°$) as the distorting load.

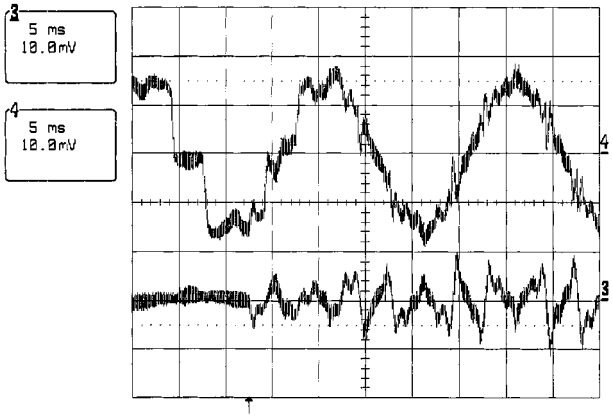

Fig. 14. Transient response following the turn-on of the active filter compensation (at the instant shown by the trigger) with $\phi_k = 0$. Top: line current (5 A/div); bottom: active filter current (5 A/div).

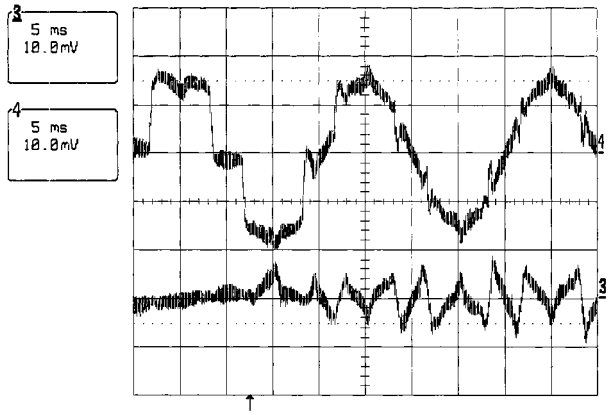

Fig. 15. Transient response following the turn-on of the active filter compensation (at the instant shown by the trigger) with $\phi_k = k\omega_S\tau_{\text{delay}}$. Top: line current (5 A/div); bottom: active filter current (5 A/div).

the same experiment was also tested using a thyristor rectifier ($\alpha = 40°$) instead of a diode rectifier. As shown in Fig. 13(c) and (d), the proposed approach overwhelms conventional solutions, especially with highly distorting loads.

In order to test the dynamic properties of the proposed compensation, Fig. 14 shows the transient following the turn-on of the active filter compensation when the leading angle ϕ_k has been set to zero. We note that low-order harmonics settle in around one line cycle, while some higher order harmonics are still in transient conditions. This result is in agreement with Fig. 3, which shows a small phase margin for high-order harmonics. The phase margin can be improved by adding a leading angle ϕ_k which compensates for the two-cycle delay of the deadbeat algorithm (i.e., $\phi_k = k\omega_S\tau_{\text{delay}}$). In fact, the results, reported in Fig. 15, show that in around one line cycle all selected harmonic components are fully compensated.

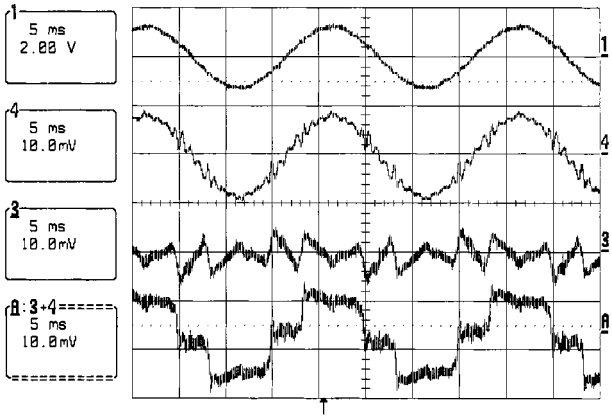

Fig. 16. Active filter behavior with capacitor C_{PF} inserted using the proposed solution. From top to bottom: line voltage (400 V/div), line current (10 A/div), active filter current (10 A/div), and load current (10 A/div).

Fig. 16 shows the active filter behavior when capacitors C_{PF} (shown in Fig. 9) have been inserted. We note that the active filter is able to perform the desired compensation, while in the same conditions conventional compensation strategies lead to unstable conditions as shown in Fig. 17. The oscillations occur around the 26th harmonic that is the frequency closed to the resonance between the capacitor C_{PF} and the line impedance. In order to highlight the limitation of the proposed approach, the capacitor has been increased so as to cause a resonance condition down to the 17th harmonic. In this case, both methods give unstable operations, as predicted by the analysis of Section III-B.

Finally, we have verified the compensation of load reactive power and unbalance, which is possible since also the fundamental component is among the selected frequencies. Fig. 18 shows the load current and the line currents in presence of a distorting and unbalanced load. It is worth noting that the active filter is able to provide both harmonic, reactive power, and unbalance compensation.

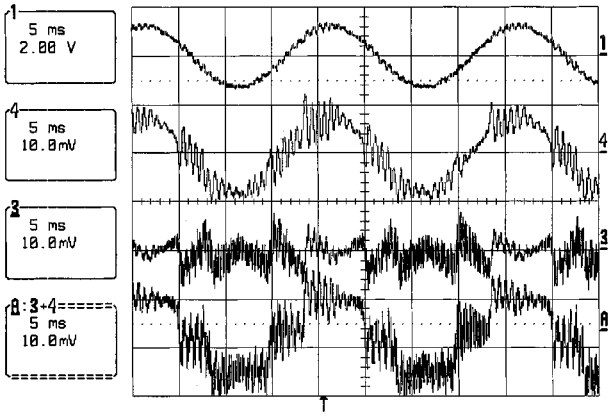

Fig. 17. Active filter behavior with capacitor C_{PF} inserted using conventional solution. From top to bottom: line voltage (400 V/div), line current (10 A/div), active filter current (10 A/div), and load current (10 A/div).

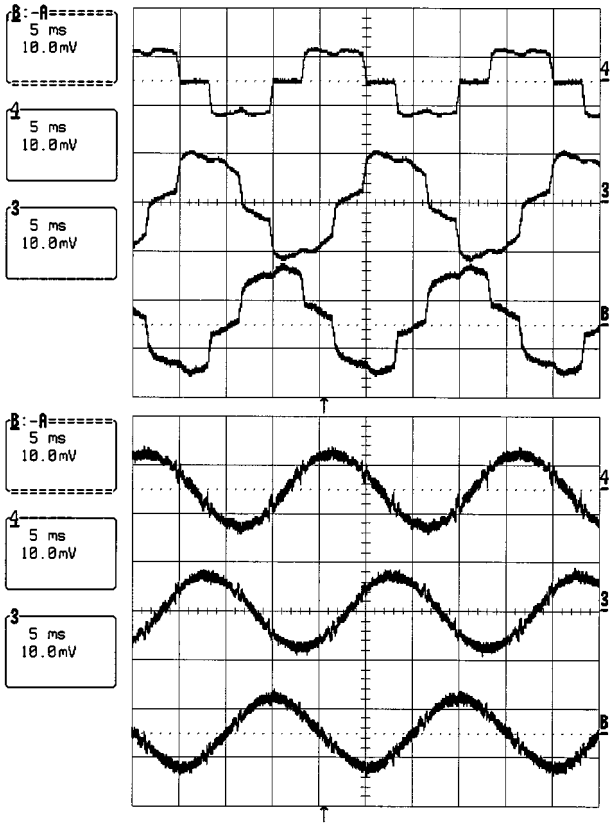

Fig. 18. Active filter behavior with unbalance and distorting loads. Top: load current (10 A/div); bottom: line currents (10 A/div) (dc-link voltage 450 V).

V. Conclusions

The use of a closed-loop control of line current harmonics seems to be very promising in active filter applications, where the distorting loads have slowly varying harmonics. In fact, using synchronous frame controllers for each selected harmonic, this approach performs the full compensation only for the selected harmonics even in the presence of a significant delay of the VSI current control, ensuring an active filter optimization in terms of performance and rating. Moreover, active filter interactions with possible dynamic components of the load are reduced. The complexity of the synchronous frame controllers has been avoided using equivalent transfer functions in the stationary frame controllers, whose design criteria have been highlighted in the paper. Experimental results on a 5-kVA prototype have demonstrated the effectiveness and advantages of the proposed solution.

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