A CMOS 128-APS linear array integrated with a LVOF for high-sensitivity and high-resolution micro-spectrophotometry

Chi Liu*, Arvin Emadi, Huaiwen Wu, Ger De Graaf, Reinoud F. Wolfenbuttel
Faculty of EEMCS, Department for ME/EI, Delft University of Technology,
Mekelweg 4, 2628 CD Delft, The Netherlands

ABSTRACT

A linear array of 128 Active Pixel Sensors has been developed in standard CMOS technology and a Linear Variable Optical Filter (LVOF) is added using CMOS-compatible post-process, resulting in a single chip highly-integrated high-resolution microspectrometer. The optical requirements imposed by the LVOF result in photodetectors with small pitch and large length in the direction normal to the dispersed spectrum (7.2μm×300μm). The specific characteristics of the readout are the small pitch, low optical signals (typically a photocurrent of 100fA~1pA) and a much longer integration time as compared to regular video (typically 100μs~63s). These characteristics enable a very different trade-off between SNR and integration time and IC-compatibility. The system discussed in this paper operates in the visible part of the spectrum. The prototype is fabricated in the AMIS 0.35μm A/D CMOS technology.

Keywords: Capacitive Transimpedance Amplifier, Correlated Double Sampling, Active Pixel Sensor, IC-compatible microspectrometers, LVOF, Variable Integration Time

1. INTRODUCTION

1.1 LVOF Microspectrometers

Microspectrometers have found application in many fields due to their small size and their low requirement on the sample volume. Figure 1 shows a general diagram of a dispersive microspectrometer. A Linear variable Optical Filter (LVOF) combined with a detector array is a suitable principle for the realization of a high-resolution microspectrometer, where the LVOF replaces the traditional grating as a dispersion component. A LVOF is actually a resonator cavity with a wedge shape. It is based on the theory of Fabry-Perot interference and the transmitted wavelength of the LVOF varies linearly with the cavity thickness. Therefore, a wide spectrum can be covered by the LVOF and no focusing element is needed. The optical resolution is mainly determined by the reflectance of the highly reflective coatings on the cavity walls. Complete LVOF fabrication involves CMOS-compatible deposition of the top and the bottom dielectric mirrors and a tapered layer in between, as shown in Figure 2 [1].

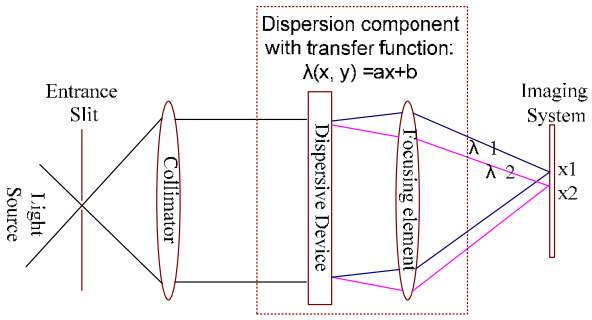

Figure 1 A general diagram for a spectrometer

*c.liu-2@student.tudelft.nl; phone +31 (0)15 2785745; fax +31 (0)15 2785755; ei.ewi.tudelft.nl

Optical Sensing and Detection, edited by Francis Berghmans, Anna Grazia Mignani, Chris A. van Hoof,
Proc. of SPIE Vol. 7726, 772616 · © 2010 SPIE · CCC code: 0277-786X/10/$18 · doi: 10.1117/12.854584

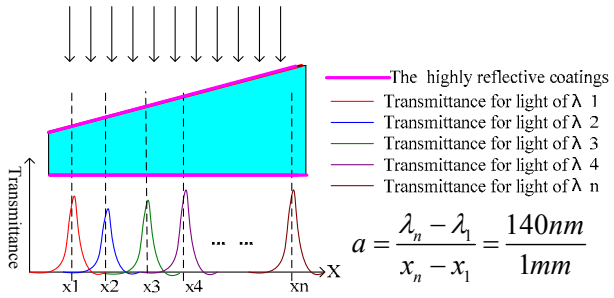

Figure 2 Principle of the Linear Variable Optical Filter (LVOF) [2]

1.2 Photodetection in LVOF Microspectrometers

A high-quality microspectrometer requires a custom-designed imaging system covered by the LVOF. The combined limitations of the LVOF design and the imaging system determine the performance of the microspectrometer in terms of spectral resolving power and light detection limit due to optical throughput (etendue). The spectral resolution of the microspectrometer is primarily determined by the LVOF design, whereas etendue is limited by the optical design and imposes the required detection limit of the detector in terms of minimum optical intensity. These parameters determine the quality of this microspectrometer. Unfortunately, reduced spectrometer dimensions are difficult to combine with high resolving power and etendue. A reduced optical throughput can be compensated for in a special mode of operation of the photodetector. Increasing the integration time of the detector is a solution. The spectral resolution should not be compromised by the photodetector design. The photodetector array specification in terms of element dimensions (pitch) and number of elements should be sufficient to cover the resolution by the LVOF. The taper angle of the LVOF, as published in [2], is sufficient for a spectral resolution of 2nm on the wavelength range between 540nm and 720nm over an LVOF length extending over 1mm. This LVOF will generates a dispersed pattern with a spatial bandwidth of 1/14.4 μm^{-1}. According to the Nyquist Sampling Theorem, a pixel pitch is required as small as 7.2μm.

There are commercialized image sensors and linear detector arrays, but their key performances are not optimized for on-chip photodetection in microspectrometers. There are two problems in the photodetection after the LVOF filtering, making the commercial image sensors less suitable:

(1) Low luminosity [3]. The function of the filter is to remove most of the input optical power by destructive interference. Therefore, only a small amount of light reaches the detector array. Thus the imaging system should be capable of low illumination detection.

(2) CMOS-compatibility. The smallest overall system dimensions are obtained when fabricating a LVOF right on top of the imaging system with the MOMEMS technology. This is an essential feature in applications such as lab-on-a-chip [4]. Thus a photodetection system with standard CMOS process is preferred for its low cost and high compatibility.

2. SMART CTIA-APS

A CTIA-APS linear array with 128 elements has been designed and fabricated within this framework, where CTIA is short for Capacitive Transimpedance Amplifier and APS is short for Active Pixel Sensor. This detector array is designed based the LVOF developed in [2]. The idea is to take advantage of the special optical pattern generated by the LVOF and to implement an IC-compatible photodetection module suitable for operation at low illumination intensities.

2.1 Detector Array

As discussed, the detector should be qualified in three aspects:

(1) Small pitches along the filter length for high spatial sampling frequency;

(2) Large light-sensitive area, for ensuring maximum sensitivity and SNR;

(3) IC compatibility.

The first two problems can be solved by applying a linear array of strip pixels. The extension of pixel length should compensate for the narrow pixel width. The nwell-psubstrate junction is selected for photodetection for an optimized responsivity in the visible light range. Considering all the specifications, the pixel size was selected at $7.2mm \times 300mm$.

2.2 Active Pixel Sensor with CTIA

Image sensors usually apply a junction capacitor as the charge-to-voltage convertor, which is not good for linearity; the popular 3T-APS has its light sensitive areas in proportional with its junction capacitance, which resulted in a limited sensitivity. A capacitive transimpedance amplifier is included in each pixel to avoid this problem, as shown in Figure 3 [5] [6].

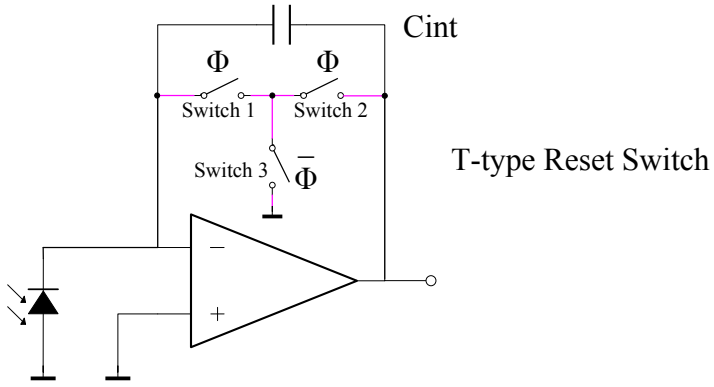

Figure 3 Capacitive Transimpedance Amplifier (CTIA) with a T-type switch

The introduction of the CTIA brings several benefits:

(1) The link between the light sensitive area and the charge-to-voltage conversion is avoided. The sensitivity can be improved by enlarging the pixel length and by decreasing the integration capacitor;

(2) The link between the accumulated charge and the integration capacitor is avoided. The linearity can be improved by implementing the integration capacitor as a poly-to-poly structure;

(3) The amplifier enables the implementation of T-type switches with large off-resistance [7], and thus long integration time. The readout time can then be traded for higher signal-to-noise ratio;

(4) By means of the virtual ground, the photodiode can be biased with a highly fixed biasing voltage, which reduces the charge modulation effect dramatically and leads to higher accuracy. The amplifier schematic is shown in Figure 4. A two-stage circuit is chosen for large output swing. The T-type switch across the input and output of the amplifier results in an off-resistance much larger than feasible with a single pass switch.

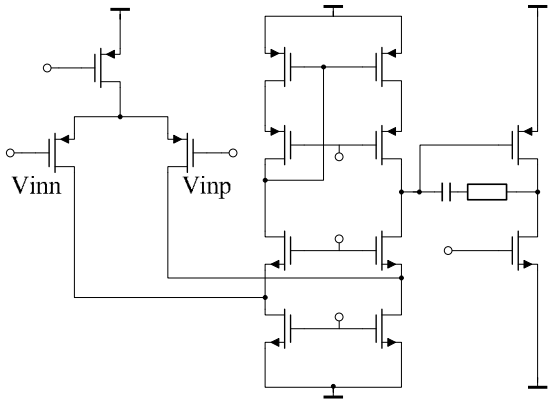

Figure 4 Schematic of the in-pixel amplifier

2.3 In-pixel CDS

Correlated Double Sampling as the traditional technique for reducing low-frequency noise is also applied here. The schematic [5] and the timing chart are shown in Figure 5 .

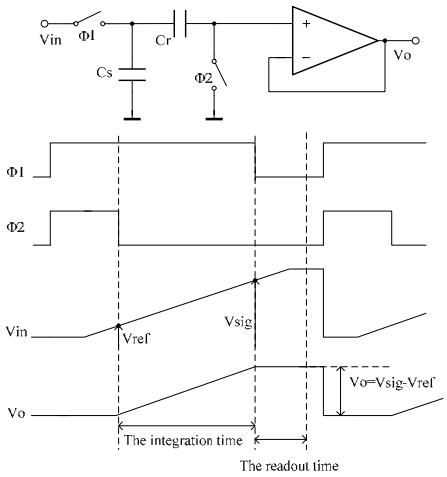

Figure 5 Schematic and timing chart for the buffered CDS

2.4 Variable Integration Time

Two different controls are applied for the photo detection, fixed integration time control and fixed voltage difference control. Both control principles are tested. The SNR and the dynamic range for the fixed integration time are [8] [9]:

$$\mathrm{DR}=20\log_{10}\frac{q_{\max}-I_{leakage}t_{\mathrm{int}}}{\sqrt{\sigma_r^2+q(I_{photo}+I_{leakage})t_{\mathrm{int}}}} \tag{1}$$

$$\mathrm{SNR}=20\log_{10}\frac{I_{photo}t_{\mathrm{int}}}{\sqrt{\sigma_r^2+q(I_{photo}+I_{leakage})t_{\mathrm{int}}}} \tag{2}$$

These expressions demonstrate that the SNR increases with integration time while the dynamic range decreases. Therefore besides the fixed integration time control, the fixed voltage difference control is also introduced to boost both the dynamic range and the signal-to-noise ratio. The In the fixed voltage difference control, the time consumed by the CTIA-APS output to increase from V1 to V2 is recorded, with the assistance of a reference clock [10]. This control principle brings three benefits:

(1) There is always a large amount of photons captured, even for low illumination levels. The photon shot noise will be the dominant noise source, which means a high SNR detection;

(2) The control principles can be implemented with digital logic circuits and integrated into each pixel simply. Each pixel can then work independently, needing no other control signals;

(3) The A/D conversion can be finished in the time recording by clock counters;

(4) The dynamic range can be improved by designing the clock and the counter appropriately, unlike in the fixed integration time control where it is jeopardized by the increasing of integration time. The working principle is shown in Figure 6.

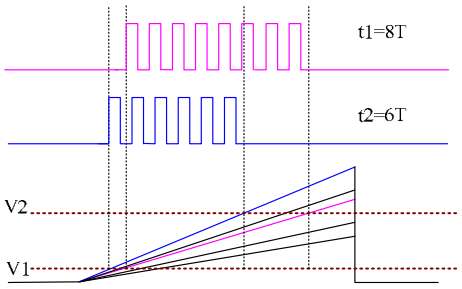

Figure 6 Working principle for fixed voltage difference control

2.5 Circuit Diagram

The circuit diagram of the readout is shown in Figure 7 (for simplicity the readout of only four pixels is shown). The standard timing chart of the pixel operation over one cycle is also presented in Figure 8.

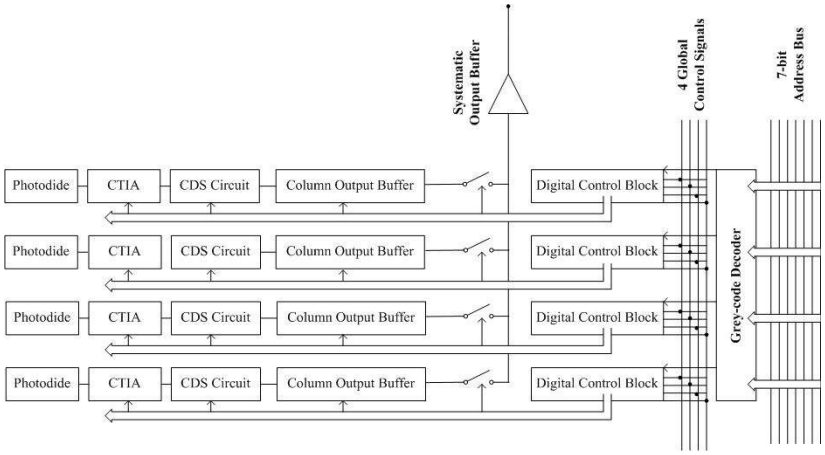

Figure 7 Complete system diagram

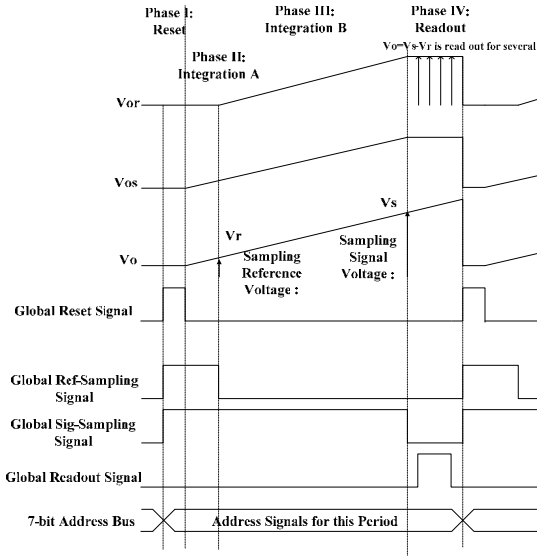

Figure 8 Standard timing chart for one pixel operation in one cycle

3. DEVICE PERFORMANCE

The prototype of this CTIA-APS array is designed and fabricated in standard CMOS technology, AMIS A/D 0.35μm. The initial tests used a halogen light source. A DAQ board controlled by a Lab View program is used for data acquisition, signal processing and generating control signals. The experimental results are to be discussed so as to demonstrate the performance of the device, including photodetectors' responsivity, leakage current, linearity, temporal noise and the APS operations under both control principles.

3.1 Photodetectors: Spectral Response and Leakage Current

The spectral response of the nwell-psubstrate junction has been tested. A Xenon lamp is used combined with a monochromator as the light source. A calibrated photodiode ORIEL 71638 has been used as the reference. The experimental result is show in Figure 9. The ripples in the spectral response curve are believed to originate from the SiN layer deposited on the wafer, which causes interference.

The leakage current contributes to the offset and the shot noise during the detection. Its effect should be estimated in advance. The leakage current of the nwell-psubstrate is tested and shown in Figure 9. It is observed that the leakage current is 4pA at a biasing voltage of 1.6V.

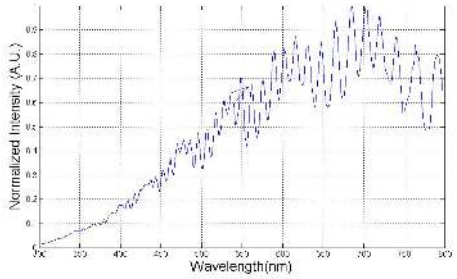

Figure 9 Spectral response of the n_{well}-$p_{substrate}$ junction

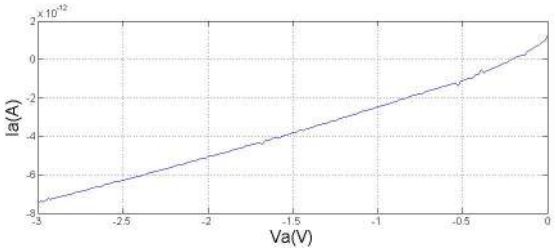

Figure 10 Leakage current of the n_{well}-$p_{substrate}$ junction

3.2 Basic APS operation

Figure 11 shows the output signal as a function of integration time at four different illumination levels. The biasing point is set at 0.9V for each photodiode. The maximum output signal before saturation is about 3.2V. The integration time can range from 100μs to 63s according to the light intensity. The minimum integration time is determined by the speed of ADC and the operations of switches. The maximum integration time is determined by the leakage current. The pixel leakage current is estimated at room temperature according to the basic APS operation and has been measured as about 30fA, which is lower than the value obtained in Figure 10.

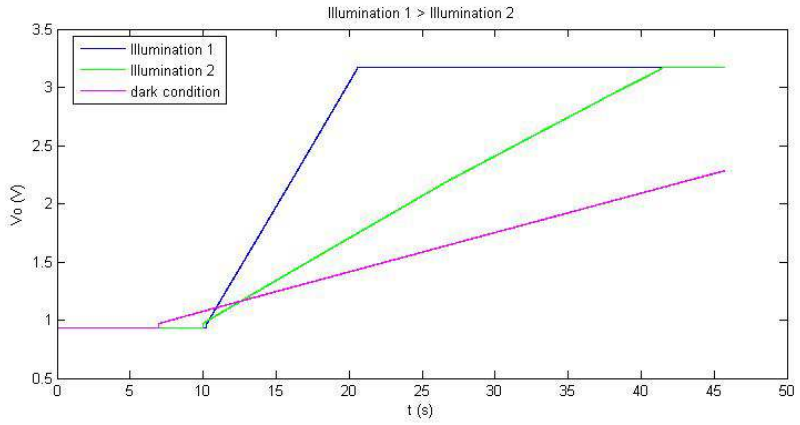

Figure 11 Output signal versus integration time

3.3 Temporal Noise

The temporal noise determines the minimum detectable signal. It is contributed by every stage along the in-pixel signal chain: (1) the photodiode contributes shot noises related to photocurrent and leakage current; (2) the CTIA contributes a readout MOS device noise as well as a reset noise; (3) the CDS circuit contributes a KT/C noise; (4) the in-pixel buffer contributes another component of circuit noise; (5) the DAQ board contributes the sampling noise. The temporal noise is first observed for all the stages of the test pixel. The measurement results are listed and discussed below.

Noise related to Photodetectors

The optical power is taken full advantage of in the photodetection only when the photocurrent-related shot noise dominates in the temporal noise. The total shot noise is estimated by the expression below [5]:

$$V_{\text{n,shot}} = \frac{\sqrt{q(I_{leakage} + I_{ph})t_{\text{int}}}}{C_{\text{int}}} \tag{3}$$

For a leakage current of 22fA and C_{int} of 500fF, the leakage current related shot noise is around $1.4' 10^{-8} V^2/s$. For an integration time of 60s, the equivalent output noise will be $900\mu V_{\text{rms}}$.

Noise related to Electronic Readout

The reset noise is the thermal uncertainty related to the output reset level. Both the reset noise and the flicker noise contributed by the CTIA can be eliminated largely by the correlated double sampling, while the thermal component of the readout noise can be reduced by averaging the multiple readout results. The CTIA readout noise is quantified at the output of the Capacitive Transimpedance Amplifier while the reset switch is kept on and in the dark condition. The noise of around $220\mu V_{\text{rms}}$ is observed. The readout noise contributed by the output buffer is tested similarly, as around $300\mu V_{\text{rms.}}$ The CDS KT/C noise is another major noise source at the APS output. It is a low frequency noise related to the two un-correlated sampling operations. This noise is quantified at the output of the CDS circuit in the dark condition, while the reset switch is kept on and the two CDS switches operates according to the standard timing chart for several cycles. The CTIA readout noise, which would otherwise appear at the CDS output, is removed by averaging the samples obtained within one cycle. The CDS KT/C noise is observed as around $240\mu V_{\text{rms.}}$

Overall Temporal Noise

The overall temporal noise is tested at the output of the test pixel in the dark condition, with all the switches operates according to the standard timing chart. An integration time of 5ms is applied in this case. A noise floor of $700\mu V_{\text{rms}}$ is observed, which is higher than the summing of the estimated noise contributions. On one hand, the DAQ board

contributes part of the noise; on the other hand, the reset noise and the readout flicker noise can not be removed fully at the same time. According to the applied timing chart and the given integration time, the flicker noise higher than 200Hz remains at the output.

3.4 CTIA-APS operation: Fixed Integration Time Control

Figure 12 shows the basic operation of this 128 CTIA-APS linear array, with half of the pixels illuminated while the rest set in the relatively dark condition. Their APS outputs are read out one by one sequentially through the multiplexer. At each end of the operation cycles, the output voltage is kept constant so as to be processed by the back-end circuit.

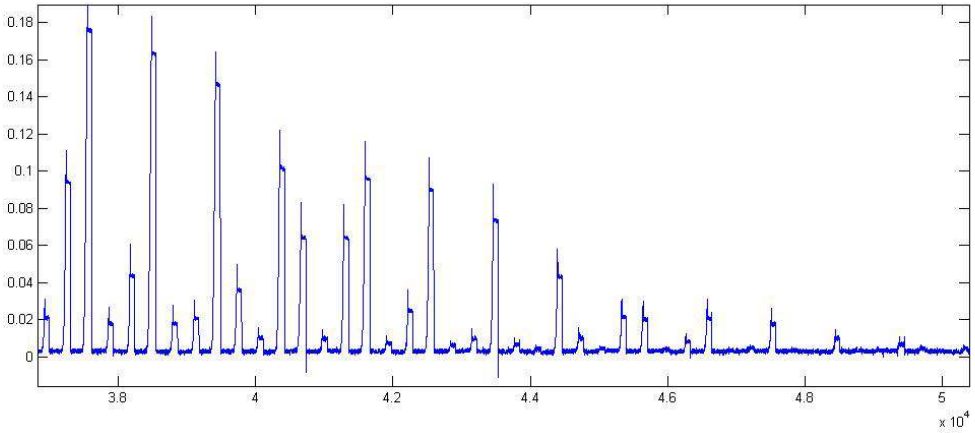

Figure 12 Operation of pixels under Fixed Integration Time Control

3.5 CTIA-APS operation: Fixed Voltage Difference Control

For the low illumination detection, a long integration time can be applied to ensure enough signal energy. Under the fixed voltage difference control, the pixel adapts its integration time according to the sensed illumination. Figure 13 shows how the tested pixel responds to the change of light intensity. In this control, the noise level is constant for all illumination levels, allowing a sensitive detection even for small optical power. For a further on-chip integration of this self-adapting functionality, two problems should be noticed: a limit on the maximum detectable signal is introduced by the speed of sampling and related logic control circuits; a limit on the minimum detectable signal may be introduced by the implementation for the in-pixel counter which is necessary for the time recording and the A/D conversion.

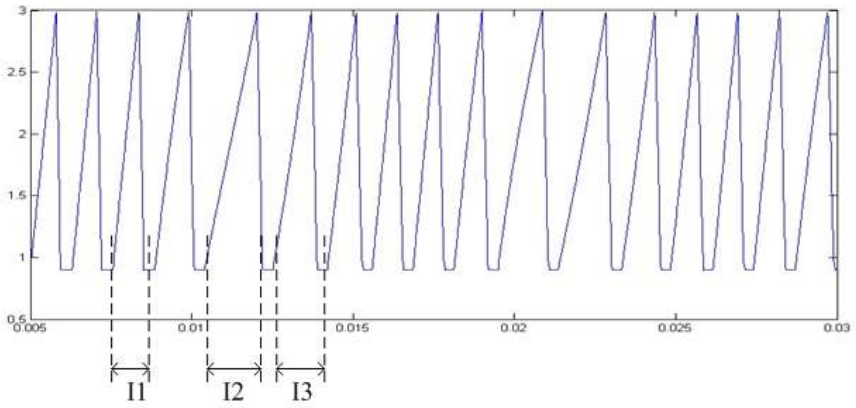

Figure 13 Operation of the test pixel under Fixed Voltage Difference Control with changing illuminations (Illumination levels: $I_1 > I_3 > I_2$)

4. SYSTEM CONFIGURATION WITH LVOF

The prototype of this linear CTIA-APS array is fabricated in the AMIS 0.35μ C035M-D/A process. Figure 14 shows the die photograph. To form a complete optical micro-system, a linear variable optical filter is fabricated right on top of the photodetection system by IC-compatible reflow [1]. Figure 15 shows the die photo of this microspectrometer. In such a combination, each pixel is supposed to detect a monochromatic light with a specific wavelength. Therefore by multiplexing the APS in this linear array, the interested spectrum can be scanned.

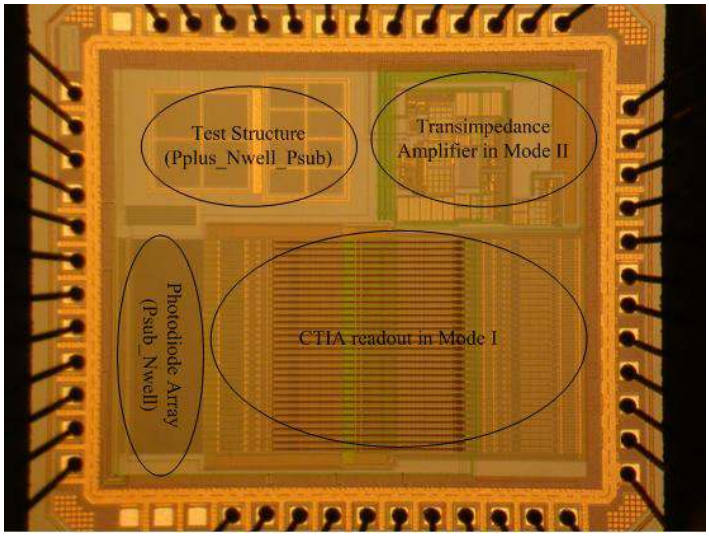

Figure 14 the die photo of the 128 CTIA-APS linear array

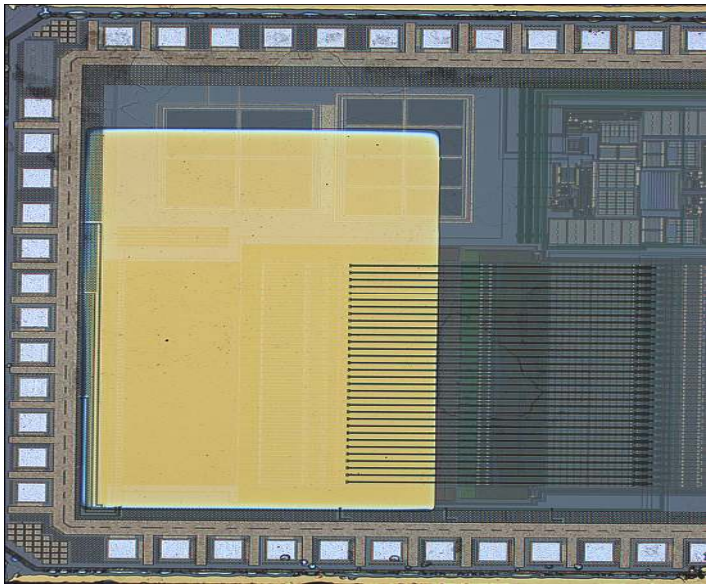

Figure 15 the die photo with the LVOF on top of the 128CTIA-APS linear array

5. CONCLUSION

In this paper a CMOS APS linear array has been designed specifically for application in an LVOF-based microspectrometer. An integration time as long as 100s can be applied to obtain high-SNR measurement results at low illuminations. A buffered CDS circuit and a complete Capacitive Transimpedance Amplifier are integrated at every pixel to increase the readout speed and to enable the testing using a Fixed Voltage Difference Control. A pixel pitch of 7.2μm is used, which is optimum for a spectral resolution 2nm in the LVOF-based microspectrometer.

REFERENCES

[1] Emadi A., Wu H., Grabarnik S., De Graaf G. and Wolffenbuttel R.F., "Vertically tapered layers for optical applications fabricated using resist reflow," Journal of Micromechanics and Microengineering 19(074014), 1-9(2009).

[2] Emadi A., Wu H., Grabarnik S., De Graaf G. and Wolffenbuttel R.F., "IC-compatible fabrication of linear variable optical filters for microspectrometer," Proc. Euro Sensors XXIII 1(1), 1143-1146(2009).

[3] Seong Ho Kong, [Infrared Micro-Spectrometer Based on a Multi-Slit Grating], PhD Thesis, Delft University Press, 13-15(2002).

[4] Ger De Graaf, [Mid-Infrared Microspectrometer Systems], PhD Thesis, Delft University Press, 23-27(2009).

[5] Hannati L., Pittet P., Lu G.N. and Carrillo G., "CMOS 32-APS linear array for high-sensitivity, low-resolution spectrophotometry," Sensors and Actuators B: Chemical 120(1), 142-149 (2006).

[6] Nagata, H., Shibai H., Hirao T., Watabe T., Noda M., Hibi Y., Kawada M. and Nakagawa T., "Cryogenic capacitive transimpedance amplifier for astronomical infrared detectors," IEEE Transactions on Electron Devices 51(2), 270-278(2004).

[7] Liu N., Chen G. and Hong Z., "A 0.18μm CMOS fluorescent detector system for bio-sensing application," Journal of Semiconductors 30(015002), 1-6 (2009).

[8] Chen, T., Catrysse P., El Gamal A. and Wandell B., "How small should pixel size be," Proc SPIE 3965, 451-459(2000).

[9] Catrysse P.B., Wandell B.A., and El Gamal A., "Comparative analysis of color architectures for image sensors," Proc SPIE 3650, 26-35(1999).

[10] Xu C., Chao S. and Chan M., "A New Correlated Double Sampling Technique for Low Voltage Design Environment in Advanced CMOS Technology," ESSDERC, 118-120 (2002).