A CMOS Bandgap Reference Circuit with Sub-1-V Operation

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***Abstract*— This paper proposes a CMOS bandgap reference (BGR) circuit, which can successfully operate with sub-1-V supply. In the conventional BGR circuit, the output voltage $V_{\rm ref}$ is the sum of the built-in voltage of the diode V_f and the thermal voltage V_T of kT/q multiplied by a constant. Therefore, $V_{\rm ref}$ is about 1.25 V, which limits a low supply-voltage operation below 1 V. Conversely, in the proposed BGR circuit, $V_{\rm ref}$ has been converted from the sum of two currents; one is proportional to V_f and the other is proportional to V_T. An experimental BGR circuit, which is simply composed of a CMOS op-amp, diodes, and resistors, has been fabricated in a conventional 0.4-μm flash memory process. Measured $V_{\rm ref}$ is 518 $\pm$ 15 mV (3σ) for 23 samples on the same wafer at 27–125°C.**

***Index Terms*—Bandgap reference, CMOS, low voltage.**

I. Introduction

Reference voltage generators are used in DRAM's, flash memories, and analog devices. The generators are required to be stabilized over process, voltage, and temperature variations, and also to be implemented without modification of fabrication process. The bandgap reference (BGR) is one of the most popular reference voltage generators that successfully achieve the requirements [1]. Regarding the generators, the demand for the low-power and low-voltage operation is strongly increasing the spread of battery-operated portable applications. The output voltage of the conventional BGR is 1.25 V, which is nearly the same voltage as the bandgap of silicon. This fixed output voltage of 1.25 V limits the low $V_{\rm cc}$ operation. This work proposes a BGR that can successfully operate with sub-1-V supply.

II. Conventional BGR Circuit

Fig. 1 shows the conventional BGR circuit, which is composed of a CMOS op-amp, diodes, and resistors. It is essential that the BGR circuit be designed without bipolar transistors because most semiconductor memories are fabricated in the CMOS process. A general diode current versus voltage relation

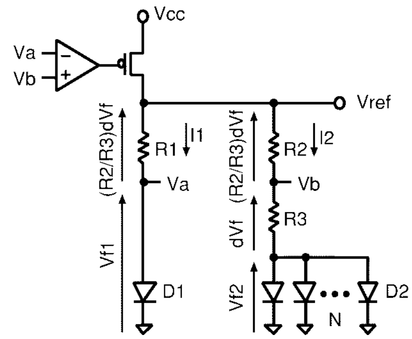

Fig. 1. Conventional BGR circuit, which is composed of a CMOS op-amp, diodes, and resistors.

is expressed as

$$I = I_s \cdot \left(e^{q\cdot V_f/k\cdot T} - 1\right) \cong I_s \cdot e^{q\cdot V_f/k\cdot T} \quad \Big| V_f \gg \frac{k\cdot T}{q} \tag{1}$$

$$V_f = V_T \cdot \ln\frac{I}{I_s} \tag{2}$$

where k is Boltzmann's constant (1.38 $\times$ 10^{-23} J/K) and q is electronic charge (1.6 $\times$ 10^{-19} C).

In the conventional circuit, a pair of input voltages for the op-amp, V_a and V_b, are controlled to be the same voltage. dV_f is the forward voltage difference between one diode $D1$ and N diodes $D2$

$$dV_f = V_{f1} - V_{f2} = V_T \cdot \ln\left(\frac{N\cdot R2}{R1}\right). \tag{3}$$

The BGR output voltage $V_{\rm ref}$ then becomes

$$V_{\rm ref} = V_{f1} + \frac{R2}{R3}dV_f \equiv V_{\rm ref}\_{\rm conv} \tag{4}$$

where V_{f1} is the built-in voltage of the diode and dV_f is proportional to the thermal voltage V_T. Here, V_{f1} has a negative temperature coefficient of -2 mV/°C, whereas V_T has a positive temperature coefficient of 0.086 mV/°C, so that $V_{\rm ref}$ is determined by the resistance ratio, being little influenced by the absolute value of the resistance. Thus, $V_{\rm ref}$ is controlled to be about 1.25 V where $V_{\rm ref}$ temperature dependence becomes

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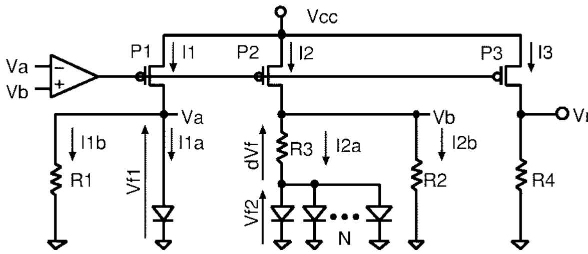

Fig. 2. Proposed BGR circuit.

negligibly small. As a result, the operational voltage V_{cc} cannot be lowered below than 1.25 V, which limits the low-voltage design for the CMOS circuits.

III. Proposed BGR Circuit

The concept of the proposed BGR is that two currents, which are proportional to V_f and V_T, are generated by only one feedback loop. Fig. 2 presents the proposed BGR circuit. The PMOS transistor dimensions of p_1, p_2, and p_3 are the same, and the resistance of $R1$ and $R2$ is the same

$$R1 = R2. \tag{5}$$

The op-amp is so controlled that the voltages of V_a and V_b are equalized

$$V_a = V_b. \tag{6}$$

Therefore, the gates of $p1$, $p2$, and $p3$ are connected to a common node so that the current $I1$, $I2$, and $I3$ becomes the same value due to the current mirror

$$I1 = I2 = I3. \tag{7}$$

In this case, $I1a = I2a$ and $I1b = I2b$

$$dV_f = V_{f1} - V_{f2} = V_T \cdot \ln(N). \tag{8}$$

$I2a$ is proportional to V_T

$$I2a = \frac{dV_f}{R3}. \tag{9}$$

$I2b$ is proportional to V_{f1}

$$I2b = \frac{V_{f1}}{R2}. \tag{10}$$

Here, $I2$ is the sum of $I2a$ and $I2b$, and $I2$ is mirrored to $I3$

$$I3 = I2 = I2a + I2b. \tag{11}$$

Therefore, the output voltage of the proposed BGR, V_{ref}, becomes

$$V_{\text{ref}} = R4\left(\frac{V_{f1}}{R2} + \frac{dV_f}{R3}\right) \equiv V_{\text{ref}}\text{\_prop}. \tag{12}$$

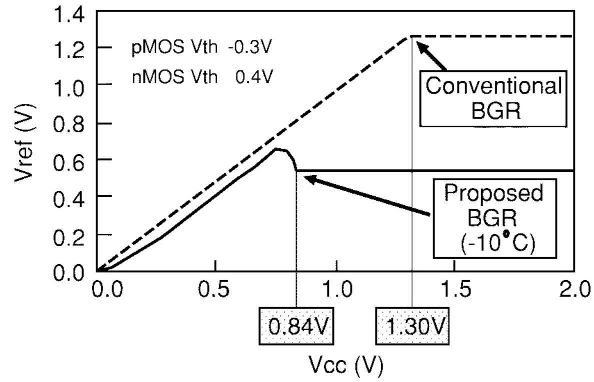

Fig. 3. Simulated V_{ref} characteristics of the conventional and proposed BGR's. The CMOS threshold voltages are optimized for the low-voltage operation, such as PMOS $V_{\text{th}} = -0.3$ V and NMOS $V_{th} = 0.4$ V.

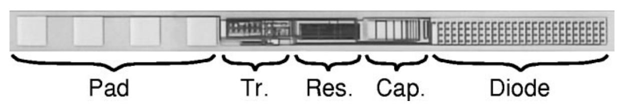

Fig. 4. Test-chip microphotograph. The size without the pads is 0.1 mm^2.

If the resistor and diode parameters for the proposed BGR are the same as those for the conventional BGR, V_{ref}_prop is simplified as

$$V_{\text{ref}}\text{\_prop} = \frac{R4}{R2} V_{\text{ref}}\text{\_conv}. \tag{13}$$

Therefore, V_{ref}_prop can be freely changed from V_{ref}_conv of 1.25 V. V_{ref} for the proposed BGR is determined by the resistance ratio of $R2$, $R3$, and $R4$ and little influenced by the absolute value of the resistance. The transistors $p1$, $p2$, and $p3$ are required to operate in the saturation region, so that their drain-to-source voltages can be small when the drain-to-source currents are reduced. Therefore, V_{cc} for the proposed BGR can be theoretically lowered to V_f if V_{ref} is set below V_f.

IV. Simulated Results

The V_{cc} minimum for the proposed BGR can be successfully lowered by the SPICE simulation when the threshold voltages are optimized for a low-voltage operation. Fig. 3 presents the simulated V_{ref} when the threshold voltages are optimized to ensure low-voltage operation of the op-amp, such as PMOS $V_{\text{th}} = -0.3$ V and NMOS $V_{\text{th}} = 0.4$ V, which can definitely be realized for a low-voltage design. Here, in the conventional BGR, V_{ref} is 1.25 V, and the V_{cc} minimum is 1.3 V. In the proposed BGR, however, the operational voltage is simply limited by V_f so that the V_{cc} minimum varies with the temperature. Even in the worst case of −10°C, the simulated V_{cc} minimum for the proposed BGR is 0.84 V, which is lower than that for the conventional BGR by 0.46 V.

V. Experiment Results and Discussion

Fig. 4 shows a chip microphotograph of the proposed BGR test chip, which has been fabricated in a conventional 0.4-μm flash memory process with P-substrate CMOS, single polysilicon, single silicide, and double metal. The test chip

TABLE I
PROCESS PARAMETERS

Flash Memory Technology	0.4μ m P-sub CMOS 1 polysilicon, 1 silicide 2 metal
PMOS Vth	-1.0V
NMOS Vth	0.7V
Native NMOS Vth	-0.2V

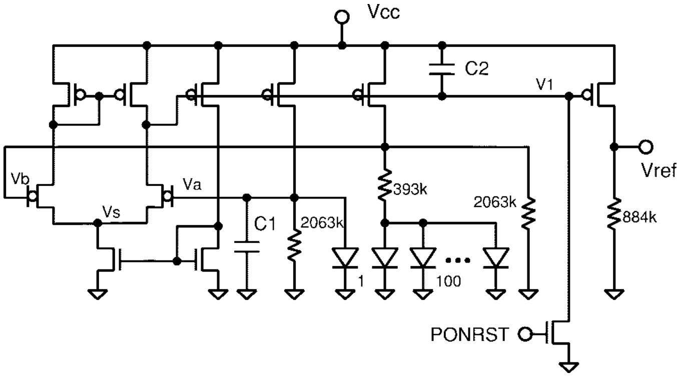

Fig. 5. Schematic of the proposed BGR test chip.

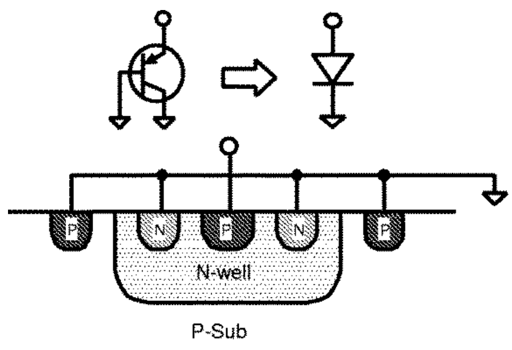

Fig. 6. Structure of the diode, which is easily fabricated by CMOS process.

is composed of four pads; some transistors, resistors, and capacitors; and 101 diodes. The size without the pads is about 0.1 mm^2. The process parameters for the test chip are summarized in Table I. The transistors were not designed for low-voltage operation, and their threshold voltages were high. The PMOS threshold voltage is -1 V, and the NMOS threshold is 0.7 V. Fig. 5 shows the circuit schematic of the proposed BGR test chip. An N-type diffusion layer is used for the resistors. Fig. 6 illustrates the structure of the diode, which is easily fabricated by CMOS process. The transistors, with V_a and V_b applied to the gates, are native NMOS transistors ($V_{\rm th} = -0.2$ V) because the threshold voltages of the enhancement-mode NMOS transistors exceed V_f in the standard 0.4-μm flash memory process. The control signal PONRST is used to initialize the BGR circuit when the power is turned on. The capacitors $C1$ and $C2$ stabilize the circuit. Fig. 7 shows the measured $V_{\rm ref}$ characteristics of the proposed BGR. $V_{\rm ref}$ is 515 mV $\pm$ 1 mV from 2.2 to 4 V at 27°C; and

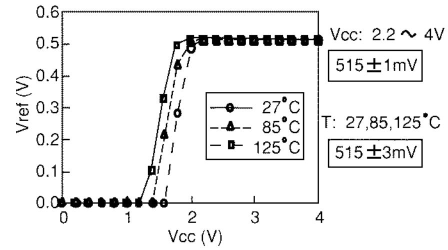

Fig. 7. Measured $V_{\rm ref}$ characteristics of the proposed BGR.

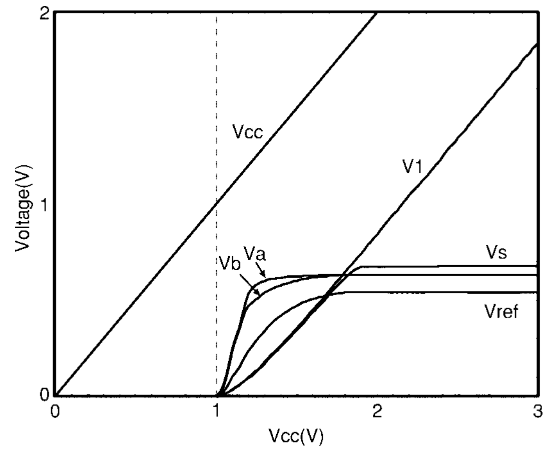

Fig. 8. Simulated results of the BGR implemented in the test chip.

515 mV $\pm$ 3 mV from 27 to 125°C for the whole voltage region, where the voltage resolution in the measurement is 1 mV. The operation current is 2.2 μA. Unfortunately, the transistors were not designed for low-voltage operation of the 0.4-μm flash memory, and their threshold voltages were high, so we utilized the native transistors. As a result, the op-amp operation was limited by a $V_{\rm cc}$ of 2.1 V. Fig. 8 shows the simulated results of the BGR implemented in the test chip. V_1 and V_s, as shown in Fig. 5, are respectively given by

$$V_1 \cong V_{\rm cc} + V_{\rm thp} \tag{14}$$

$$V_s \cong V_b - V_{\rm thi} \tag{15}$$

where $V_{\rm thp}$ (~ -1 V) is the threshold voltage of PMOS field-effect transistors (FET's) and $V_{\rm thi}$ (~ -0.2 V) is that of native NMOS FET's. The minimum $V_{\rm cc}$ of the BGR is determined as follows. In accordance with the decrease in V_1 with $V_{\rm cc}$ lowering, V_1 is equal to V_s. This defines the minimum $V_{\rm cc}$, $V_{cc\ \rm min}$, which is given by

$$V_{cc\ \rm min} \cong V_f - V_{\rm thi} - V_{\rm thp}. \tag{16}$$

Fig. 9 compares the measured $V_{\rm ref}$ distribution of the conventional and proposed BGR's. Supply-voltage, temperature, and process variations are included. There are four $V_{\rm cc}$ conditions and three temperature conditions. Thus, there are twelve matrix measurement conditions: $V_{\rm cc} = 2.4$, 2.7, 3.3, and 3.9 V; and temp $= 27$, 85, and 125°C. The number of samples is 34 for the conventional BGR and 23 for the proposed BGR. In the upper graph, 408 ($4 \times 3 \times 34$) points are plotted, and in

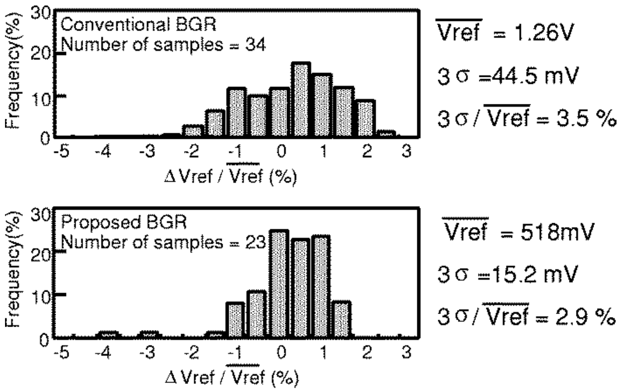

Fig. 9. Measured V_{ref} distributions of the conventional BGR and the proposed BGR. The temperature and voltages are varied in the measurement: Temp(27, 85, 125°C) × V_{cc}(2.4, 2.7, 3.3, 3.9 V).

the lower graph, 276 (4 × 3 × 23) points are plotted. The 3σ of V_{ref} for the proposed BGR is 15.3 mV, which is about one-third that for the conventional BGR of 44.5 mV. As a result, the normalized dispersion, $3\sigma/\mathrm{mean}(V_{\mathrm{ref}})$, for the proposed BGR is 2.9%, which is similar to that for the conventional BGR, 3.5%. The variation of V_{ref} for the proposed BGR mainly originates from an offset voltage of the op-amp, as it does for the conventional BGR. Considering the offset voltage of V_{os}, the BGR operates under the condition of

$$V_a = V_b + V_{\mathrm{os}}. \tag{17}$$

The total V_{ref}, including the effect of V_{os}, is given by

$$V_{\mathrm{ref}} \cong V_{f1} + \frac{R2}{R3}\,dV_f - \left(1 + \frac{R2}{R3}\right)\cdot V_{\mathrm{os}} \tag{18}$$

for the conventional BGR and

$$V_{\mathrm{ref}} \cong \frac{R4}{R2}\cdot\left\{V_{f1} + \frac{R2}{R3}\,dV_f - \left(1 + \frac{R2}{R3}\right)\cdot V_{\mathrm{os}}\right\} \tag{19}$$

for the proposed BGR. The ratio of the effect of V_{os} on V_{ref} for the proposed BGR is the same as that for the conventional BGR. To reduce the effect of V_{os} on V_{ref}, it is effective to decrease the ratio of $R2/R3$, i.e., to increase dV_f.

VI. CONCLUSIONS

A CMOS BGR, which can operate with sub-1-V supply, has been proposed and verified. V_{ref} is generated by the sum of two currents with one feedback loop. V_{ref} can be set at any level between 0 V and V_{cc}. The simulated V_{cc} minimum of 0.84 V has been achieved. The measured V_{ref} is 518 ± 15 mV for 3σ. The proposed BGR may therefore be a key technology for low-voltage CMOS circuit design.

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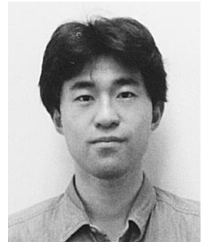

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