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ABSTRACT

An On-pixel Analog-to-Digital Converter based on both PFM and PWM schemes is reported. The proposed architecture uses a limited number of transistors that can be implemented in a small silicon area resulting in a 23% fill-factor. The digital sensor can be externally configured in order to operate under either the PFM or PWM scheme. At high-light intensities, the PFM scheme is replaced by the PWM scheme which proves to be much more efficient in terms of power consumption and clock frequency requirements. An in-built light adaptation mechanism has also been implemented which allows the sensor to better adapt to low-light intensity or to adjust the sensor saturation level. As a consequence, the sensor features a programmable dynamic range. Image lag is reduced in both schemes since a reset of the photodetector is performed after the conversion period. The pixel based ADC has been designed and fabricated using CMOS $0.25\mu m$ technology.

1. INTRODUCTION

Digital vision sensors are very important components of future multi-media and intelligent systems. In order to meet the requirement of such systems in terms of low cost and low power consumption, it is very important to integrate the Analogue-to-Digital Converter (ADC) on the chip. This provides the possibility of integrating on-chip digital processing together with the image acquisition circuitry allowing the designers to greatly benefits from the on-going advancement of CMOS technology. In order to fully benefit from these advantages, one must consider very carefully the trade-offs involved in such a VLSI implementation.

In digital vision applications, ADCs can be integrated at the array level [1,2], at the column level [3,4], or at the pixel level [5]-[7]. The array level approach is at present the most widely used. In this approach, a single ADC is used for the

entire array, which reduces the total silicon area and allows the realization of high fill-factor vision sensor since most of the pixel area would be dedicated to the photodetector. However, by using an array level ADC, the signal-to-noise ratio is reduced since the weak pixel output would drive the entire column bus. In addition, for video applications, very high speed ADC, operating at about 10Msamples/s, is required for the array level ADC, which tend to increase the power consumption. To lower the ADC operating speed, the column-level approach has been used [3,4]. In this approach, a battery of ADCs, each dedicated to one or more columns of the array, is used. The ADCs are operated in parallel, and therefore, low-to-medium-speed ADC architectures can be used. To lower ADC speeds even further the pixel-level approach has been recently introduced. In this approach, an ADC is dedicated to each pixel and the array is operated in parallel. Consequently very high frame rates can be obtained with ADCs operating at only tens of samples per second [6]. In addition, when ADCs are integrated at the pixel level the load capacitance seen at the pixel's output is negligible as compared to the one that is associated with the array based ADC which results in SNR improvements. Unfortunately, the main drawback of an on-pixel ADC is a reduced fill-factor of the image sensor since a significant part of the pixel area will be dedicated to the ADC circuitry. As a consequence, implementing high fill-factor On-pixel ADC is a real challenge that faces researchers and CMOS imager designers.

This paper presents two efficient Analog-to-Digital conversion schemes based on Pulse Frequency Modulation (PFM) and Pulse Width Modulation (PWM) principles. The digital sensor can be externally configured in order to operate under both schemes. In addition the circuit can be integrated with very limited number of transistors leading to a high fill-factor on-pixel ADC. Section 2 presents the principle of the PFM and PWM based ADC together with the sensor in-built light adaptation mechanism. Section 3 describes the VLSI design and presents the simulation results of the on-pixel ADC. Section 4 presents a conclusion.

2. PFM/PWM-BASED ADC

The main advantage of our proposed on-pixel architecture
is that it uses the same hardware resources to produce ei-
ther a PFM or a PWM coding at the sensor's output. The
circuit, as shown in the block diagram of Figure 1, is com-
posed of a photosensitive device (photodiode P_d) with its
internal capacitance C_d, a reset circuit, a feedback circuit,
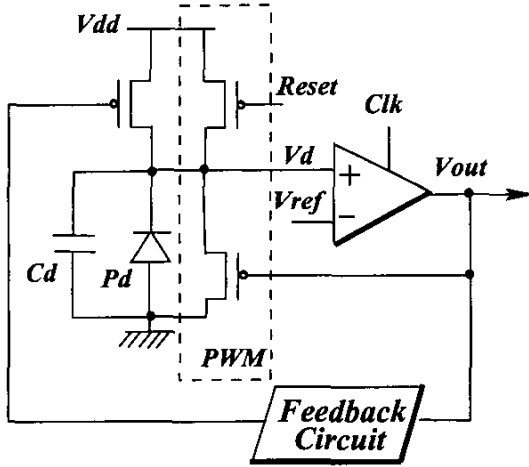and a clocked comparator.

Fig. 1. Block diagram of the proposed pixel based ADC.
Dashed lines corresponds to the circuit parts related to
PWM scheme.

The reset circuit can be either controlled by the feed-
back of the comparator in the case of the PFM mode or ex-
ternally, using the reset signal, in the case of a PWM mode.
For this last case, a PMOS transistor is also added in order
to reset the voltage Vd across the node of the photodiode.
For both modes, the light falling onto the photodiode Pd
is responsible for discharging the internal capacitor of the
photodiode Cd. This results in a linearly decreasing volt-
age Vd across the node of the photodiode. This voltage
Vd is compared to a reference voltage Vref using a volt-
age comparator triggered by a clock signal Clk. When the
voltage V_d reaches the reference voltage V_{ref}, the output of
the comparator V_{out} switches and a feedback circuit is used
to reset the photodiode node to either V_{dd} or V_{ss} in the PFM
mode or PWM mode respectively. At the next cycle, the
same procedure is repeated again for the PFM mode while
a stand-by is applied to the circuit, until an external reset
signal is received, in the case of the PWM mode. A pulse is
generated at the output of the comparator whenever the volt-
age V_d reaches V_{ref}. Figures 2.A and 2.B show the voltage
across the photodiode V_d and the output of the comparator
V_{out} for the PFM and PWM modes respectively. It can be
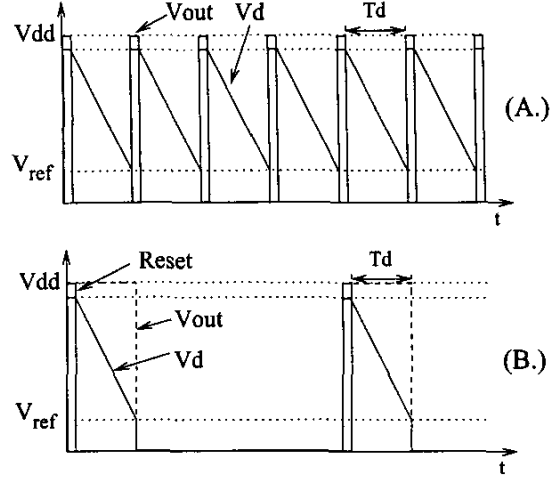seen that only one pulse is needed for the PWM mode while

Fig. 2. Waveforms at different nodes of the circuit. Vd
is the voltage across the photodiode, Reset is the external
reset signal applied in the case of the PWM sceme, Vout is
the output voltage of the comparator.

a train of pulses is required for the PFM based conversion.
On both Figures (2.A and 2.B), T_d represents the discharge
time of the capacitor from V_{reset} to V_{ref} which can be ex-
pressed by:

$$T_d = \frac{(V_{reset} - V_{ref}) \times C_d}{i_d} \qquad (1)$$

where i_d and C_d are the photocurrent and the photodiode ca-
pacitor, respectively. The frequency f of the voltage across
the photodiode V_d, for the PFM mode, is inversely propor-
tional to T_d and therefore can be expressed as:

$$f \approx \frac{1}{T_d} = \frac{i_d}{(V_{reset} - V_{ref}) \times C_d} \qquad (2)$$

The pulse width for the PWM scheme represented on Figure
2.B can also be expressed by:

$$P_w = T_d = \frac{(V_{reset} - V_{ref}) \times C_d}{i_d} \qquad (3)$$

The switching frequency f (and the pulse width P_w) of the
comparator output V_{out} for the PFM mode (and the PWM
mode) is directly proportional (inversely proportional) to
the capacitor discharge current i_d. Therefore, a conversion
from photocurrent to pulse frequency (and pulse width) is
obtained. In order to obtain the digital output from the
two previous coding schemes, the output of the comparator
is directly connected to the input of a digital configurable
counter/decounter. The output of the comparator is either
connected to the counter input in the case of PFM scheme
or to the Enable signal of the clocked decounter in the case
of the PWM scheme.

In the case of the PFM scheme, the enable signal (En) is provided externally allowing the counter to be operational only during a counting period T_{cnt}. The number of impulses detected by the counter is therefore given by:

$$N_{imp} \simeq \frac{T_{cnt}}{T_d} \simeq \frac{T_{cnt} \times i_d}{(V_{dd} - V_{ref}) \times C_d} \qquad (4)$$

Global adaptation to the mean light intensity of the digital sensor can be simply implemented by modulating the T_{cnt} signal according to the mean light intensity. If the sensor is being used in a given scene where illumination levels result in a photocurrent varying from 0 to i_{dm}, then T_{cnt} will be modulated such that 2^n impulses resulting from the PFM scheme are counted for the highest photocurrent i_{dm}, where n is the number of bits. By substituting $N_{imp} = 2^n$ and $i_d = i_{dm}$ in Eq.(4) we deduce the optimum T_{cnt} as follow:

$$T_{cnt} = 2^n \times \frac{(V_{dd} - V_{ref})}{i_{dm}} \times C_d \qquad (5)$$

In our digital sensor, the Enable signal of the counter, which is high during T_{cnt}, is therefore used to adapt the ADC to different illumination levels so that the brightest pixel would always generate 2^n pulses and hence would correspond to the full range of the ADC. According to this adaptation mechanism, for each environment where the photocurrent varies from 0 to i_{dm}, a corresponding optimum T_{cnt} can be obtained using Eq.(5). This T_{cnt} will correspond to the minimum counting time that allows the use of the ADC's full range. In other words, T_{cnt} will optimise the dynamic range as well as the conversion speed of the ADC. Table 1 illustrates a typical example in which we consider the use of the ADC for three different environments: (i) a typical bright office; (ii) a typical outdoor light, and (iii) a typical sunlight. In this example Tcnt is obtained from Eq.(5), with V_{dd} = 2.5V, V_{ref} = 1V, C_d = 1fF and n = 8-bits. For the three cases, the ADC operates within its full dynamic range (digital output: 00-FF).

Table 1. Conversion results for an 8-bit accuracy using Optimal T_{cnt} values (Eq. 5) for three different environments.

Environment	Photocurrent ”i_d”	Optimal ”T_{cnt}”	Digital Output (Hex)
Bright office	$0-2$ nA	192 μs	$00-FF$
Outdoor light	$0-4$ nA	96 μs	$00-FF$
Sunlight	$0-8$ nA	48 μs	$00-FF$

The previous example shows that the Enable signal provides the possibility to adapt the sensor to any illumination level and allows the ADC to operate within its full range providing a programmable dynamic range of the photosensor. This last feature is usually obtained through a complex gain control amplifier integrated within the photodetectors array. In our case, this is simply realized by using a digital enable signal of a conventional digital counter. It must be noticed that for high level of illumination it is required to maintain the clock frequency of the comparator very high in order to reduce offset errors. Figure 3 shows the required clock frequency of the PFM scheme, for different illumination levels and for different precisions.
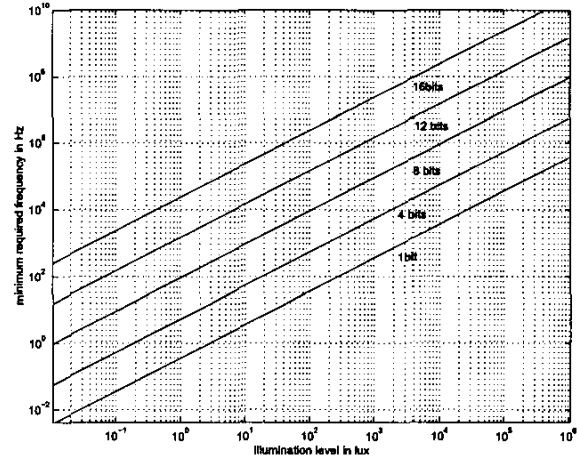
Fig. 3. Required clock frequency of the comparator as function of the illumination level for different precisions.

From this figure one can deduce that for higher level of illuminations the power consumption of the PFM scheme is dramatically increased which makes the PWM approach more suitable.

3. VLSI DESIGN

Both the PFM and the PWM based converters operate in two different phases: (i) counting phase and (ii) shift-out phase. During the counting phase, all the pixels are operated in parallel resulting in full parallelism. Once the conversion is achieved, the shift-out mode is set and the digital values of the pixels stored in the internal registers are red-out. In this scheme, no read-out circuit is needed and hence the silicon area is fully dedicated to the photodetector array.

Additional gating circuitry has been included within each pixel in order to switch all the analog circuitry part to a stand-by mode during the shift-out phase. The circuit is also placed at a stand-by mode once the pulse is obtained for the PWM scheme. This has resulted in a significant reduction in power consumption during the shift-out phase. The average power consumption per pixel at a frequency of 200KHz is estimated at $85\mu W$ and $10\mu W$ for PFM and PWM respectively. More than 95% of this power is dissipated during the counting phase.

Figure 4 shows the layout of the pixel based ADC. It has been implemented using CMOS $0.25\mu m$ technology and occupies an area of $45 \times 45\mu m^2$ with a fill-factor of 23%. Careful attention has been paid to the layout of the pixel by separating the analog and digital parts and using guard rings and grounded shields.
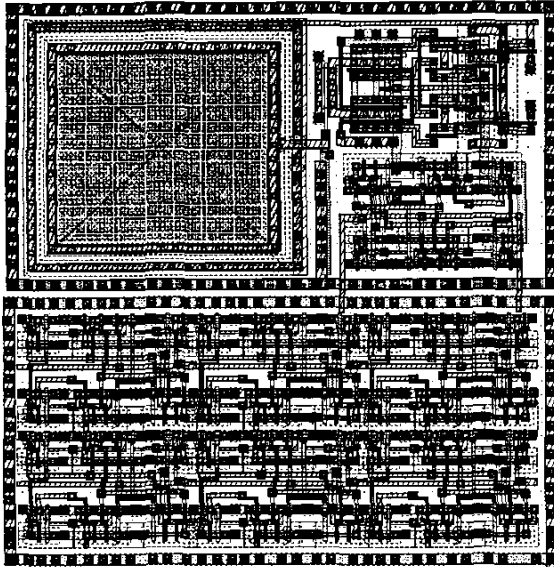

Fig. 4. Layout of the pixel based ADC. It occupies an area of $45 \times 45\mu m^2$ with a fill-factor of 23%.

4. CONCLUSION

In this paper I have presented a digital vision sensor based on both the PFM and PWM schemes. The proposed architecture uses a simple circuit that can be implemented in a small silicon area resulting in a 23% fill-factor. The main advantage of the proposed on-pixel architecture is that it uses the same hardware resources to produce either a PFM or a PWM coding at the sensor's output. This feature allows the user to switch the converter to either modes depending on the light intensity. For example, At high-light intensities, the PFM scheme is replaced by the PWM scheme which proves to be much more efficient in terms of power consumption and clock frequency requirements. An in-built light adaptation mechanism has also been implemented in the PFM mode, whereby it is possible to either improve the low light performance of the digital sensor or to modify its saturation level. As a consequence, the proposed sensor features a programmable dynamic range. This feature reduces considerably the blooming effect that can occur for typical natural scene illumination conditions.

A prototype including an array of 32×32 pixels has been designed and fabricated using CMOS $0.25\mu m$ technology. The circuit occupies an area of $10mm^2$. The average power consumption per pixel at a frequency of 200KHz is estimated at $85\mu W$ and $10\mu W$ for PFM and PWM respectively.

Acknowledgement

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