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A CMOS In-Pixel CTIA High Sensitivity Fluorescence Imager

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Abstract

Traditionally, charge coupled device (CCD) based image sensors have held sway over the field of biomedical imaging. Complementary metal oxide semiconductor (CMOS) based imagers so far lack sensitivity leading to poor low-light imaging. Certain applications including our work on animal-mountable systems for imaging in awake and unrestrained rodents require the high sensitivity and image quality of CCDs and the low power consumption, flexibility and compactness of CMOS imagers. We present a 132×124 high sensitivity imager array with a 20.1 μm pixel pitch fabricated in a standard 0.5 μ CMOS process. The chip incorporates n-well/p-sub photodiodes, capacitive transimpedance amplifier (CTIA) based in-pixel amplification, pixel scanners and delta differencing circuits. The 5-transistor all-nMOS pixel interfaces with peripheral pMOS transistors for column-parallel CTIA. At 70 fps, the array has a minimum detectable signal of 4 nW/cm^2 at a wavelength of 450 nm while consuming 718 μA from a 3.3 V supply. Peak signal to noise ratio (SNR) was 44 dB at an incident intensity of 1 μW/cm^2. Implementing 4×4 binning allowed the frame rate to be increased to 675 fps. Alternately, sensitivity could be increased to detect about 0.8 nW/cm^2 while maintaining 70 fps. The chip was used to image single cell fluorescence at 28 fps with an average SNR of 32 dB. For comparison, a cooled CCD camera imaged the same cell at 20 fps with an average SNR of 33.2 dB under the same illumination while consuming over a watt.

Index Terms

CMOS imager; fluorescence imaging; capacitive transimpedance amplifier (CTIA); low-light imaging; microscopy; functional imaging

I. Introduction

Fluorescence imaging is a powerful technique for minimally invasive spatiotemporal mapping of structure and function of cellular and neural systems [1]. Imaging offers the

potential to investigate at multiple scales - from single cells to tissues. Photodetectors for various fluorescence imaging techniques used in biology have a range of required specifications. On one end of the spectrum are photon-starved processes like multi-photon [2] and confocal fluorescent imaging [3], which need very high sensitivity and low dark current. One the other hand, certain functional imaging techniques that look at fast dynamic changes like action potentials require fast frame rates and a high dynamic range apart from good sensitivity. Examples include imaging voltage [4] and calcium [5] sensitive dyes.

While imaging *in vitro* systems like fixed specimens or tissue slices can be used to study anatomy and functional connectivities, imaging in live animals has opened a window to investigate physiological processes in their native, unperturbed state. Most *in vivo* imaging is done in anesthetized and restrained animals. However, a fast emerging area is imaging in awake and behaving animals. Majority of the work in this area has used optical fiber bundles or electrical cables, tethering the animal to traditional imaging system components [6]–[8]. This relaxes power and size constraints on the photodetector allowing the use of commercially available large, power-hungry cooled CCD or CMOS cameras. However the tethers imposed by such systems greatly limit the nature and duration of imaging studies that can be done. A few groups are attempting to move the entire imaging apparatus into a compact device that can be affixed to an animal for chronic imaging [9]–[11] avoiding the use of optical fibers and cables. Photodetectors for such systems need to be compact and low powered in addition to having sufficient sensitivity and high signal-to-noise (SNR) performance comparable to detectors traditionally used for biomedical imaging.

Though charge coupled device (CCD) and complementary metal oxide semiconductor (CMOS) based image detectors were both invented around the late 1960s, their development took different routes [12]. From their inception till the 1990s, fabrication technology was not developed enough to take advantage of the key benefit of CMOS detectors - the ability to integrate circuits on the image plane. CCD detectors [13], [14] were optimized for applications requiring very high sensitivity and superior low-light performance. Due to this, almost all low-light biomedical imaging is done with CCD based imagers. Today CMOS detectors [15], [16] offer compact, single-chip, low power integrated systems capable of not only detecting photons but also performing signal and image processing operations [17], [18]. However, they still lag behind CCD detectors in sensitivity and low-light performance. For this reason CMOS detectors are used only in medium- to highlight applications where dynamic range or speed rather than sensitivity is critical [19].

The requirement for high performance with a small power-and size-footprint has led to some recent work on high-sensitivity CMOS imagers for biomedical applications. Ng *al.* presented a 176×144 imager with 7.5 μm pixels in a 0.35 μ CMOS process as part of an integrated system that could be implanted in deep brain structures for fluorescent imaging [20]. The minimum detectable signal was 100 nW/cm^2 at 470 nm with a frame rate of 0.31 fps. Eltoukhy *et al.* presented a 8×16 imager with 240 μm × 210 μm pixels designed in a imager-customized 0.18 μ CMOS process for bioluminiscence detection. The chip was capable of detecting 0.1 pW/cm^2 at 562 nm with an exposure time of 30 s [21]. Beiderman *et al.* reported a 128×128 imager with 7 μm pixels in a 0.18 μ CMOS process with an integrated fluorescence emission filter for contact imaging [22]. At 30 fps, the minimum detectable intensity was 400 nW/cm^2 at 450 nm with an SNR of 15 dB. Park *et al.* presented a 32×32 imager with 75 μm pixels in 0.5 μ CMOS process for voltage sensitive dye imaging [23]. At 40 fps, the minimum detectable signal was about 10 lux (~3 μW/cm^2)[†] with an SNR of 35.2 dB.

[†]Converted using photopic luminosity function and assuming broadband illumination

None of the above systems combine the sensitivity, resolution, speed and flexibility required for a detector capable of imaging single-cell fluorescence at low illumination levels. We present a 124×132 imager with 20.1 μm pixels in a 0.5 μ CMOS process, capable of imaging single cell fluorescence at light levels equal to those required by cooled CCD cameras. The 5-transistor pixels feature n-well/p-sub photodiodes and a capacitive transimpedance amplifier (CTIA) for signal amplification [24] and noise reduction [25]. The novel design splits the amplifier with only nMOS transistors inside the pixels. Each column shares the pMOS transistors of the CTIA.

The paper is organized as follows. Section II describes the circuit design of the imager including the photodiode, the active pixel sensor circuit and peripheral circuits. Circuit analysis including simulation and noise analysis is presented in Sec. III. Section IV shows measurement results from the array and Sec. V concludes the paper.

II. Chip Architecture

The design of the chip can be divided into three distinct modules - the photodiode, the capacitive transimpedance amplifier (CTIA) and the peripheral circuits. All metal interconnects were done in metal1 and metal2 layers. Non-photosensitive areas of the chip were covered by metal3 and care was taken to design the sensitive analog output pads without protection diodes to prevent non-specific photo-induced output from outside the pixel array.

A. Photodiode

Based on our prior work characterizing photodiodes in 0.5 μ CMOS technology [26], the imager array was designed with n-well/p-sub photodiodes. Some of the advantages of this topology are:

1. Low-doped n-well creates a wider depletion region, increasing the collection efficiency of the junction.
2. Since n-wells are created by diffusion, the junction tends to be deeper than n+/p-sub junctions with significant sidewalls, further increasing collection efficiency.
3. Wider depletion region leads to a smaller capacitance, increasing the charge-to-voltage conversion ratio.

The pixel was designed with a pitch of 20.1 μm. The photodiode area was 170 μm^2 leading to a fill factor of 42%. While this seems small, scalable design rules for the process used, require a minimum of 18λ between n-wells. In 0.5 μ CMOS (λ = 0.3), the largest photodiode that can fit in a 20.1 μm pixel is 14.7 μm × 14.7 μm with a fill factor of 53.5%. The perimeter of the photodiode, a measure of the lateral sidewall dimension, was 58 μm. The photodiode was designed to occupy a roughly square area in a corner of the pixel with a two-sided border containing circuits and metal interconnect lines. Corners of the photodiode were cut to reduce dark current. Layout of the pixel showing the photodiode location and geometry is shown in Fig. 1.

B. Capacitive Transimpedance Amplifier (CTIA)

CTIAs have been used in image sensors initially as column amplifiers [27] and also as in-pixel amplifiers [24]. These designs included entire CTIA layouts in the pixel, requiring area-expensive pMOS transistors in the pixel. Our design partitions the amplifier and includes only nMOS transistors in the pixel. The pMOS transistors that complete the amplifier are shared by all the pixels in a column. This partitioning follows from the detector implementing a rolling shutter where only one row needs to be fully active at any time.

Figure 2 shows the schematic of a single pixel enclosed within the dotted line containing nMOS transistors M1–M5, feedback capacitance C_{fb} and the photodiode. Also shown are the column level pMOS transistors that complete the CTIA (M6, M7).

Transistors M1 ($12\mu/1.2\mu$), M2 ($2.4\mu/2.4\mu$), M6 ($16.8\mu/4.2\mu$) and M7 ($16.8\mu/4.2\mu$) implement a cascoded high gain inverting amplifier which constitutes the CTIA when a particular row is selected with M3 ($1.8\mu/0.6\mu$) and M4 ($1.8\mu/0.6\mu$), which are minimum sized switches, being shorted by a logical high on the row select line (RS). Transistor M1 was sized and biased to be in sub-threshold, maximizing the gain to current ratio for maximum energy efficiency and minimum noise. M6 and M7 were sized relatively larger to ensure sufficient drive capability for the long output lines. Poly1/poly2 capacitor C_{fb} acts as the feedback element in the closed loop CTIA with a value set to 5 fF ($2.4\mu \times 2.4\mu$). Transistor M5 ($1.8\mu/0.6\mu$) was a minimum sized switch which served to set the amplifier output to its inversion point. Bias voltages V_{cn}, V_{cp}, and V_{bp} were generated off-chip. Layout and relative positions of the transistors and the capacitor are shown in Fig. 1 and a simplified block diagram is shown in Fig. 3a. The CTIA output was connected to a column level delta difference sampling (DDS) circuit that is described in the next section.

C. Peripheral Circuits

The peripheral circuits for the imager array consist of pMOS transistors that complete the column level CTIA, sample and hold based circuits for column level delta difference sampling, circuits for row and column scanning and output buffers.

1) Delta Difference Sampling—Figure 3b shows the schematic of the circuit for performing delta difference sampling which calculates the difference between a pixel's light-dependent signal value and the subsequent reset value as a measure of the photon flux [28]. Capacitors C_1 and C_2 were poly1/poly2 capacitors sized to 150 fF, laid out as a parallel combination of six 25 fF unit capacitances ($5.7\mu \times 5.7\mu$) for good matching [29]. Transmission gates T1 and T2 and nMOS switch M1 were realized with minimum sized ($1.8\mu/0.6\mu$) transistors. T1 and T2 were driven by non-overlapping clocks generated on chip from an external clock hold. M1 was driven by an external signal sample. The amplifier was realized as a single stage cascoded inverting amplifier as shown with M2 ($9.6\mu/1.2\mu$) sized and biased in sub-threshold. Since the drive requirements for the amplifier are smaller than those for the in-pixel CTIA, M3, M4 and M5 were sized small ($2.4\mu/2.4\mu$) to pitch match the circuit to the pixel. The DDS output was multiplexed to an output buffer controlled by the column ring counter, described in the following section. Bias voltages V_{cn}, V_{cp}, V_{bp}, and V_{ref} were generated on-chip using a resistor chain between Vdd and ground. Note that these biases were different from the ones for the in-pixel CTIA.

2) Row and Column Scanners—The row scanner consisted of circuits for selecting and resetting an addressed row shown by signals RS and RST in Fig. 2. For addressing rows, a 124 bit circular shift register was implemented. The column scanner consisted of the pMOS transistors of the pixel CTIA, the DDS circuit and a 132 to 1 multiplexer for connecting the output of an addressed column to the output buffer. The multiplexer was implemented as switch array with one transmission gate for each column. A similar multiplexer also connected the pixel output directly without the DDS circuit to a second output buffer. Column addressing was done by a 132 bit circular shift register. The row and column shift registers were driven by non-overlapping clocks generated from external signals ROWCLK and COLCLK. Both registers could be programmed with a desired sequence from an external pin and the respective clock signals.

3) Output Buffer—A very simple output buffer was implemented as a single large nMOS transistor (120μ/2.4μ). The gate of the transistor was driven by the output of the 132 to 1 multiplexer in the column scanner. Both the source and the drain of the transistor were brought out to pads on the die. An off chip resistor was used to configure the transistor as a source follower to buffer the output of the DDS circuit. A similar circuit buffered the output of the pixel directly without delta differencing.

III. Circuit Analysis and Simulations

A. Pixel Operation

Consider the simplified circuit of the pixel when its row is selected shown in Fig. 3a with C_{pd} and C_{fb} referring to the photodiode and feedback capacitances. Let the CTIA, composed of in-pixel nMOS transistors and column level pMOS transistors, have an open loop gain of A. At the input node of the CTIA, we can write:

$$I_{pd}(s)+\left(\frac{v_{out}(s)}{A}-v_{out}(s)\right)sC_{fb}+\frac{v_{out}(s)}{A}sC_{pd}=0 \quad (1)$$

which simplifies to:

$$v_{out}(s)=\frac{I_{pd}(s)}{sC_{fb}\left(1-\left(1+\frac{C_{pd}}{C_{fb}}\right)\frac{1}{A}\right)} \quad (2)$$

Assuming $A \gg C_{pd}/C_{fb} > 1$ we have:

$$v_{out} \approx \frac{1}{C_{fb}}\int I_{pd}dt \quad (3)$$

Equation 3 describes the operation of the CTIA pixel. During the pixel reset, signal RST is high, forcing the photodiode and the amplifier output nodes to the inversion point of the amplifier. Once RST is released, the amplifier pins the output node of the photodiode and forces the photocurrent to integrate on C_{fb}. C_{fb} is a design parameter unlike C_{pd}, which is dependent on the size and the nature of the photodiode junction. Effectively, by implementing $C_{fb} < C_{pd}$, a gain of C_{pd}/C_{fb} can be achieved over the operation of the standard three-transistor (3T) pixel [16]. This increases the sensitivity of the pixel by improving the charge-to-voltage conversion by a factor given by the CTIA gain. Another departure from 3T operation is that due to the inverting nature of the CTIA, the output of the pixel charges upward towards Vdd in response to light as opposed to discharging towards ground. Mathematically, $dv_{out}/dt > 0$.

Figure 4 shows a simulation of the pixel. The following parameters were used: C_{pd}=150 fF and I_{pd}=6 pA. With a bias current of 200 nA and a capacitive load of 1 pF, the amplifier had a simulated open loop gain of 85 dB and a gain-bandwidth product of 675 kHz. Trace out5f corresponds to C_{fb}=5 fF and trace out10f corresponds to C_{fb}=10 fF. The slopes of the traces, 1.12 kV/s and 580 V/s, correspond well to the expected values from equation 3, 1.2 kV/s and 600 V/s for the 5 fF and 10 fF cases, respectively.

B. DDS Operation

The DDS operation [28] consists of two phases. With reference to Fig. 3b, in the first phase, SAMPLE and $HOLD_1$ are high while $HOLD_2$ is low. Let the input to the DDS circuit v_{in} =

v_1 in this phase. Capacitors C_1 and C_2 store charges ($v_1 - v_{inv}$) and ($v_{ref} - v_{inv}$) respectively where v_{inv} is the inversion point of the amplifier. In the next phase, SAMPLE and $HOLD_1$ go low while $HOLD_2$ goes high. Let the input to the DDS circuit $v_{in} = v_2$ in this phase. Now, the charges stored in C_1 and C_2 are ($v_2 - v_{inv}$) and ($v_{out} - v_{inv}$) respectively. This follows from the fact that during the transition between the two phases, the input node of the amplifier is effectively floating and can not change. Due to conservation of charge, and assuming $C_1=C_2=C$, we can write:

$$C(v_1-v_{inv})+C(v_{ref}-v_{inv})=C(v_2-v_{inv})+C(v_{out}-v_{inv}) \quad (4)$$

which simplifies to:

$$v_{out}=v_{ref}-(v_2-v_1) \quad (5)$$

Thus the circuit effectively computes the difference between voltages applied to its input at two phases, offset by a bias v_{ref}. The following section describes how the circuit computes the light dependent signal generated by the pixel.

C. Peripheral Circuit Operation

Figure 3c shows a timing diagram for the peripheral circuits and serves to illustrate the readout sequence of the entire array including pixel addressing, DDS operation and output multiplexing. Prior to the times shown in the diagram, the row and column ring counters are loaded with a single 1 at the LSB position. Consider an arbitrary starting point, t_1. The rising edge of ROWCLK causes the row ring counter to increment and select the *ith* row of the array by setting RS_i high. The CTIAs of all the pixels in row *i* are now complete and their outputs are connected to the respective column level DDS inputs. Following this, SAMPLE is pulsed high which constitutes the first phase of the DDS operation, storing pixel outputs after photocurrent integration in addition to the pixel reset value. Next, non-overlapping clocks $HOLD_1$ and $HOLD_2$ are inverted leading to the second phase of DDS operation where the computation of equation 5 is performed. Now the output of each DDS circuit reflects the difference between the integrated photocurrent and the subsequent reset value. While this is similar to corelated double sampling (CDS) [30] which reduces reset noise, DDS operation adds to the noise since consecutive reset levels may not be the same.

By virtue of the single 1 loaded into the column ring counter, the output of the 132 to 1 multiplexer is equal to the DDS output of the first pixel in the *ith* row. This value is read out by an off chip analog-to-digital converter (ADC). Next, 132 pulses on COLCLK allow the sequential acquisition of all the pixels in that row. Finally the HOLD clocks are inverted again and ROWCLK is pulsed leading to the deselection and selection of the *ith* and the *(i +1)th* row, respectively. This cycle is repeated 124 times at the end of which the entire array has been read out. It follows that the integration time is $124t_{row}$ where $t_{row} = t_2 - t_1$. Without a mechanical shutter, this imposes a lower limit of the exposure time dependent on ADC speed.

D. Noise Analysis

Photodetector noise comprises of several sources [31]. Temporal noise sources include shot noise, reset noise and read noise. Shot noise is inherent in the production of photons from any source. Reset noise is the noise sampled onto the photodiode capacitance during pixel reset. Read noise is composed of thermal and flicker noise in the readout chain of the array. Spatial noise originates from fabrication mismatches across the array. This can manifest as an offset or a gain error. Since the active reset employed minimizes reset noise [25], the dominant temporal noise source is the read noise.

The primary read noise contribution is from the CTIA formed by M1, M2, M6 and M7 with noise from M1 dominating. At the designed transconductance and bias current of M1, thermal noise dominates over shot noise. The input referred noise power spectral density of a transconductance amplifier is given by [32]:

$$v_{n,i}(f)=\frac{\alpha 2kT}{g_m} \quad (6)$$

where k, T and g_m are the Boltzmann constant, absolute temperature and the amplifier transconductance respectively. α is a constant between 2/3 and 2 depending on the amplifier design. Considering the low frequency small signal equivalent circuit of the CTIA shown in Fig. 5, the output referred noise power is:

$$v_{n,o,rms}^2=\int_{-\infty}^{+\infty} v_{n,i}^2(f)|H(f)|^2 df \quad (7)$$

Where $H(f)$ is the transfer function of the CTIA. From Fig. 5, we can write:

$$v_x-v_i=v_o\frac{C_{fb}}{C_{fb}+C_{pd}} \quad (8)$$

$$sC_{pd}(v_x-v_i)+g_m v_x+v_o(1/r_{out}+sC_l)=0 \quad (9)$$

where C_l is the parasitic load capacitance driven by the CTIA. The equation simplifies to:

$$H(f)=\frac{v_o}{v_i}=\frac{-g_m}{\frac{1}{r_{out}}+\frac{g_m C_{fb}}{C_{fb}+C_{pd}}+s\left(C_l+\frac{C_{fb}C_{p\,d}}{C_{fb}+C_{pd}}\right)} \quad (10)$$

Recognizing $H(f)$ to be of the form $a/(b+jcf)$ and recalling:

$$\int\left|\frac{a}{b+jcf}\right|^2 df=\frac{a^2}{c^2}\int\frac{df}{\left(\frac{b}{c}\right)^2+f^2}=\frac{a^2}{bc}tan^{-1}\frac{fc}{b}$$

equation 7 can be simplified to:

$$v_{n,o,rms}^2=\frac{\alpha kT g_m}{\left(\frac{1}{r_{out}}+\frac{g_m C_{fb}}{C_{fb}+C_{p\,d}}\right)\left(C_l+\frac{C_{fb}C_{pd}}{C_{fb}+C_{pd}}\right)} \quad (11)$$

Assuming $g_m r_{out} \gg C_{pd}/C_{fb} > 1$ (note that this is the same assumption made earlier in Sec. III-A with the CTIA open loop gain being $g_m r_{out}$), we have:

$$v_{n,o,rms}^2=\frac{\alpha kT}{\left(\frac{C_{fb}}{C_{fb}+C_{pd}}\right)\left(C_l+\frac{C_{fb}C_{pd}}{C_{fb}+C_{pd}}\right)} \quad (12)$$

From eqs. 3 and 12, the SNR $v_{out}/v_{n,o,rms}$ is monotonically increasing for decreasing C_{fb}. However, reset noise and mismatch limit the minimum C_{fb} that can be implemented. Based on prior measurements from test structures, we chose C_{fb}=5 fF. With C_f=1 pF, C_{fb}=5 fF,

C_{pd}=250 fF and α=1.5, the output referred rms noise voltage due to read noise is about 560 μV at 300 K.

IV. Results

The 124 × 132 imager array was fabricated in a 0.5 μm 3-metal, 2-poly CMOS process. Figure 6 shows the annotated micrograph of the chip. The die size was 3 mm × 3 mm. Area excluding the pads was 7.88 mm^2 with the pixel array occupying 6.61 mm^2, the column scanner occupying 0.67 mm^2 and the row scanner occupying 0.24 mm^2. Pads were confined to two sides to maximize area usage.

A. Characterization

For characterization, a microcontroller (Microchip, Chandler, AZ) was used to generate all control signals. Independent 3.3 V regulators were used to power the analog and digital supplies of the chip. Off chip biases were generated by a 12 bit digital-to-analog (DAC) chip. The analog output of the chip was buffered using a unity gain amplifier and digitized to 16 bits at 1.5 MHz with a data acquisition card (National Instruments, Austin, TX) and read into a computer for analysis.

Figure 7 shows an oscilloscope plot illustrating the raw output of a pixel without delta differencing. Signals RESET and ROWCLK are also shown. Prior to the trigger point, the pixel in the first row and column is selected, completing its CTIA. During the first 100 μs after the trigger, the pixel was reset with the output going to the inversion point of the CTIA. Then RESET was released and the positive slope of the pixel output can be seen. Following this, ROWCLK is pulsed, disconnecting the CTIA of the first pixel, and completing the CTIA of the second pixel in the column. Immediately afterwards RESET goes high sending the output to the inversion point of the CTIA in the pixel in the second row, first column. Next ROWCLK is pulsed 122 times, with the *ith* pulse disconnecting the CTIA in the *(i+1)th* and connecting it in the *(i+2)th* row. During this period, the output of the pixels can be seen to remain at the inversion point of the respective amplifiers. Finally RESET goes low and there is one more pulse on ROWCLK which disconnects the CTIA in the 124th row and connects the CTIA of the pixel in the first row, first column again. The output can be seen to follow the same linear trajectory as seen before scanning. This confirms the linear photo-response of the pixel and the row scanning operation.

Figure 8 shows the output of all the column level DDS circuits in response to three different light levels - 0 or dark, I_0 and $2I_0$. I_0 was an arbitrary intensity and I_0 is derived from $2I_0$ using a OD 0.3 neutral density filter inserted in the optical path. After removing the 240 mV offset in an off-chip calibration step, the DDS output can be seen to double from 190 mV to 380 mV in response to light intensity increasing by a factor of two, indicating proper delta differencing. Column scanner operation can also be seen as the DDS output remains stable as all the pixels in a row are scanned by pulsing COLCLK. One would expect the output of all the pixels to be the same as they were under flat-field illumination.

While the results presented so far focus on the operation of a single pixel and the DDS circuit, we now show measurements from the entire imager array. Figure 9 shows the average digitized output of all the pixels in the chip for increasing light intensities measured by a radiometer. The imager was run at 70 fps with an exposure time of 14.3 ms. A blue light emitting diode centered at 450 nm, driven by a constant current source, was used to illustrate the chip. A diffuser was used to generate flat-field illumination. A blue LED was chosen to get a lower limit of the imager performance. From spectral response measurements of the pixel [26], at 450 nm, the photodiode sensitivity is about 65% of the peak sensitivity at 650 nm.

Figure 10 shows the average signal-to-noise ratio (SNR) of the array measured for the same intensities. Average SNR was defined as:

$$SNR = \frac{\left(\sum_1^N \mu_i\right)/N}{\left(\sqrt{\sum_1^N \sigma_i^2}\right)/N} \quad (13)$$

where N is the number of pixels. μ_i and σ_i are mean and standard deviation of the output of the *ith* pixel calculated over a thousand frames. To characterise the entire array, signal contributions of each pixel were added in phase and the noise contributions were added in quadrature. As can be seen, at 70 fps the minimum detection limit is about 4 nW/cm^2, which compares favorably with several recent low-intensity imagers shown in Table I. The peak SNR of 44 dB at 1 μW/cm^2 is likely limited due to the small full-well capacity imposed by the 5 fF sense node capacitance. Factoring in the pixel area and the exposure time, the limit corresponds to 36.4 photons/ms/pixel, suitable for single cell fluorescence imaging [19].

The dark signal was measured over an exposure of 1 s with a response of 742.2 ADC counts. This implies a dark signal of 113 mV/s. Using eq. 3 and our pixel area of 4.04×10^{-6} cm^2, this equates to a dark current density of 0.14 nA/cm^2. Comparing the dark signal with the saturation value from Fig. 10, the imager will saturate in darkness at integration times longer than 3 s. This limit can be extended if a low dark current, imager optimized CMOS process is used instead of the standard mixed-signal 0.5 μ process used here.

At 75% of saturation, fixed pattern noise (FPN) of the entire array was 0.84%. The FPN was calculated as the mean of the standard deviations of all the pixels computed over a thousand frames at an intensity of 0.5 μW/cm^2. FPN of pixels within a single column that share the p transistors of the CTIA and the DDS circuit was 0.66%. The corresponding numbers for 0% saturation were 0.99% and 0.86%. The FPN is relatively high due to the use of very small feedback capacitance (~5 fF) in a 0.5 μ technology where the recommended size of well matched capacitors is 100 fF [29]. Any mismatch in the in-pixel photodiodes and feedback capacitors, and the column parallel DDS circuits will manifest as FPN.

The measured output referred read noise was 824 μV. The corresponding input referred noise is lower by a factor given by the CTIA gain. Using eq. 3, the input referred charge noise was estimated to be 26 e$^-$. To estimate the reset noise, we made use of the fact that each reset sample comprises of a fully correlated reset noise and an uncorrelated read noise [31]. By analyzing several instances of two consecutive reset samples, the read noise can be estimated. From a thousand reset frames, we calculated the output referred reset noise to be 192.9 μV which corresponds to a input referred noise of 6 e$^-$.

With respect to CCD detectors, binning is a process in which the outputs of several pixels are combined before they are read off chip, effectively creating larger photosites. The purpose is to trade off spatial resolution for increases in sensitivity and frame rate. Binning could be implemented in our detector by skipping rows and columns during the readout phase and not resetting the skipped photodiodes. Once those photojunctions saturate, the photoinduced electrons can diffuse to the junctions that are not being skipped, effectively increasing the size of each photosite. Figure 11a shows the effect of 4×4 binning on the sensitivity and the SNR of the chip. The maximum frame rate increased to 675 fps from the earlier maximum of 70 fps. Alternately, if the frame rate was kept at 70 fps, the detection limit could be reduced to about 0.8 nW/cm^2. Figure 11b–d show the effect of binning on spatial resolution. From left to right, the images are at the native resolution (132×124, t_{exp}=14.3 ms, 70 fps), 2×2 binning (66×62, t_{exp}=4.44 ms, 225 fps) and 4×4 binning (33×31, t_{exp}=1.48 ms, 675 fps), respectively.

At 70 fps, the chip consumes a total of 718 μA of current from a 3.3 V supply leading to a power draw of 2.37 mW. Digital circuitry including pixel scanners and clock generation consumes 58 μA while the pixel array, DDS circuits and bias generation circuits consume 660 μA.

Table I shows a comparison of several recently published low-intensity CMOS imagers designed for biomedical applications. The detection limits were reported at different SNR, incident wavelengths and exposure times. The table shows the incident intensity and the number of photons required by each of the detectors to achieve the reported SNR. For comparison, we measure how many photons our detector needs to achieve the same SNR at the reported wavelength. We also calculate the incident intensity required by our imager to equal the reported SNR after scaling our pixel area and exposure time to match the reported values. These data are shown in Table II The calculations were performed using the measured SNR *vs.* intensity curve (Fig. 10) and the spectral sensitivity of n-well/p-sub photodiodes fabricated in the 0.5 μ CMOS process used [26]. Standard luminosity functions [33] were used to convert from units of lux to W/cm^2.

B. Fluorescent imaging

Figure 12 shows images of mouse spinal cord neurons with immunostained neurofilament, a structural protien found in neurons. The primary antibody used for labelling was SMI-32 which binds to non-phosphorylated neurofilament [35] and the secondary antibody was conjugated to a fluoroscent cyanine dye, Cy-3. Neurofilaments play a role in controlling axonal diameter and nerve conduction velocity. Abnormalities in the protein leads to phenotypes similar to amyotrophic lateral sclerosis (ALS) [36].

Figure 12a was taken with a cooled CCD camera [34], the standard in biomedical imaging while Fig. 12b is from the imager designed in this work. Since the CCD pixels are smaller than the CMOS pixels (6.45 μm *vs.* 20.1 μm), CCD data was binned for a fair comparison. The images were taken at a magnification of 20× through a Nikon epi-fluorescent microscope with a constant incident intensity and an exposure time of 36 ms for both detectors. Figure 12c compares the average SNR of the two imagers computed using eq. 13 for regions of different saturation levels within each image in order to compare performance in both bright and dark regions of one image.

The sensitivity and the SNR performance of the imager is comparable to the cooled CCD camera in both light and dark areas of the image. However, the CCD detector has better performance in the dark areas of the image (saturation $\prec$ 40%) due to its shot noise limited nature and low dark current. Our detector is limited by read noise due to relatively high noise from the high gain CTIA, which was required to boost the sensitivity. Migrating to an imager optimized process with higher quantum efficiency should relax the requirement on the amplification. The CMOS imager achieves a higher frame rate than the CCD, 28 fps *vs.* 20 fps, due to global shuttering.

V. Conclusions

We presented a high sensitivity image sensor fabricated in a standard, *non imager optimized*, 0.5 μ CMOS process. With a 20.1 μm pixel size and a frame rate of 70 fps, the imager was capable of detecting down to 4 nW/cm^2 of 450 nm light while consuming 2.37 mW. Inclusion of a capacitive transimpedance amplifier allows the enhanced sensitivity while controlling the reset noise. Binning was implemented to increase frame rate (to 675 fps) or sensitivity (to 0.8 nW/cm^2 at 70 fps) at the cost of spatial resolution. We were able to image fluorescence down to single cell level with sensitivity and signal to noise ratio comparable to cooled CCD cameras.

This work was geared towards applications that require the best of both worlds, the sensitivity and low light performance of CCDs and the power requirements, modularity and system-on-chip capability of CMOS detectors. In particular, we are integrating the presented detector with a miniaturized microscope to create a system that combines illumination, optics and photodetection [11]. The power characterstics of the imager allow battery operation and the high sensitivity and SNR performance will permit the creation of a small footprint device that can be attached to a rat skull and used to chronically image the brain in awake and behaving animals. The lack of optical fiber or electrical cables will allow tether-free operation enabling a wide range and duration of imaging studies. Such a device may extend our understanding of structural changes in the brain with normal development or in response to abnormal pathologies. Also, using optical functional imaging techniques such as voltage sensitive dyes [4], calcium dyes [5] or laser speckle [37], one can probe neuronal and vascular activity in relation to behavioral activity. In closing, we expect the CMOS imager presented here to be an integral component of miniaturized systems enabling imaging studies in freely-moving animals without any restraints.

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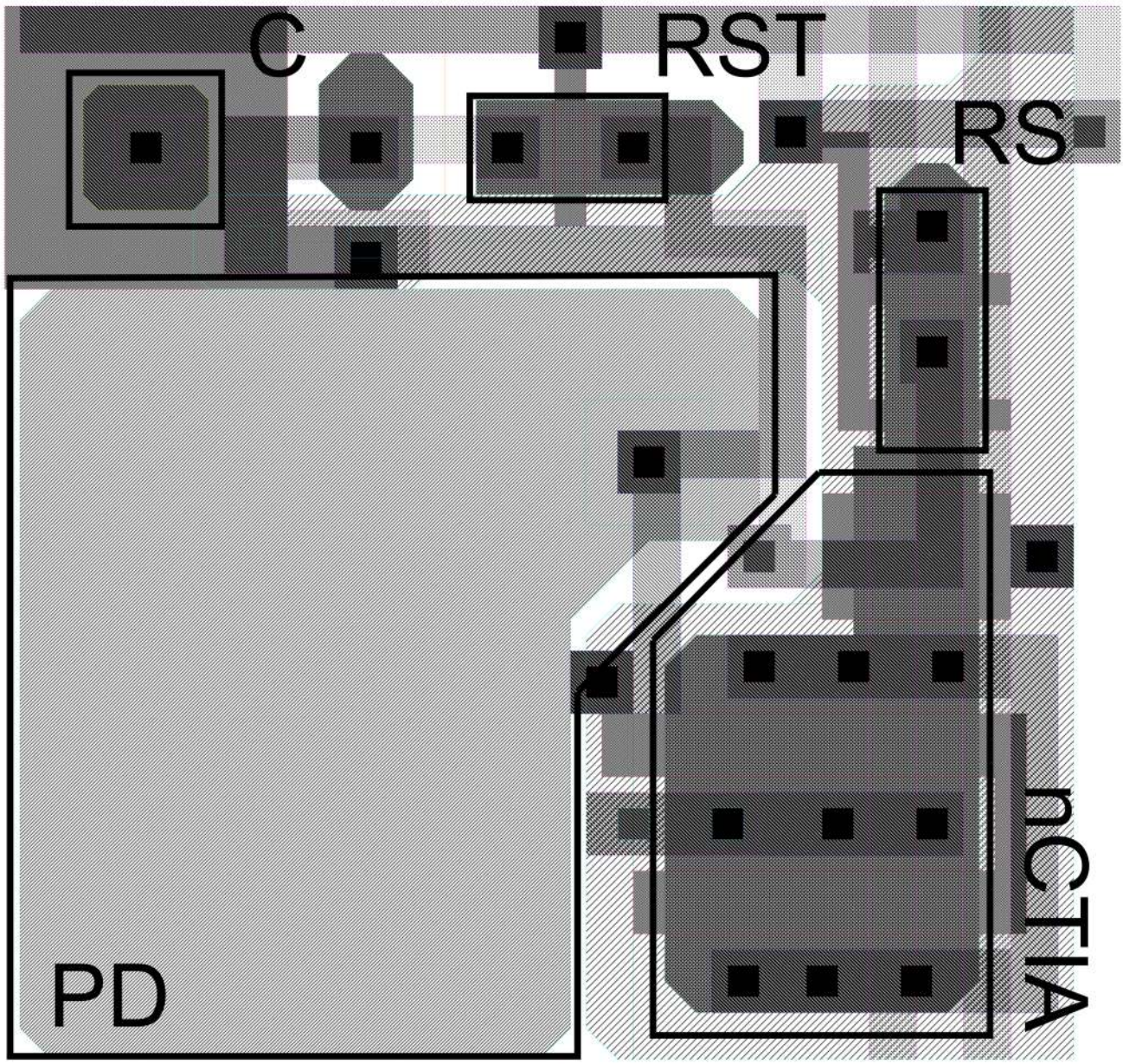

Fig. 1.
Layout of the pixel showing the photodiode (PD), nMOS transistors of the CTIA (nCTIA), the feedback capacitor (C) and the row select (RS) and reset (RST) transistors.

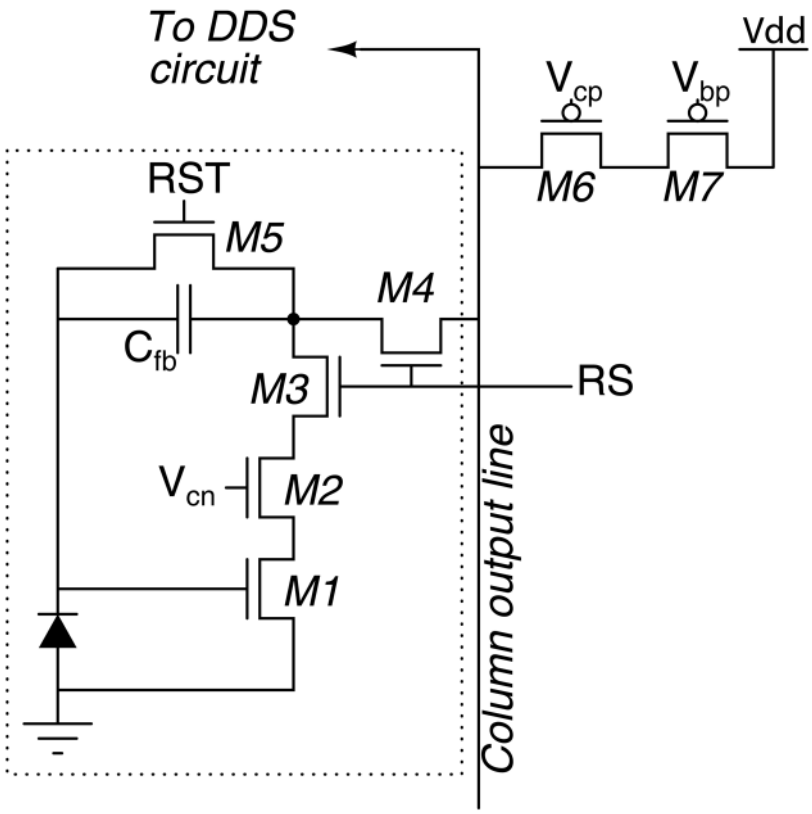

Fig. 2.
Schematic of the nMOS-only pixel circuit (within dotted line), also showing the column level pMOS transistors.

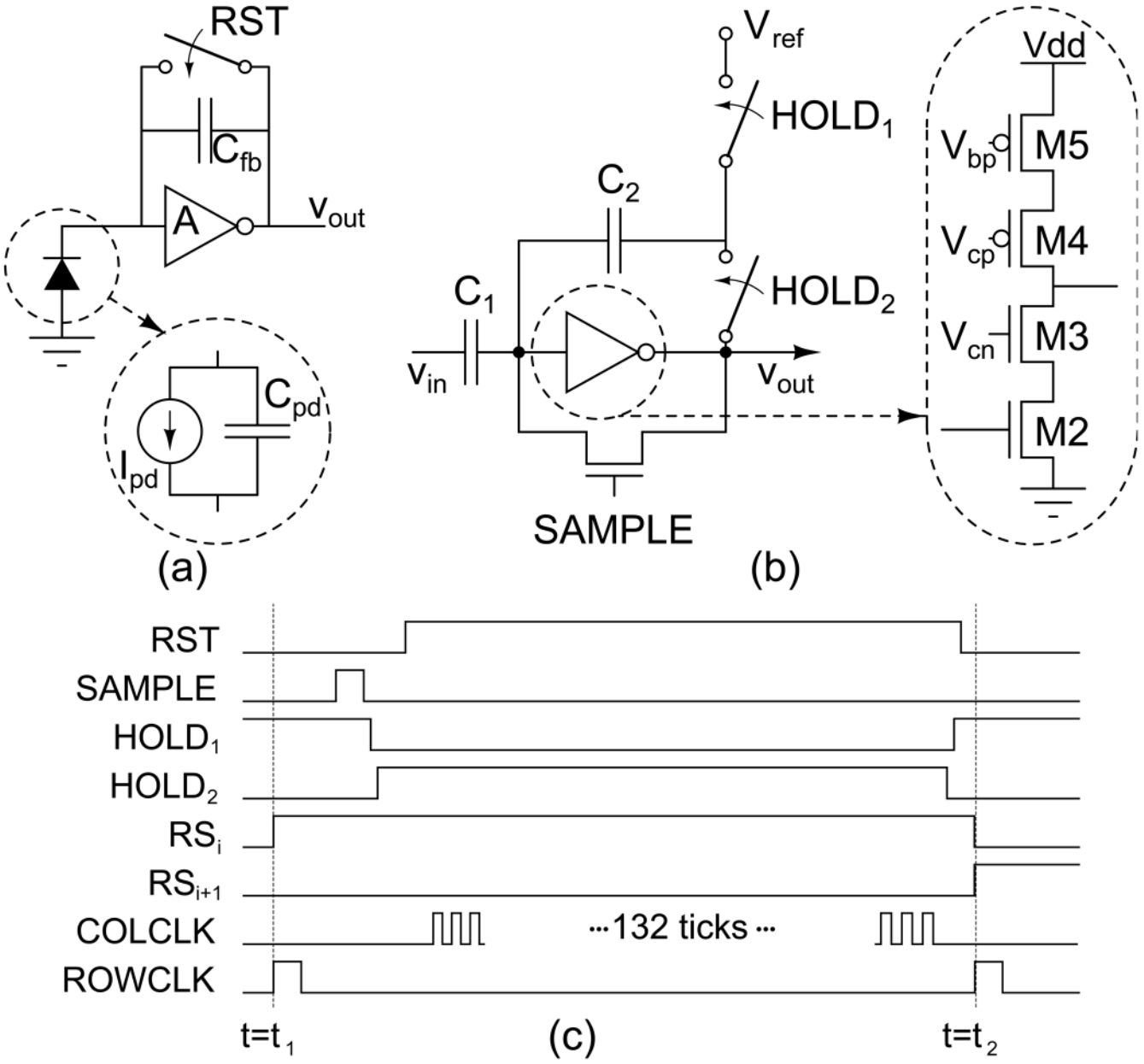

Fig. 3.

(a) Simplified schematic of a pixel when its row is selected and the CTIA is completed. (b) Schematic of the column parallel delta difference sampling (DDS) circuit. Biases V_{cn}, V_{cp}, V_{bp}, and V_{ref} generated on-chip and separate from CTIA biases in Fig. 2. (c) Timing diagram showing the readout sequence of the entire array including pixel addressing, DDS operation and output multiplexing.

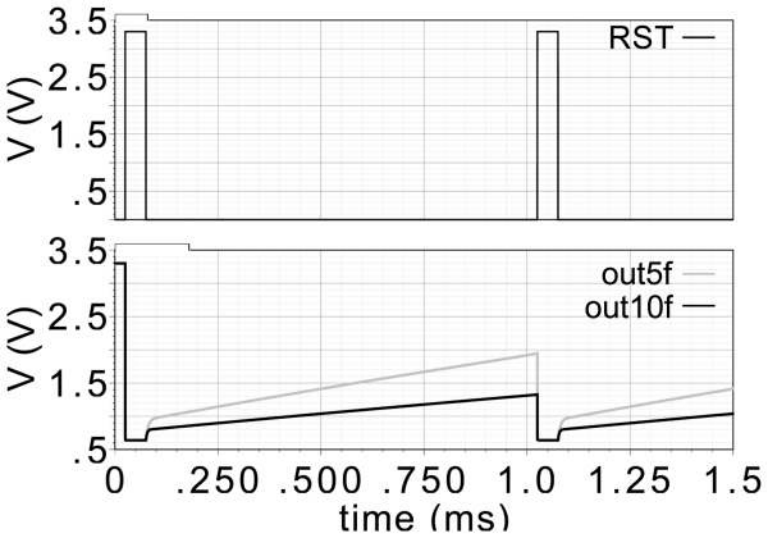

Fig. 4.
Simulation of the pixel circuit with C_{pd}=150 fF, I_{pd}=6 pA, and C_{fb}=5 fF (out5f) and 10 fF (out10f).

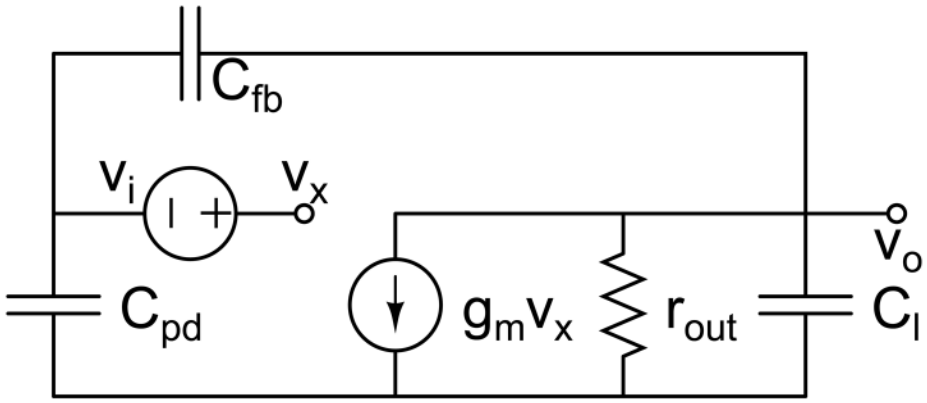

Fig. 5.
Low frequency small circuit equivalent circuit for the CTIA used to compute the forward transfer function.

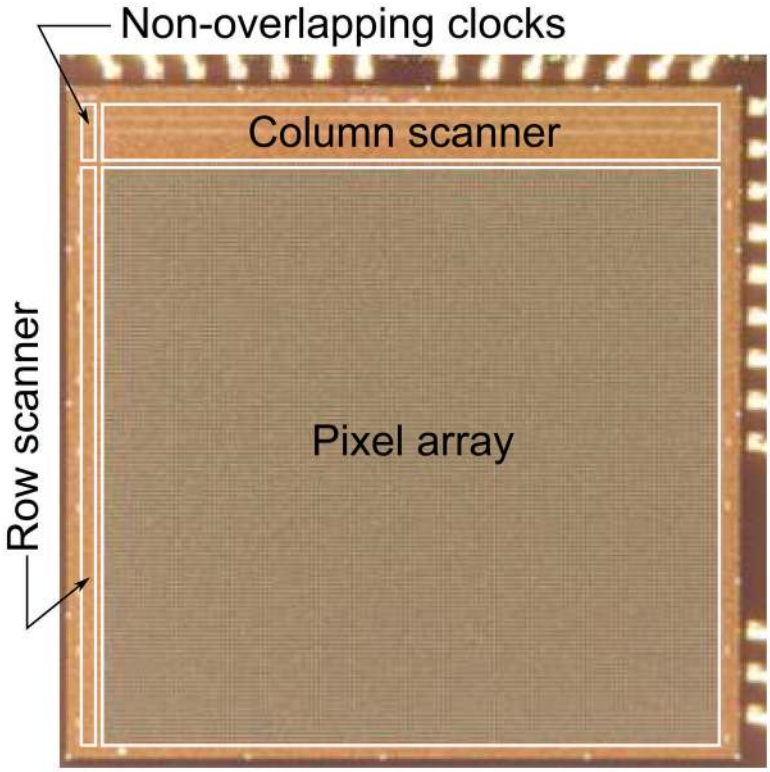

Fig. 6.
Annotated micrograph of the 3 mm × 3 mm chip showing the pixel array, row and column scanners and clocking circuits.

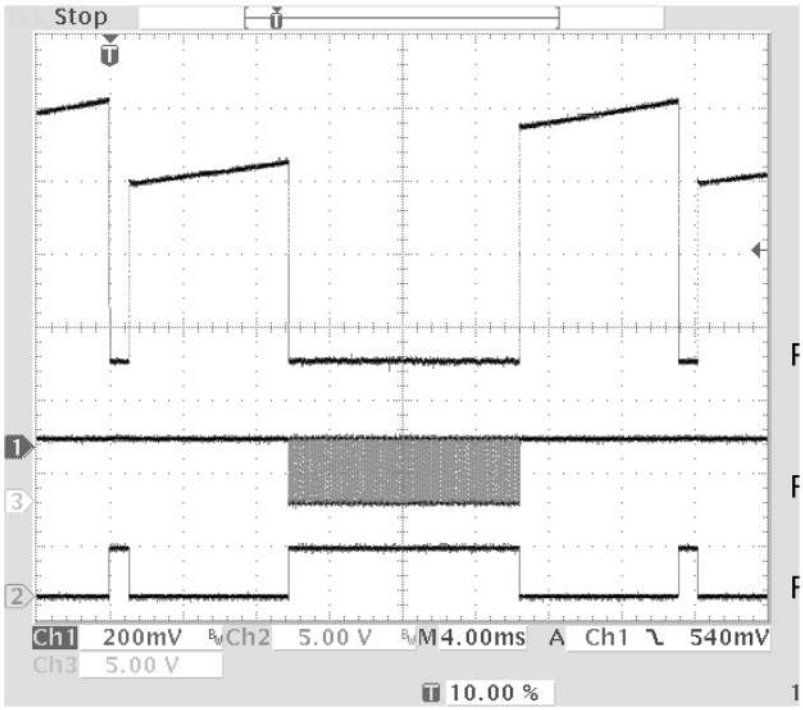

Fig. 7.
Oscilloscope plot showing the raw output of one of the pixels. As expected, scanning and resetting other rows during the exposure period does not affect the pixel operation.

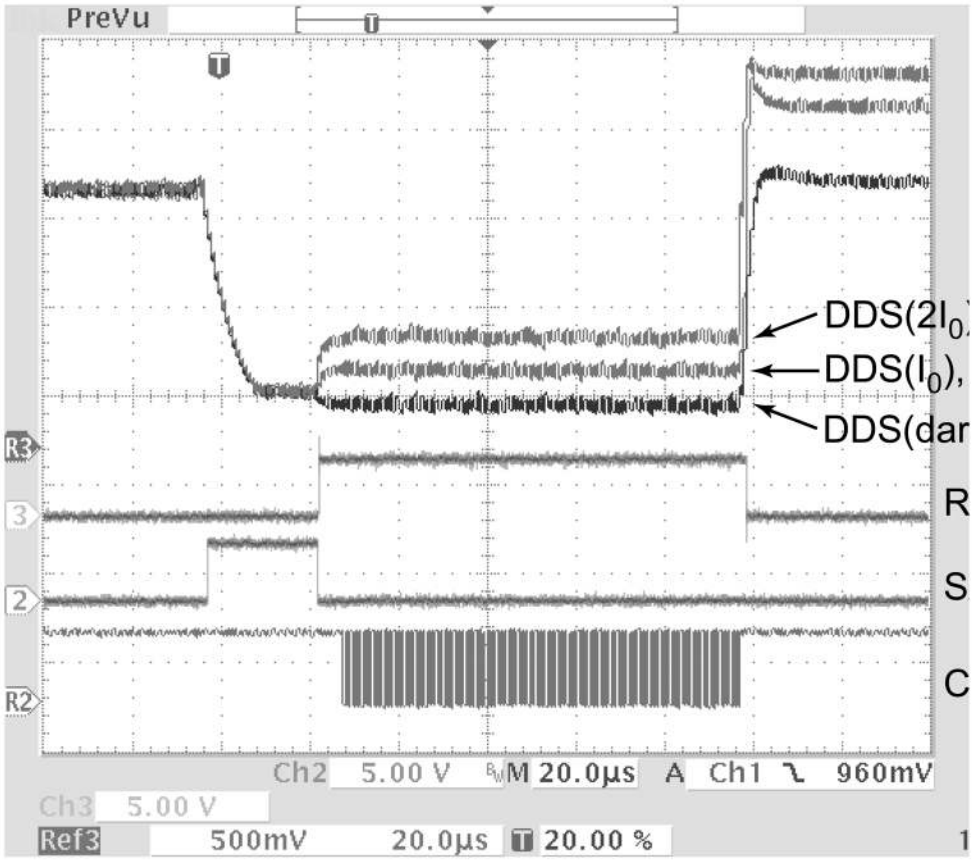

Fig. 8.

Oscilloscope plot showing DDS and column scanning control signals and operation for three light levels - dark, I_0 and $2I_0$. Traces marked DDS represent the output of an entire row of pixels scanned by the column scanner.

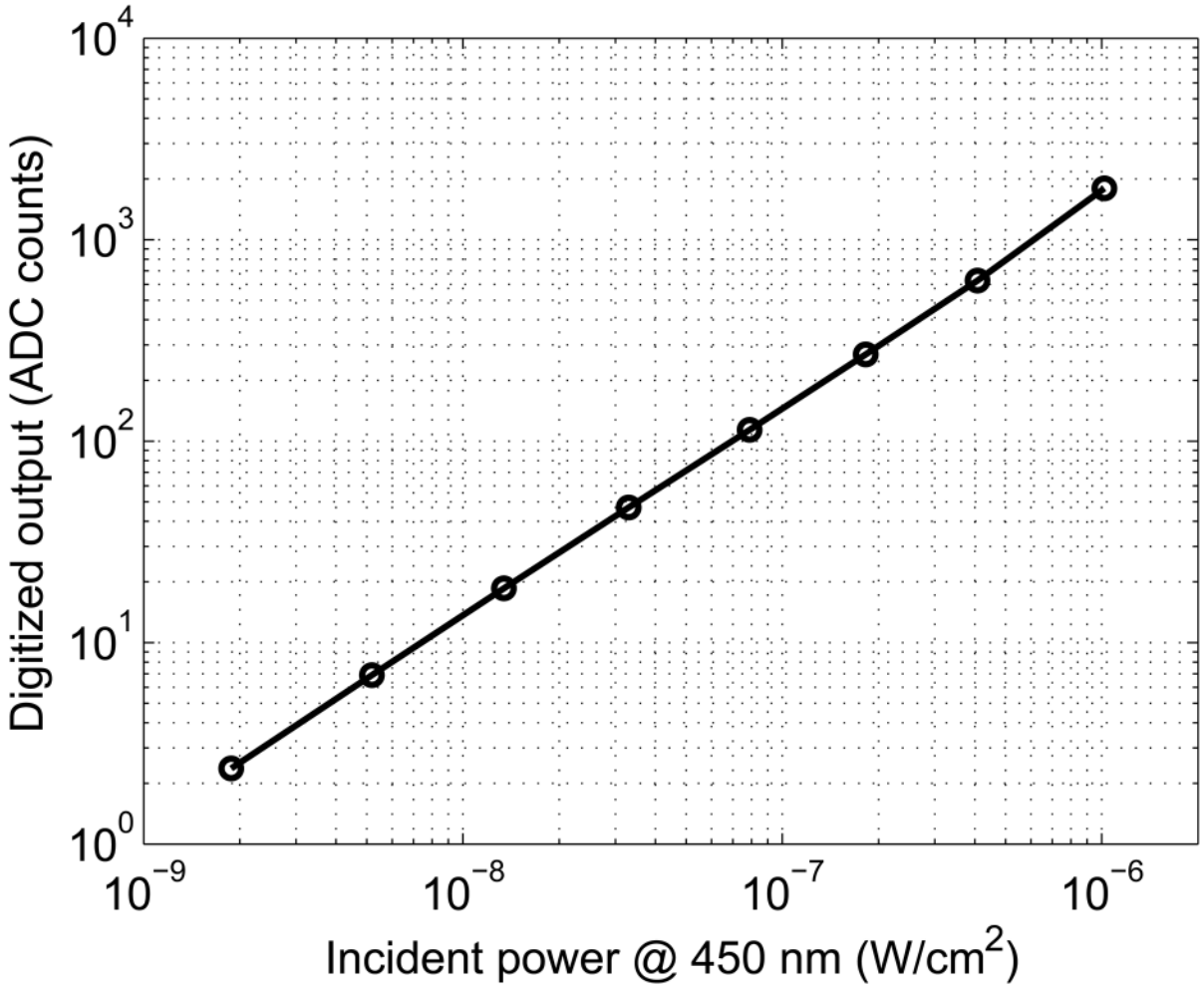

Fig. 9.
Average digitized output of all pixels in the array over 1000 frames with a 14.3 ms exposure time (70 fps) for increasing 450 nm light intensity.

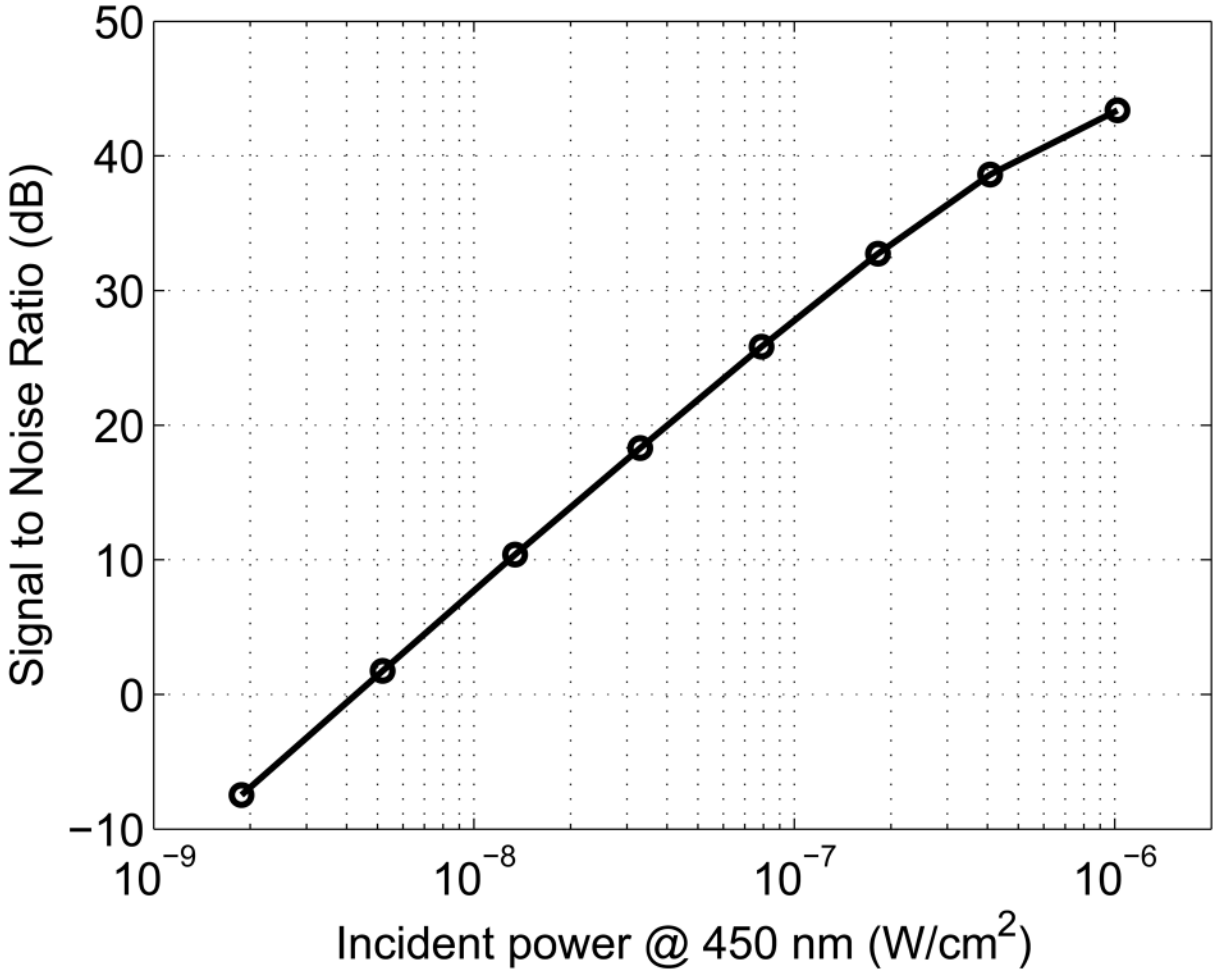

Fig. 10.
Average SNR of all pixels in the array over 1000 frames with a 14.3 ms exposure time (70 fps) for increasing 450 nm light intensity.

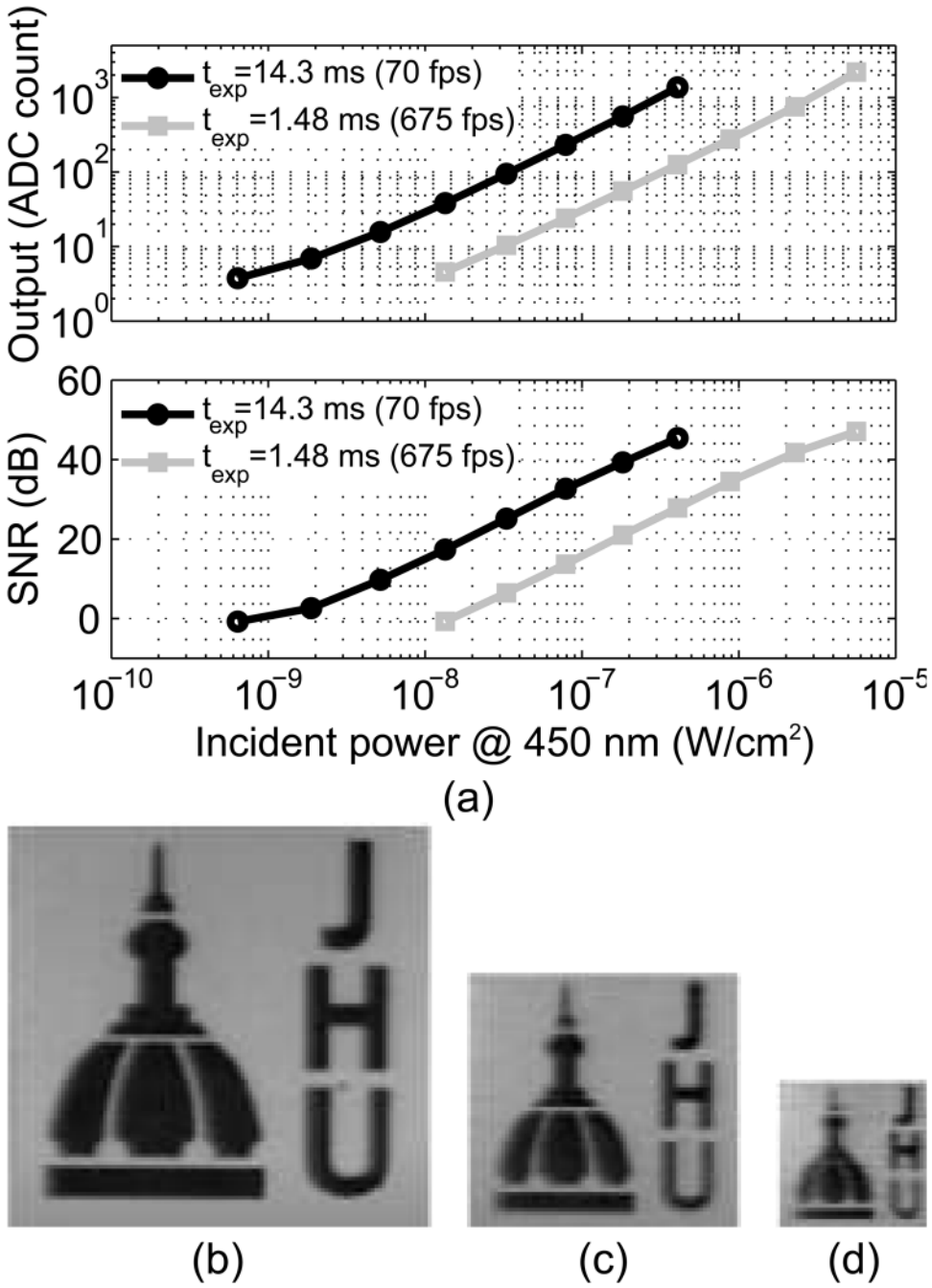

Fig. 11.

(a) Increased frame rate or sensitivity achieved by 4×4 binning, (b) native resolution image at 70 fps, (c) 2×2 binned image at 225 fps and (d) 4×4 binned image at 675 fps

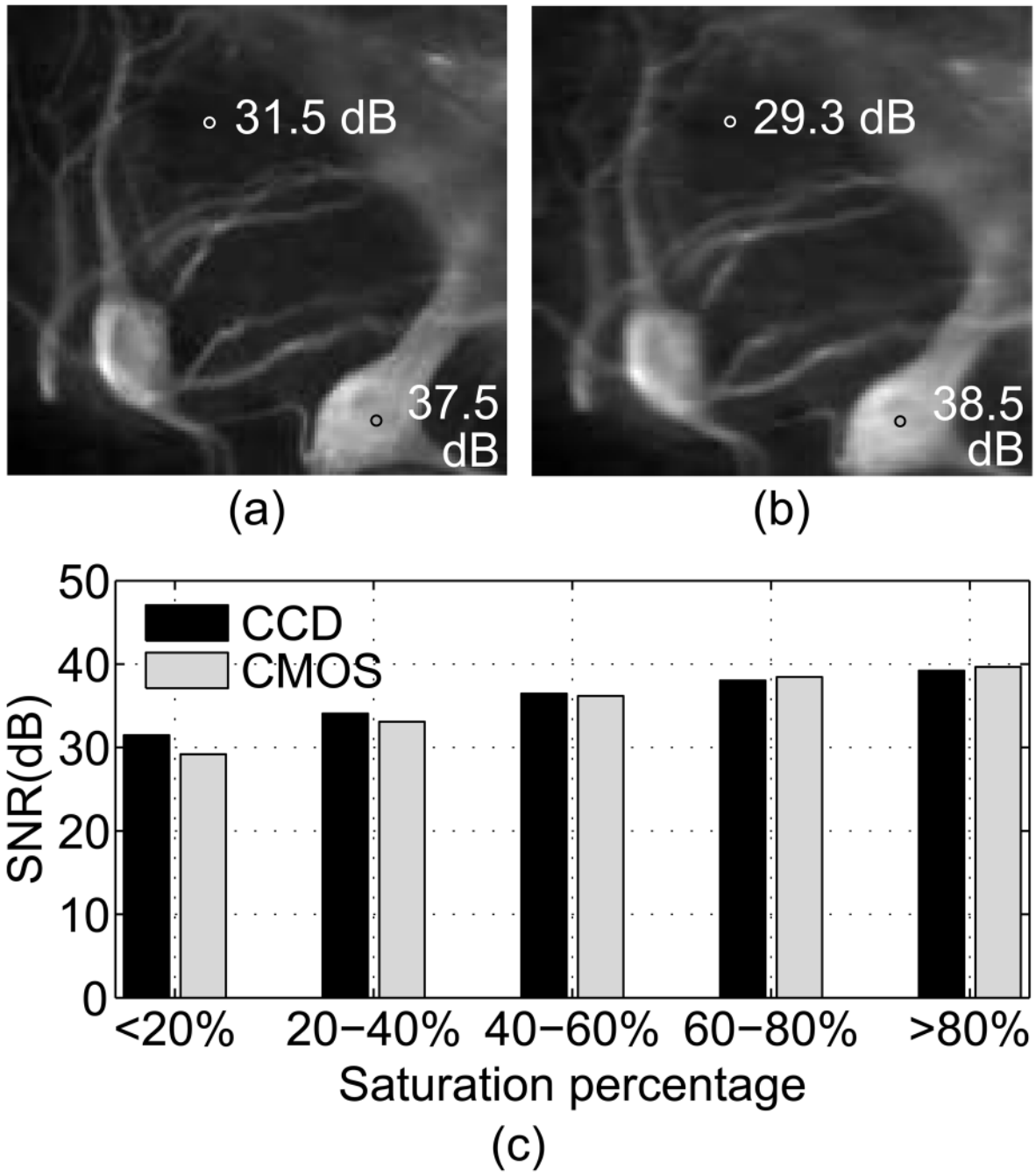

Fig. 12.
Images of mouse spinal cord neurons fluorescently labeled by a Cy-3 conjugated antibody to neurofilament taken by (a) a cooled CCD camera [34] and (b) the imager presented in this work. Annotations indicate measured SNR in indicated regions. (c) shows average SNR for different saturation levels for both detectors.

TABLE I

Comparison of low-intensity CMOS imagers

	[20]	[21]	[22]	[23]	This work
Chip resolution	176×144	8×16	128×128	32×32	132×124
Pixel size	7.5 μm×7.5 μm	240 μm×210 μm	7 μm×7 μm	75 μm×75 μm	20.1 μm×20.1 μm
CMOS technology	0.35 μ	0.18 μ (custom)	0.18 μ	0.5 μ	0.5 μ
Dark frame FPN	–	–	0.16%	4.16%	0.99%
Reported detection limit					
SNR	0 dB	0 dB	15 dB	35.2 dB	0 dB
Wavelength	470 nm	562 nm	450 nm	–	450 nm
Exposure (frame rate)	3.2 s (0.3 fps)	30 s (0.03 fps)	33 ms (30 fps)	25 ms (40 fps)	14.3 ms (70 fps)
Intensity	100 nW/cm^2	0.1 pW/cm^2	400 nW/cm^2	2.9 μW/cm^2	4 nW/cm^2
Photon count	4.2×10^5	4.3×10^3	1.4×10^4	1.1×10^7	5.2×10^2

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TABLE II

Calculated intensity and photon count required by this work to match parameters specified in [20]–[23]

	[20]	This work
Intensity	100 nW/cm^2	0.11 nW/cm^2
Photon count	4.2×10^5	5.4×10^2
	[21]	This work
Intensity	0.1 pW/cm^2	0.01 pW/cm^2
Photon count	4.3×10^3	6.5×10^2
	[22]	This work
Intensity	400 nW/cm^2	80.2 nW/cm^2
Photon count	1.4×10^4	3.0×10^3
	[23]	This work
Intensity	2.9 μW/cm^2	14.2 nW/cm^2
Photon count	1.1×10^7	4.1×10^4