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A CMOS Magnitude/Phase Measurement Chip for Impedance Spectroscopy

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***Abstract*—The measurement of electrical impedance is used in a plethora of biomedical applications. The most common technique used is the synchronous demodulation method, which provides the real and imaginary parts of the impedance. However, in practice, the method requires elaborate calibration and matching between the injection and monitoring stages. This paper presents the integrated realization of an alternative method that is less intricate to implement. The circuit was fabricated in a 0.35-μm CMOS technology, occupies an active area of 0.4mm^2 and dissipates about 21mW of power from ±2.5V supplies. The chip was used to measure equivalent RC circuits of the electrode-tissue interface over the frequency range of 50 Hz to 100 kHz, showing a good correlation with the theoretical results.**

***Index Terms* — CMOS, biosensor, comparator, instrumentation amplifier, impedance spectroscopy, synchronous detection, magnitude phase measurement.**

I. Introduction

THE measurement of impedance over a frequency range, also known as electrical impedance spectroscopy (EIS) is used in a plethora of applications, including bioimpedance analysis [1] and impedance cardiography [2] for patients undergoing dialysis and stroke patients respectively. When used for electrical impedance tomography (EIT), applications include continuous lung monitoring [3], tumor detection [4] and brain function imaging [5]. EIS is also used in lab-on-a-chip biosensing applications for the detection of proteins, single-stranded DNA hybridization [6], common allergens [7] and bacteria [8] as well as impedance flow cytometry [9].

Ideally, impedance measuring (or *impedimetric*) systems employ measurements of ac voltage following the injection of ac current (adhering to medical safety limits, e.g. 5mA$_{p-p}$ at 50 kHz [5]). Some applications require measurements over a wide frequency spectrum (up to a few MHz). However, the design of high frequency voltage controlled current sources (VCCSs) is a challenging task [10] because high output impedance is needed to ensure current amplitude accuracy independent of the load impedance value. Consequently, the few commercial current drivers available are bandwidth limited (e.g. up to 100 kHz in [11]). Alternatively, a voltage can be applied and the injected current measured, as often done in biosensor applications [6-9] employing commercial impedance analyzers. However, voltage output bio-interfacing is considered less safe, as the risk of tissue damage is higher [12], since there is no control over the current injected, because the load is not constant.

Our group develops custom integrated circuits (ICs) for EIS and EIT systems. Using custom IC implementations also offers the opportunity to overcome some of the dominant instrumentation issues degrading performance in common techniques (see below), and it allows for portable/implantable and for lab-on-a-chip realizations.

The most common impedimetric technique is *synchronous detection* (SD), see Fig. 1. Preamplified by an instrumentation amplifier (IA), the measured potential is multiplied with a signal in-phase with the injected current and then low-pass filtered to obtain a dc level corresponding to the real part of the impedance. Similarly, multiplication with a 90° shifted signal provides the imaginary part. The main advantage of the technique is that it "locks" to the carrier frequency, without the use of band-pass filters.

However, in practice the method suffers from matching, offset and synchronization errors. Matching issues are important when two or more channels are used for simultaneous real and imaginary measurements and/or in multi-frequency systems. IC implementations are far superior in eliminating such errors. Inherent dc offsets at the output stages are also particularly detrimental as the outputs of SD are

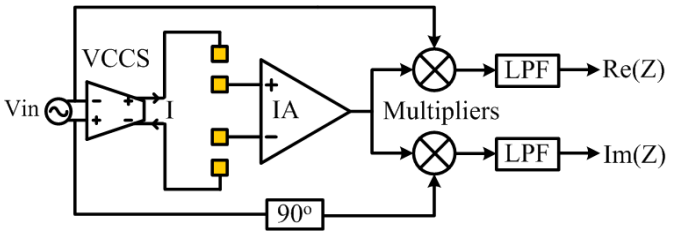

Fig. 1. Single frequency synchronous detection (also known as synchronous-, quadrature- or phase sensitive- demodulation and lock-in).

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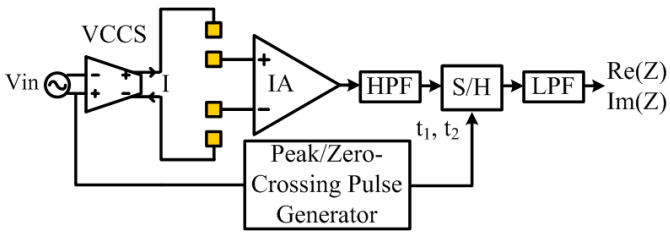

Fig. 2. Single frequency synchronous sampling.

dc voltages. The integrated solutions in [13] and [14] (two-frequency system) employed chopping to remove the dc offsets and utilized switching modulators/demodulators to perform both the SD and the chopping functions.

The greatest source of error in the SD method is related to the need for precise synchronization between the injecting and measuring stages. The signals are generated, for example, using quadrature oscillators and then fed (through a summing amplifier in multi-frequency systems) into a high output impedance VCCS. The demodulation signals are square waves generated by comparators from the oscillator outputs. All of these blocks will introduce different delays (time and phase). Thus phase errors between the demodulation carriers and the injected signal (or signals) are very difficult to avoid, resulting to an erroneous dc component in both real and imaginary outputs, which can be particularly detrimental in swept or multi-frequency applications as it differs in value for different carrier frequencies. Some correction can be provided through additional phase shifting circuitry, at the expense of an increase in complexity. However, this would usually be placed prior to the summing amplifier at the signal path and after the comparators at the demodulation path, hence failing to take the summer and VCCS phase contributions in consideration.

Another method for measuring impedance is synchronous sampling [15-16], where sampling of the measured signal at the time when the injected signal peaks and crosses zero allows the calculation of the real and imaginary parts (see Fig. 2). Offsets can be eliminated by averaging the samples of both positive and negative half-cycles and multi-frequency realizations can be implemented without the use of band-pass filters [16], similarly to SD. However, the analog implementation of SS [15] can be very challenging especially for high frequencies [15] as it requires very precise sampling timing and, as with SD, synchronization is a major degrading factor for both real and imaginary values.

Solutions to these synchronization limitations require appreciable increase in circuit complexity. Thus, in order to increase measurement accuracy, it is desirable to adopt circuit topologies that do not suffer from such issues.

In [17-20] the measurement of magnitude and phase has been proposed as an alternative to the abovementioned techniques. In [17] a discrete component magnitude/phase measurement system was presented using a gain-phase detector AD8302 IC from Analog Devices. The system performs division using log-domain subtraction of the injected signal across a known resistor minus the measured signal to extract the magnitude. A custom IC version of this system was proposed in [18]. If the VCCS was custom-designed with very high output impedance, complexity would be reduced as the amplitude of the injected current would remain constant throughout the bandwidth and the amplitude range applied, eliminating the need for the division of the two voltages. In this case, the calculation of the impedance magnitude would be independent from the source signal. In [19] the magnitude was found through a peak detector. While in [18] the voltage offsets of the logarithmic stage are considered, as in [19] the offsets associated with the IA are ignored. In [18] phase was measured using an XNOR gate, while in [19-20] square wave versions of the injected and measured signals were fed into an XOR gate. The calculation of the impedance phase still requires an in-phase reference easily generated on the measurement side through a sense resistor. Even though this resembles the in-phase demodulation carrier in SD and SS techniques, the reference signal in this case does not need to be fed to a phase shifter at the signal path to correct the systematic phase errors. Therefore complexity is greatly reduced relative to these methods.

In this paper we propose a new magnitude/phase measurement IC for EIS biosensing applications, where a single frequency at a time is applied. The system features low complexity, avoids synchronization issues, and eliminates IA offset errors not addressed in the aforementioned realizations. This paper presents an integrated solution based on the principles of the discrete system recently presented in [20]. The remaining sections of the paper are organized as follows. Section II describes the proposed magnitude/phase measurement system and the basic equations relating the measured signals to the impedance being measured. Section III describes the circuits of the individual system blocks. Section IV presents measured impedance magnitude/phase responses of an electrode-tissue interface RC equivalent circuit, obtained using the fabricated chip. The conclusion of Section V completes the paper.

II. New Magnitude/Phase Measurement System

The schematic diagram of Fig. 3 shows the proposed magnitude/phase measurement system, which utilizes fully-differential signaling throughout.

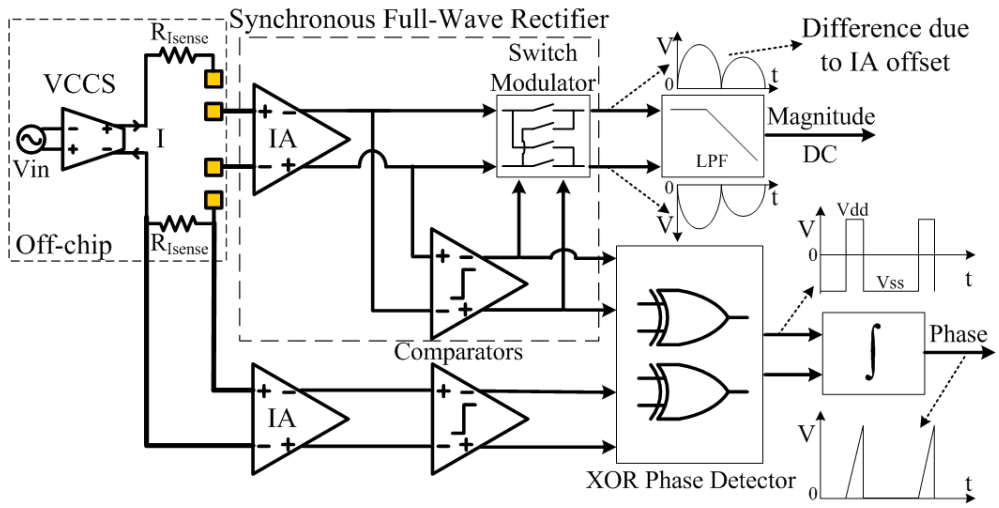

Fig. 3. Proposed magnitude/phase measurement system

The potential differences across the unknown impedance and the known current-sense resistor (R_{Isense}) are measured by two IAs and then converted into square waves using two clockless comparators. An XOR gate then produces a pulse signal, with the pulse width representing the phase delay introduced by the unknown impedance at that particular frequency. Since the same on-chip IAs and comparators are used, any delays imposed on the signals are matched and thus no error in the phase calculation occurs, provided that the gain settings of the IAs are the same. Two XOR gates are used in order to produce a differential signal. This is subsequently applied to a Gm-C integrator. Depending on the phase difference between the signals, the duty cycle of the XOR output will not always be 50%, leading to unequal charging and discharging of the integrator capacitor. Thus, in order to produce a symmetrical signal that will not reach the power supplies and saturate, a switch is placed across the capacitor, driven by one of the XOR outputs, thus synchronously discharging the capacitor at the end of every pulse. In this way a sawtooth wave is generated, the peak of which is proportional to the pulse duration and thus the phase. The measured signal has already been converted into a square wave for the calculation of the phase of the measured impedance. This can be used as the clock required by a switch modulator for synchronously rectifying the measured signal. This is then low-pass filtered to obtain the full-wave rectified signal dc average voltage. The phase (Φ) of the unknown impedance from the output of the phase detector is calculated by

$$\Phi = 360 \cdot \Delta t \cdot f. \tag{1}$$

If this is low-pass filtered, then the output of the filter is equal to

$$V_{PD} = \frac{V_{DD}}{\pi} \cdot \Phi, \tag{2}$$

and if it is integrated, the output of the integrator can be found by

$$V_{Int} = \frac{V_{DD} \cdot \Delta t}{\tau_{Int}}, \tag{3}$$

where Δt is the pulse width and f is the frequency of the applied signal, V_{DD} is the positive supply voltage (2.5V) and τ_{Int} is the time-constant of the integrator. The magnitude (M) of the unknown impedance is calculated from:

$$M = \frac{\pi \cdot V_{DC}}{2 \cdot A_v \cdot I}, \tag{4}$$

where V_{DC} is the filter output, A_v is the IA gain and I is amplitude of the injected current.

The fundamental difference between the proposed topology and those in [17-19] is that the magnitude is obtained through multiplication. In practice, the IA has a dc offset voltage. Thus, each output from the fully differential IA will have a dc level, which will be different between them. Because of the multiplication, this dc offset of the IA output signal is modulated from dc to the frequency of the injected signal, while the sinusoidal part of the output, similarly to SD, is in this way "locked-in" and demodulated to dc. If we consider the multiplication of the sine-wave output of the IA of angular frequency ω, amplitude V_o and a dc offset component B with a square wave of the same frequency with amplitude equal to unity and expand the square wave up to its first three components, then,

$$V_{out} = \frac{4}{\pi} \cdot \begin{bmatrix} \frac{V_o}{2} + B\sin(\omega t) - \frac{V_o}{3}\cos(2\omega t) + \frac{B}{3}\sin(3\omega t) \\ -\frac{V_o}{15}\cos(4\omega t) + \frac{B}{5}\sin(5\omega t) - \cos(6\omega t) + \ldots \end{bmatrix}, \tag{5}$$

As it can be seen from (5), the dc offset component has been modulated to the odd harmonics of the injected signal. Both

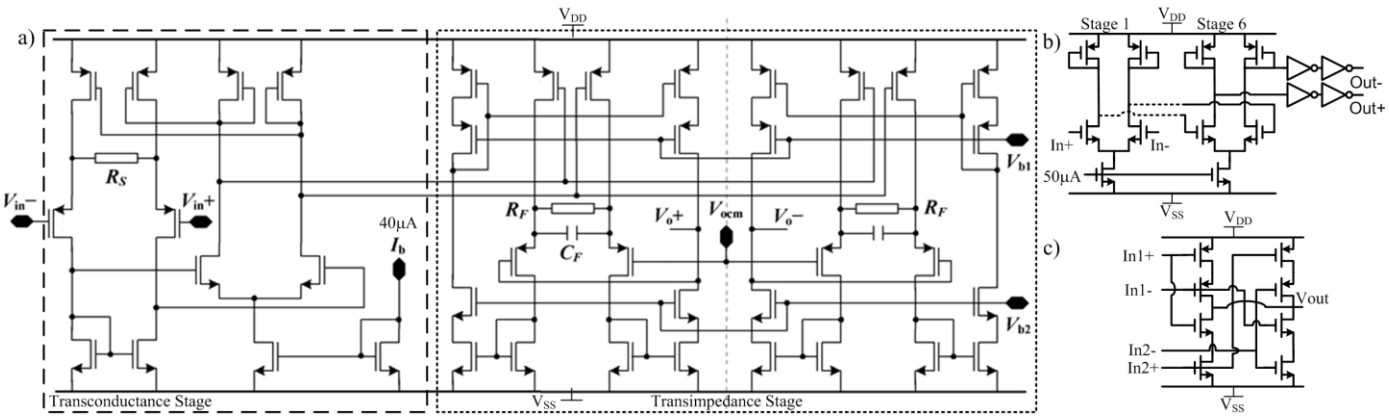

Fig. 4. (a) The current feedback IA, (b) the unlatched clockless continuous-time multi-step comparator topology and (c) the AOI XOR gate.

even and odd harmonics can be removed by the low-pass filter. In practice, a switch modulator is used instead of a multiplier. The inherent dc offsets at the outputs of the IA and the demodulator are eliminated by full-wave rectification of each of the single ended parts of the fully differential architecture. The difference of the differential modulator outputs effectively cancels out the dc component. The synchronous rectifier is comprised by elements which do not introduce any dc offsets. However, this advantage comes with the expense of needing a high-speed comparator. The delay of the comparator will introduce an error in the calculation of the magnitude. This, however, can be minimized with good design. To illustrate this in a simple manner we can examine the same multiplication as in (5), by ignoring B and all the harmonics of the square wave, only that now the square have fundamental has an added phase delay, ϕ:

$$V_{out} = \frac{2V_o}{\pi} \cdot \left(\cos(\phi) - \cos(2\omega t + \phi)\right), \tag{6}$$

Comparing the dc components of (5) and (6), it is obvious that there is an additional gain factor of $\cos(\phi)$, due to the delay of the comparator. This needs to be minimized.

The IC design of the system of Fig. 3 used 0.35-μm CMOS technology (austriamicrosystems C35) with 5V transistors (typical transistor gain factors K_N=100μA/V^2 and K_P=31μA/V^2 and threshold voltages of V_{TN}=0.7V and V_{TP}=-0.97V). The design and layout were performed with Cadence software.

III. System Blocks

A. Instrumentation Amplifier (IA)

The IA used is a current feedback topology [Fig. 4(a)] previously designed by our group [21], which has since been used in various impedance measurement systems [13, 14, 18, 19]. It is comprised of an input transconductance stage and two copies of the output transimpedance stage in order to make it fully-differential. High-swing cascode current mirrors and a CMOS neutralization capacitor (not shown) are used in order to enhance the CMRR (measured 90dB at 2MHz [21]). Its gain is set by the ratio of two integrated resistors (R_F and R_S). Gains of 10, 75, 140 and 200 can be programmed through switches using a 2-bit digital word. The IA is biased by a 40μA dc current.

B. Comparator

The delay of the comparator is important for the synchronous rectifier part of the system and needs to be very small. The comparator design is an unlatched clockless continuous-time multi-step comparator. As discussed in [22-23], dividing the total gain required for a specific resolution between n stages, results to less propagation delay than a single high gain stage. However, there is an optimum number of stages that minimizes the delay for a certain resolution and gain. For a split 5V=2E_{OH} supply, by setting a resolution (Δ_d) of 25mV>10$^{-3}E_{OH}$, and according to [22]

$$N_{opt} \approx 1.1 \cdot \ln\left(\frac{E_{OH}}{\Delta_d}\right) + 0.79, \tag{7}$$

the required number of amplification stages is approximately equal to six and the gain per stage is 2.2.

The gain-stage used was a simple differential pair with diode connected loads [Fig. 4(b)]. The output nodes are of relatively low impedance, the diode transistors control the output dc voltage and thus this topology does not need common-mode feedback [23]. The gain of this circuit is simply equal to the ratio of the transconductances of the N to the P transistors. This is independent of bias current and depends only on the device dimensions and the N and P mobility. For high speed and a set voltage gain, the ratio of the input pair transconductance (or equivalently of the diode connected load transconductance) to the load capacitance is important and has to be maximized. There is a trade-off between transconductance increase via device dimensions and load capacitance. Increasing the aspect ratio of the input pair will increase the drain-bulk capacitance, while increasing the diode-connected load dimensions will increase the gate area of these transistors and thus also the capacitance. Furthermore,

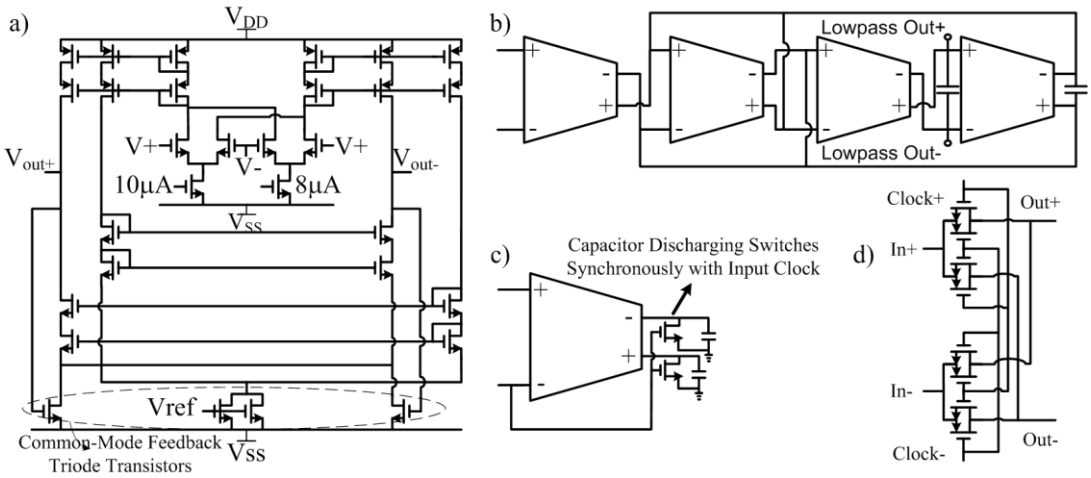

Fig. 5. (a) Non-linear term cancellation linearization double-balanced OTA topology used to implement the integrator. (b) The biquadratic filter structure. (c) the integrator with the discharging switches and (d) the switch modulator.

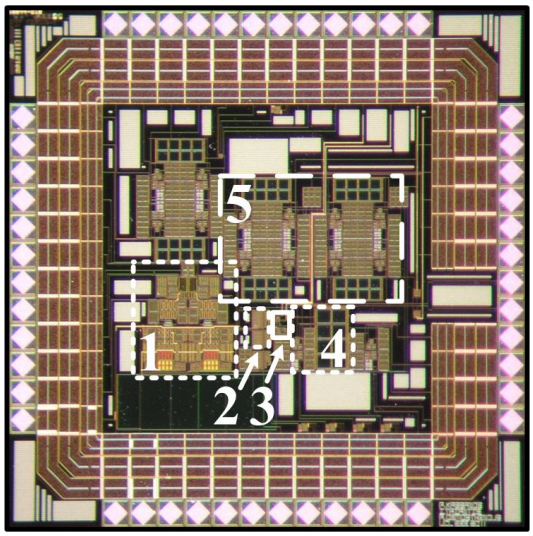

Fig. 6. Microphotograph of the fabricated chip. The marked areas show: 1: the two IAs, 2: the two comparators, 3: the switch modulator and the two XOR phase detectors, 4: the Gm-C integrator and 5: the chain of the two biquads.

since this is a multi-step topology, the input pair transistors of a stage are also loads to the previous stage. This is another reason why the dimensions of the input pair transistors need to stay small. Thus, the power efficiency was sacrificed in order to increase the transconductances without increasing parasitic capacitances by keeping transistor dimensions small.

Digital buffers, i.e. push-pull inverters, need to be used at the end of the amplifier chain in order to convert the amplified signal into the required digital levels, since the inverter has a rail-to-rail output swing. They are also used in order to increase the current driving capability without sacrificing speed and slew-rate; thus they should not load the previous stage. A chain of two push-pull inverters follows the amplifier chain.

Each stage of the comparator has a -3dB bandwidth of about 456MHz. Simulations indicated that the nominal delay of the comparator is only about 3ns. Thus, using (1) and (6) the

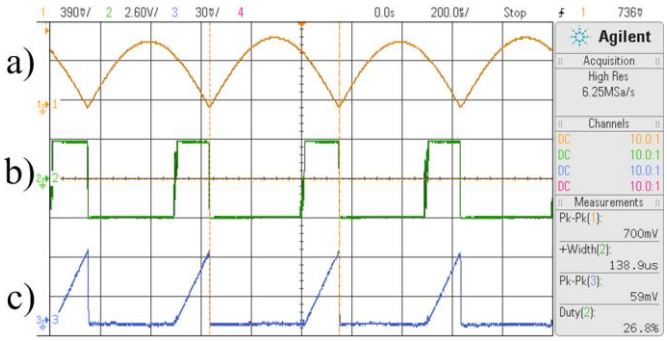

Fig. 7. Waveforms obtained from the fabricated chip. From top to bottom: (a) The synchronous rectifier output as obtained from the outputs of the switch modulator. (b) The XOR phase detector output and (c) the Gm-C integrator output.

magnitude error due to the delay of the comparator is, for example, at 1MHz equal to a gain factor of 0.999.

C. Switch Modulator

This type of switch modulator [Fig. 5(d)] is extensively used in chopping offset compensation techniques and it has also been used in synchronous demodulation systems [13-14]. By inputting a differential signal and by driving the switches by square waves of the same frequency and phase, the modulator combines the positive half cycles together and does the same for the negative ones, thus producing a differential full-wave rectified signal.

D. Phase Detector

The phase detector is implemented by a simple AND-OR-invert (AOI) logic XOR gate [Fig. 4(c)] designed according to [24]. XOR gates are capable of detecting phase differences between 0° and 90°, what one would expect from impedances with a capacitive reactance component, which is usually the case in biomedical applications. Alternatively, the switch modulator used for the synchronous rectifier, described in the previous subsection, could have been used for implementing the phase detector.

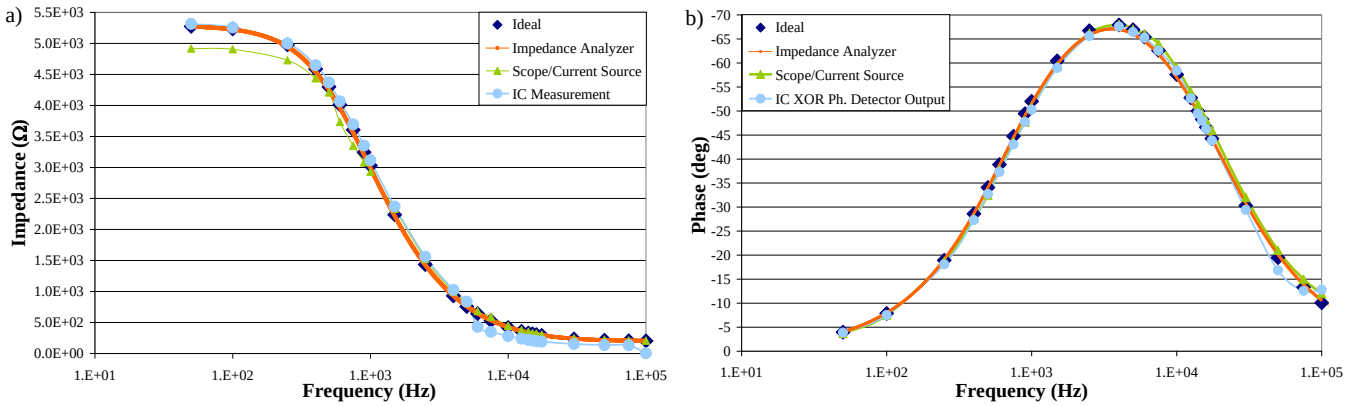

Fig. 8. Comparison of (a) the magnitude and (b) the phase of the equivalent RC circuit using theoretical calculations, an impedance analyzer, the ac current source and the oscilloscope and the fabricated chip.

E. Gm-C Integrator

The use of operational transconductance amplifiers (OTA's) for realizing integrators and filters is well established. Their open-loop operation, however, leads to increased distortion. Thus over the years many different linearization techniques have been proposed in order to reduce the harmonic content of the OTA output signals. One such technique [Fig. 5(a)] is the one discussed in [25]. It belongs to the family of non-linear term cancellation techniques.

The linear range of a simple long-tail differential pair, i.e. the range of input voltages, which results to a proportional change of output current, depends on the overdrive voltage of the input pair transistors. The larger this is, the larger the input linear range. This is a function of current and device dimensions. Thus, there is a tradeoff between these two factors. According to [25], the closer the tail current of the differential pairs are, the better the non-linear term cancellation is, leading, however, to larger reduction of transconductance. In order to obtain a very-large time-constant, a very-small transconductance is required. The two differential pairs of Fig. 5(a) used tail currents of 10μA and 8μA. Additional transconductance reduction can be achieved by using a double-balanced OTA topology and using the PMOS mirrors to divide the current flowing in the output branches (in order not to affect the input linear range or the linearization) and to obtain a differential output signal.

An OTA is a VCCS, thus, ideally it has infinite output impedance. As a result, the AC response of an ideal integrator has a dominant pole at DC with an infinite gain and a constant phase of 90°. Due to the very-small transconductance, the output resistance of the OTA needs to be increased. This is achieved by using simple cascode NMOS and PMOS current mirrors at the output branches Simple triode-transistor common-mode feedback (CMFB) was used as proposed in [26] in order to stabilize the common-mode output dc level to the mid-supply level of 0V. The OTA of Fig. 5(a) was used to implement both the biquadratic filter of Fig. 5(b) and the integrator of Fig. 5(c). A chain of two biquads was used.

IV. Measured Results

The chip microphotograph is shown in Fig. 6 with the various system blocks marked. The blocks occupy a silicon area of approximately $0.4mm^2$. The chip operates with ±2.5V power supplies and consumes about 21mW of power. The chip was mounted on a printed circuit board and tested with different RC loads.

As an example, the equivalent circuit proposed in [27] of the electrode/tissue impedance was used as the impedance to be measured. It consists of a 200Ω resistor in series with the parallel combination of 45nF capacitor and a 5kΩ resistor. Two 200Ω resistors were used on either side of the equivalent circuit as sense resistors. Simulations suggest that the chip can operate up to about 1 MHz. However, limited by the operating frequency of the current driver [11], measurements were restricted to 100 kHz. The current driver was used to inject a 50μA current to the equivalent circuit. Fig. 7 shows oscilloscope traces obtained experimentally using the fabricated chip. The measured results in Fig. 8 show a good agreement with the theoretical results, the results obtained using an impedance analyzer (Wayne Kerr 6500B) and measurements performed using the current source and simply an oscilloscope. Table I summarizes the performance of the chip.

Table I. Summary of Measured Performance

Parameter	Value
Technology	0.35-μm CMOS
Active area	0.4 mm^2
Supply voltage	±2.5 V
Power consumption	21mW
Frequency range	>1 MHz
Phase measurement accuracy	>94%
Magnitude measurement accuracy	>90% at 50 Hz - > 5 kHz >65% at 6 kHz - > 100kHz

V. Conclusion

Commonly used EIS methods like SD and SS suffer from inherent issues that require increasingly complex circuitry to

tackle. Magnitude/phase measurement is an alternative. The proposed system can alleviate some of the synchronization and offset limitations associated with these other systems whilst significantly reducing complexity. A CMOS integrated magnitude/phase impedimetric chip has been presented as a proof of concept. The experimental results obtained using this early-stage implementation showed a good correlation with theoretical results in measuring the impedance of an equivalent RC circuit. The system presented will be combined with a custom designed high bandwidth and high output impedance ac current source. This is currently being developed as a parallel project in our group, to offer a complete, accurate and low-complexity EIS solution.

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