A CMOS Smart Temperature Sensor With a 3σ Inaccuracy of $\pm 0.5\,^{\circ}\mathrm{C}$ From $-50\,^{\circ}\mathrm{C}$ to $120\,^{\circ}\mathrm{C}$

Michiel A. P. Pertijs, *Student Member, IEEE*, Andrea Niederkorn, Xu Ma, Bill McKillop, *Member, IEEE*, Anton Bakker, *Senior Member, IEEE*, and Johan H. Huijsing, *Fellow, IEEE*

***Abstract*—A low-cost temperature sensor with on-chip sigma-delta ADC and digital bus interface was realized in a 0.5 μm CMOS process. Substrate pnp transistors are used for temperature sensing and for generating the ADC's reference voltage. To obtain a high initial accuracy in the readout circuitry, chopper amplifiers and dynamic element matching are used. High linearity is obtained by using second-order curvature correction. With these measures, the sensor's temperature error is dominated by spread on the base-emitter voltage of the pnp transistors. This is trimmed after packaging by comparing the sensor's output with the die temperature measured using an extra on-chip calibration transistor. Compared to traditional calibration techniques, this procedure is much faster and therefore reduces production costs. The sensor is accurate to within $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ) from $-50\,^{\circ}\mathrm{C}$ to $120\,^{\circ}\mathrm{C}$.**

***Index Terms*—Calibration, curvature correction, dynamic offset cancellation, smart sensors, temperature sensors.**

I. Introduction

INTEGRATED temperature sensors with an on-chip analog-to-digital converter and bus interface find growing application in thermal management systems. These so-called "smart" temperature sensors are widely applied in PCs and laptops to monitor the temperature of the microprocessor, the case, and power-consuming peripheral ICs. This application requires low-cost temperature sensors with a desired inaccuracy below $\pm 1.0\,^{\circ}\mathrm{C}$ [1].

Previous smart temperature sensors were usually calibrated at one fixed temperature, at which their inaccuracy could be trimmed below $\pm 1.0\,^{\circ}\mathrm{C}$ at the cost of a time-consuming (and therefore expensive) calibration after packaging. Their inaccuracy over the industrial temperature range is however larger than $\pm 1.0\,^{\circ}\mathrm{C}$ [2]–[8].

This paper describes in detail a smart temperature sensor which achieves an inaccuracy of $\pm 0.5\,^{\circ}\mathrm{C}$ (3σ) from $-50\,^{\circ}\mathrm{C}$ to $120\,^{\circ}\mathrm{C}$ [9]. Costs are kept low by using a mature 0.5-μm CMOS process and a fast calibration procedure. After packaging, the sensor is calibrated by measuring its die temperature using an extra on-chip calibration transistor. Thus, the required calibration time is greatly reduced compared to a traditional calibration with an external reference thermometer. To obtain a high initial accuracy, dynamic offset cancellation and dynamic element matching are applied in the analog front-end. Good linearity over a wide temperature range is obtained by applying second-order curvature correction.

This paper is organized as follows. Section II introduces the measurement principle, including the curvature correction technique. In Section III, the analog front-end circuitry is discussed, which generates two temperature-dependent currents. These are input to a second-order sigma-delta ADC, which is described in Section IV. The calibration technique is detailed in Section V. The paper ends with experimental results in Section VI and conclusions.

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M. A. P. Pertijs and J. H. Huijsing are with the Electronic Instrumentation Laboratory, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: pertijs@ieee.org).

A. Niederkorn is with Zoran Corporation, Mesa, AZ 85210 USA.

X. Ma is with Microchip Technology, Chandler, AZ 85224 USA.

B. McKillop is with On Semiconductor, Phoenix, AZ 85082 USA.

A. Bakker is with Analog Devices, San Jose, CA 95134 USA.

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II. Measurement Principle

To convert temperature to a digital value, both a well-defined temperature-dependent signal and a temperature-independent reference signal are required. Both can be derived from the base-emitter voltage of a bipolar transistor, in the form of the thermal voltage kT/q and the silicon bandgap voltage [10]. In a CMOS process, substrate pnp transistors are mostly used for this purpose [11]. These are vertical bipolar transistors with a p^{+} diffusion as emitter, an n-well as base, and the p^{-} substrate as collector.

Two voltages are of interest: the base-emitter voltage V_{BE} of a single transistor in its forward-active region, and the difference ΔV_{BE} between the base-emitter voltages of two such transistors biased at different collector current densities.

A. Temperature Dependence of V_{BE}

From the well-known exponential relation between the collector current I_C and the base-emitter voltage V_{BE}, the following expression for V_{BE} as a function of absolute temperature T can be derived [10]:

$$V_{BE}(T) = V_{g0}\left(1-\frac{T}{T_r}\right) + \frac{T}{T_r}V_{BE}(T_r) - \eta\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) + \frac{kT}{q}\ln\left(\frac{I_C(T)}{I_C(T_r)}\right) \quad (1)$$

where V_{g0} is the extrapolated bandgap voltage at 0 K, η is a process-dependent constant, k is Boltzmann's constant, q is the electron charge, and T_r is an arbitrary reference temperature. As illustrated in Fig. 1(a), $V_{BE}(T)$ is an almost linear function of temperature, with a typical slope of -2 mV/K. The nonlinearity, or curvature, is represented by the last two terms of (1).

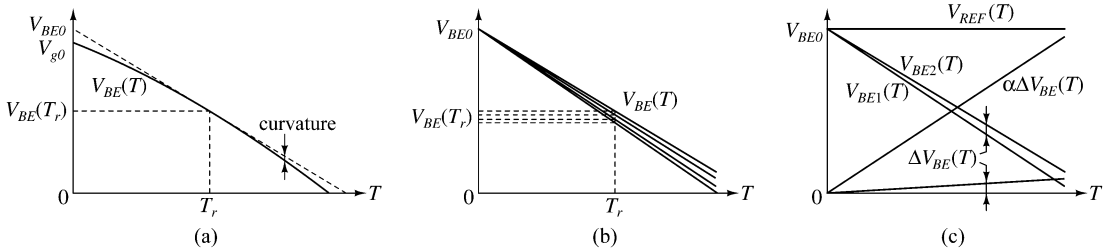

Fig. 1. (a) Temperature dependence of the base-emitter voltage V_{BE}. (b) Variation in V_{BE} due to process spread (curvature omitted for clarity). (c) Combination of V_{BE} and ΔV_{BE} to yield the bandgap reference voltage V_{REF} (curvature again omitted).

It depends on the constant η and on the temperature dependence of the collector current.

The slope of the base-emitter voltage depends on process parameters and the absolute value of the collector current. Its extrapolated value at 0 K, however, is insensitive to process spread and current level, as illustrated in Fig. 1(b). Therefore, a calibration at one temperature can be used to trim the slope of V_{BE} to a desired value [12].

V_{BE} is also sensitive to stress. Fortunately, substrate pnp transistors are much less stress-sensitive than other bipolar transistors [13]. Packaging-induced shifts in V_{BE} will be corrected by calibrating the sensor after packaging, as will be discussed in Section V.

B. Temperature Dependence of ΔV_{BE}

The difference ΔV_{BE} between the base-emitter voltages of a transistor operated at two collectors I_{C1} and I_{C2} can be expressed as [10]

$$\Delta V_{BE}(T) = V_{BE2}(T) - V_{BE1}(T) = \frac{kT}{q}\ln\left(\frac{I_{C2}}{I_{C1}}\right). \quad (2)$$

Provided the collector-current ratio is constant, ΔV_{BE} is proportional to absolute temperature (PTAT), as shown in Fig. 1(c).

In contrast with V_{BE}, ΔV_{BE} is independent of process parameters and the absolute value of the collector currents.[1] Moreover, it is insensitive to stress [15]. Its temperature coefficient is, however, typically an order of magnitude smaller than that of V_{BE} (depending on the collector current ratio).

C. Combining V_{BE} and ΔV_{BE}

In a bandgap voltage reference, an amplified version of ΔV_{BE} is added to V_{BE} to yield a temperature-independent reference voltage V_{REF}, as illustrated in Fig. 1(c). In our temperature sensor, this addition is implemented in the current domain at the input of the sigma-delta modulator (Fig. 2). Depending on the bitstream output bs of the modulator, either a current $\Delta V_{BE}/R_1$ is integrated (when $bs = 0$) or a current $-V_{BEtrim}/R_2$ (when $bs = 1$), where V_{BEtrim} is a trimmed base-emitter voltage. The negative feedback in the modulator will ensure that the average current flowing into the integrator is zero. This implies

$$\mu\frac{V_{BEtrim}}{R_2} = (1-\mu)\frac{\Delta V_{BE}}{R_1}$$
$$\Longrightarrow \mu = \frac{\alpha\Delta V_{BE}}{V_{BEtrim} + \alpha\Delta V_{BE}} = \frac{\alpha\Delta V_{BE}}{V_{REF}} \quad (3)$$

where μ is the average value of the bitstream (i.e., the fraction of 1's), and $\alpha = R_2/R_1$. The denominator of (3) is essentially a bandgap reference voltage, while the numerator is PTAT. The average μ will therefore also be PTAT, so that the bitstream can be used, with appropriate scaling in the digital decimation filter, to produce a digital representation of the chip's temperature in degrees Celsius.

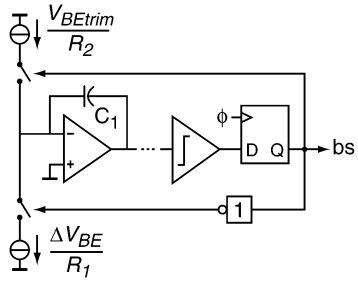

Fig. 2. Simplified circuit diagram of the sigma-delta modulator.

With the configuration of Fig. 2, only about 30% of the dynamic range of the sigma-delta modulator is used, since $\mu = 0$ corresponds to -273 °C and $\mu = 1$ corresponds to approximately 325 °C, while the temperature range of interest is from -50 °C to 125 °C. Other combinations of V_{BEtrim} and ΔV_{BE} can be used to utilize more of the dynamic range [16], but these require copying or scaling of the currents, thus introducing more sources of errors. Since a second-order sigma-delta modulator is used, which can easily provide sufficient resolution, a more efficient use of the dynamic range is not needed. In fact, for the single-loop modulator used (Section IV), the quantization noise strongly increases for μ close to 0 or 1. With the configuration of Fig. 2, these regions are conveniently avoided.

D. Curvature Correction

The curvature of V_{BE} will also be present in the reference voltage V_{REF}, which, in turn, results in a nonlinearity in $\mu(T)$. The curvature is modeled by the last two terms in (1). For a value of $\eta = 4.4$ for our process and a PTAT collector current (as used

[1]Often a multiplicative factor n is included in the equation for ΔV_{BE} to model the influence of the reverse Early effect and other nonidealities [14]. If V_{BE} and ΔV_{BE} are generated using transistors biased at approximately the same current density, an equal multiplicative factor will appear in V_{BE}. In a smart temperature sensor, these factors cancel, and will therefore not be considered further.

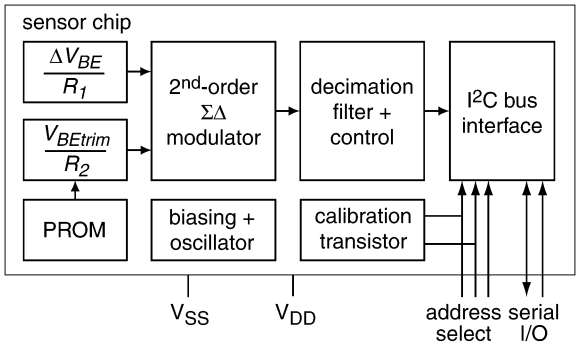

Fig. 3. Block diagram of the temperature sensor.

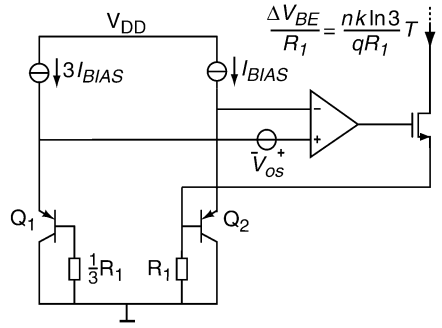

Fig. 4. Simplified circuit diagram of the ΔV_{BE}-dependent current source.

in our design), the corresponding nonlinearity amounts to 2 °C over the temperature range of −50 °C to 125 °C.

Fortunately, the second-order component of the curvature can easily be eliminated by giving V_{REF} a small positive temperature coefficient [4], [17], i.e., by making α in (3) slightly larger than in a bandgap reference. With an appropriate value for α (22 in our case), such a temperature-dependent V_{REF} gives rise to a second-order nonlinearity in $\mu(T)$ which exactly cancels the second-order nonlinearity originating from V_{BE}. What remains is a third-order nonlinearity of about 0.3 °C over the temperature range.

E. Block Diagram

The input currents for the sigma-delta modulator of Fig. 2 are generated by a $\Delta V_{BE}/R_1$ current source and a V_{BEtrim}/R_2 current source, as shown in the block diagram of Fig. 3. A decimation filter converts the bitstream output of the modulator to a digital representation of the temperature, also taking care of the scaling required to convert the average value μ of the bitstream to °C. The result is communicated to the outside world using an I^2C bus interface. Also on the chip are the calibration transistor, a PROM to hold the setting of the trimming of V_{BE}, a biasing circuit and an oscillator.

III. Temperature-Dependent Current Sources

A. ΔV_{BE}-Dependent Current Source

A simplified circuit diagram of the $\Delta V_{BE}/R_1$ current source is shown in Fig. 4 [16]. Two substrate pnp transistors Q_1 and Q_2 are biased at a 3:1 current ratio. The bias currents are generated in a separate circuit (not shown). The resulting difference in base-emitter voltage ΔV_{BE} has a sensitivity of 100 μV/°C. By means of the feedback loop, ΔV_{BE} is generated across a resistor R_1 in series with the base of Q_2, resulting in the desired output current. To avoid that the output current is affected by the base current of Q_2, a resistor $R_1/3$ is added in series with the base of Q_1. As the base current of Q_1 is three times as large as that of Q_2, the base currents result in an equal voltage drop across both resistors, which is a small common-mode change that does not affect the output current.

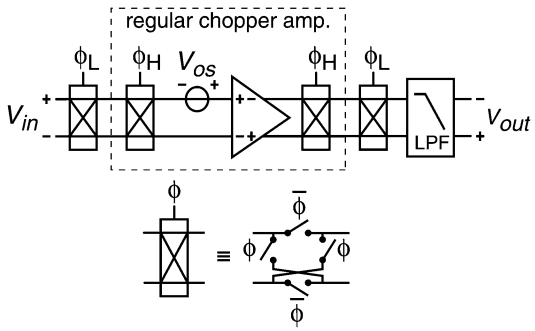

Fig. 5. Principle of a nested-chopper amplifier.

The inaccuracy of the circuit of Fig. 4 is mainly determined by the offset V_{os} of the opamp, which directly adds to ΔV_{BE}. To result in a negligible temperature error (0.1 °C), this offset has to be smaller than 10 μV. Since typical offsets of CMOS opamps are in the millivolt range, offset cancellation is required. Mismatch in the current sources or the pnp transistors also leads to temperature errors. For these errors to be negligible, the matching has to be better than 0.035%, which requires dynamic element matching.

The offset of the opamp can be reduced using the chopping technique. In a regular chopper amplifier, a pair of chopper switches is added around the amplifier whose offset V_{os} needs to be cancelled (Fig. 5) [16]. The chopper at the input modulates the input signal to the frequency of control signal ϕ_H, which lies above the offset and $1/f$ corner frequency of the amplifier. The chopper at the output demodulates the amplified input signal, and simultaneously modulates the amplified offset and $1/f$ noise to the frequency of ϕ_H, where they can be filtered out by a low-pass filter (LPF).

Due to charge injection and clock feedthrough, a regular chopper amplifier has a typical residual offset of a few tens of microvolts. To reduce the offset below 10 μV, an extra outer pair of chopper switches is added. This is controlled by a low-frequency control signal ϕ_L. This pair modulates the regular chopper amplifier's residual offset to the frequency of ϕ_L, where it can also be removed by the LPF. The residual offset of the resulting *nested*-chopper amplifier is determined by clock feedthrough and charge injection in the low-frequency chopper switches, and is therefore much smaller than that of the regular chopper amplifier. Residual offsets as low as 100 nV have been reported [18].

Fig. 6 shows how the nested-chopper amplifier is embedded in the $\Delta V_{BE}/R_1$ current source. The opamp is split up into three stages, with chopper switches between them. The first stage is a folded-cascode amplifier, the second stage is a differential pair, and the third stage is its current mirror load. Miller compensation (not shown) is used to stabilize the opamp.

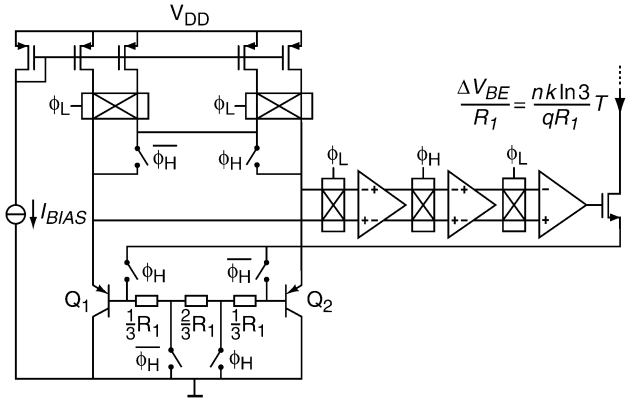

Fig. 6. Detailed circuit diagram of the ΔV_{BE}-dependent current source.

The input chopper driven by ϕ_H is implemented in the current domain, by switching between a 3:1 and 1:3 current ratio. Thus, offset resulting from mismatch between the pnp transistors is also chopped. To maintain the correct feedback polarity, the connection to the output transistor is switched back and forth between the bases of Q_1 and Q_2. As in Fig. 4, compensation for the base currents is realized by making sure that a resistor $R_1/3$ is in series with the base of the transistor that carries the larger bias current.

The bias currents are generated by four current sources of 0.5 μA each, which are dynamically matched using the control signals ϕ_H and ϕ_L. Alternately, one of the current sources biases one transistor, while the remaining three bias the other.

The control signal ϕ_H switches at 16 kHz, while ϕ_L switches at 80 Hz. The modulated offset and $1/f$ noise components are filtered out by the sigma-delta modulator and the decimation filter, as will be discussed in Section IV.

B. V_{BE}-Dependent Current Source

The trimmed base-emitter voltage V_{BEtrim} is generated by adjusting the base-emitter voltage V_{BE} of a substrate pnp transistor with a small programmable PTAT voltage. Fig. 7 shows how this is implemented: a PTAT current is passed through a digitally programmable resistor in series with a diode-connected substrate pnp. The PTAT voltage across this resistor compensates for the PTAT-type spread on V_{BE} [Fig. 1(b)]. The PTAT current in Fig. 7 is generated in a separate bias circuit (not shown).

The current V_{BEtrim}/R_2 is generated using a voltage-to-current converter around a regular chopper amplifier controlled by ϕ_L. Because of the higher sensitivity of $V_{BE}(-2\ \text{mV}/^{\circ}\text{C})$, a nested-chopper amplifier was not needed here. The amplifier has a folded-cascode topology. To accurately define the ratio α in (3), the resistors R_1 and R_2 are made of identical unit resistors.

To save power, the nominal output current is kept relatively small (0.5 μA). Therefore, a large resistance (more than 1 MΩ) is required. In order to reduce the size of the resistor, a current mirror with a dynamically matched 3:1 ratio is used. The dynamic element matching is again controlled by ϕ_L and ϕ_H. Thus, the chip area required for the resistor is reduced by a factor 3 without using special high-resistivity resistors (which would require extra processing steps).

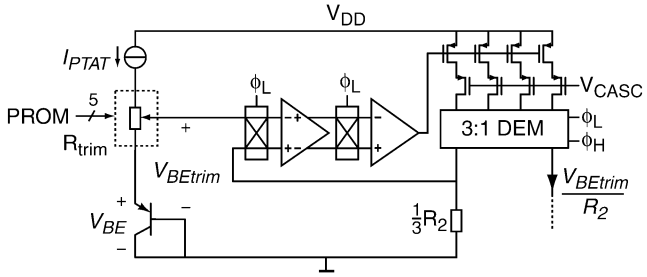

Fig. 7. Circuit diagram of the V_{BE}-dependent current source.

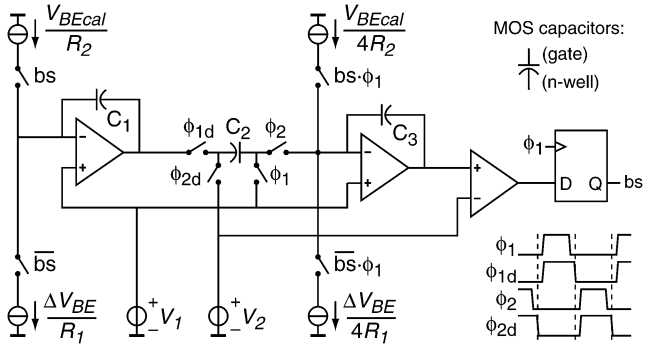

Fig. 8. Circuit diagram of the sigma-delta modulator; initialization circuits are omitted for clarity; unused currents are switched to V_1.

IV. Sigma-Delta ADC

A sigma-delta ADC is used to convert the temperature-dependent currents into a digital temperature reading. A quantization noise below 0.05 °C in a conversion time of 30 ms was desired. With a first-order sigma-delta modulator, as was used in previous work [4], [16], this would require a clock frequency of about 500 kHz. As this would lead to an undesirably high power consumption, a second-order modulator was used, which requires a clock frequency of only 16 kHz.

As in an incremental ADC [19], the integrators of the modulator are reset at the beginning of the conversion, and a second-order decimation filter is used rather than the usual third-order filter. In contrast with an incremental ADC, however, the input signal is not sampled and held during the conversion, but it is integrated continuously so as to filter out the modulated offset and $1/f$ noise.

A. Sigma-Delta Modulator

A simplified circuit diagram of the sigma-delta modulator is shown in Fig. 8. It is clocked using a nonoverlapping clock which runs at the same frequency as the control signal ϕ_H in the current sources. This ensures that modulated offset at harmonics of ϕ_H is averaged out within a clock cycle of the modulator. As discussed in Section II-C, the bitstream determines which of the two input currents is integrated on the first integrator. Unused currents are dumped into a reference node at V_1 (not shown).

During clock phase ϕ_1, the output of the first integrator is sampled on capacitor C_2. During phase ϕ_2, the charge is transferred to the second integrator, the output of which is fed into a clocked comparator that produces the bitstream bs. To minimize charge injection onto C_2, clock signals ϕ_{1d} and ϕ_{2d} have

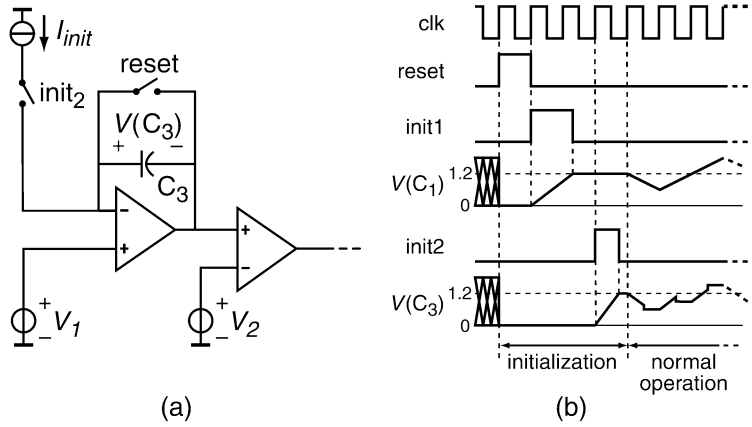

Fig. 9. (a) Initialization circuit for the second integrator. (b) Waveforms during the initialization sequence.

delayed downgoing edges with respect to ϕ_1 and ϕ_2. Scaled copies of the input currents are integrated on the second integrator during phase ϕ_1 to ensure stability of the modulator and to minimize the swing at the output of the first integrator. The scaled copies are not critical for the dc accuracy of the modulator; mismatches up to several percent can be tolerated.

The modulator is implemented using MOS capacitors, to avoid the extra processing steps required for linear capacitors. C_1 and C_2 are made from identical unit capacitors to ensure linear charge transfer in spite of the nonlinearity of these capacitors. The nonlinearity of C_3 is not relevant, since only the sign of the output of the second integrator is detected by the comparator.

To maximize the capacitance per area of the MOS capacitors, and to avoid operating them in their most nonlinear region (around 0 V), they are biased in accumulation. The gates of the capacitors are at V_1, while the feedback ensures that the average voltage on their wells is V_2. Therefore, they can be biased in accumulation by choosing V_1 sufficiently higher than V_2 (1.2 V in this case).

B. Initialization Sequence

In contrast with the usual continuous operation of sigma-delta ADCs, the temperature sensor requires a "one-shot" type of operation, i.e., the converter is powered up, produces a single conversion result, and powers down again to save power. This has implications for both the initialization of the modulator, and the design of the decimation filter.

After power-up, the modulator is brought into a well-defined state by resetting the integration capacitors. After the reset, the integration capacitors could be driven into accumulation by the feedback loop, but this may take many clock cycles (depending on the input signal). To expedite this, the capacitors are precharged using an initialization current I_{init}, as shown in Fig. 9(a) for the second integrator. The initialization current is switched to the input of the integrator until its output reaches the voltage V_2, which is detected by the comparator.

To allow for similar initialization of the first integrator, its output can be connected to the input of the comparator using a set of switches (not shown). The total initialization sequence consists of resetting both integration capacitors, precharging the capacitor of first integrator, and then precharging that of the second integrator. The corresponding waveforms are shown in Fig. 9(b).

C. Decimation Filter

Once the modulator has reached its steady state, the bitstream is fed into a decimation filter, which produces a single conversion result. Usually, the order of a sinc decimation filter is chosen one higher than that of the loop filter [20], which implies a third-order filter for our second-order modulator. However, for a given conversion time, and thus a given impulse response length of the filter, the corner frequency of a third-order filter is higher than that of a second-order filter. Due to this higher corner frequency, the use of a third-order filter will result in more quantization noise, in spite of its faster roll-off. Therefore, a less complex sinc^2 filter is used rather than a sinc^3 filter.

For the chopping and dynamic element matching in the current sources to be effective, the decimation filter has to filter out the residuals modulated by the low-frequency control signal ϕ_L. Therefore, ϕ_L is clocked at a frequency that coincides with the first zero in the frequency response of the sinc^2 filter, which is at approximately 80 Hz.

The decimation filter is implemented by an up/down counter and an accumulator. The counter counts up during the first half of the decimation period and down during the second half, thus realizing the triangular impulse response of a sinc^2 filter. The accumulator adds the counter value if the bitstream is "1". The initial value of the accumulator and the exact length of the decimation period (and thereby the gain of the filter) are chosen such that the accumulated value at the end of the conversion can be directly interpreted as a temperature in degrees Celsius.

V. Calibration Technique

To calibrate any integrated temperature sensor, its temperature reading has to be compared to that of a reference thermometer at the same temperature as the sensor chip. The difference between the readings may then be used to trim the sensor. This calibration is often done at wafer-level, which has the advantage that the temperature of the whole wafer can be stabilized

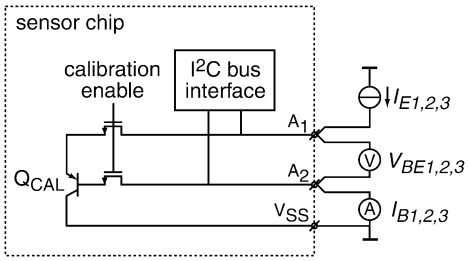

Fig. 10. Connection of the calibration transistor by reusing digital input pins.

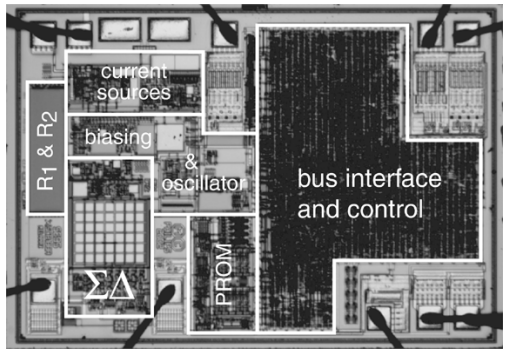

Fig. 11. Chip micrograph of the temperature sensor.

and measured, after which the individual sensors can be calibrated and trimmed using a wafer prober. An important disadvantage of this approach, however, is that additional errors introduced by packaging stress are not taken into account. Even when the sensor design is based on relatively stress-insensitive substrate pnp transistors, a significant error will result if a low-cost plastic package is used. Experiments on a bandgap reference based on such pnps have shown shifts up to 2 mV in V_{BE} [13]. As can be derived from (3), this translates to a temperature error of about 0.5 °C. Therefore, it is desired to do the calibration after packaging.

If the temperature of each individual packaged sensor has to be stabilized and measured with an inaccuracy below $\pm 0.5\,^{\circ}$C using a reference thermometer, this becomes the dominant contributor to the test time of the sensor. A faster and therefore cheaper alternative is to make use of the process- and stress-insensitivity of ΔV_{BE} (discussed in Section II-B): an extra substrate pnp transistor, the calibration transistor, has been integrated on the sensor chip, and is used as a reference thermometer *inside* the package [21]. From its ΔV_{BE}, measured using external electronics, the die temperature can be determined within $\pm 0.1\,^{\circ}$C [21]. As it is integrated on the same thermally conducting silicon as the sensor circuit, very little thermal settling time is required. Moreover, the requirements on the thermal stability of the production setup are relaxed.

Fig. 10 shows how the calibration transistor (Q_{CAL}) is connected without reserving extra pins for it. Two existing address pins of the I²C bus interface are reused during calibration to connect to the base and emitter of Q_{CAL}. During normal operation, Q_{CAL} is isolated from these pins using MOS switches. These switches are controlled via the bus interface.

The temperature of the on-chip calibration transistor is determined by applying a number of bias currents to it, and measuring its base-emitter voltage and base current using external electronics. Thus, ΔV_{BE} can be measured while compensating for series resistances [22] and current-gain variations. From this, the chip temperature can be calculated with an absolute accuracy of $\pm 0.1\,^{\circ}$C [21]. The difference between this temperature and a reading of the sensor is then used to determine the appropriate setting for the programmable resistor R_{trim} in Fig. 7. This setting is then programmed in PROM via the I²C bus interface.

VI. Experimental Results

The temperature sensor was fabricated in a standard 0.5-μm CMOS process. A chip micrograph is shown in Fig. 11. The chip area is 2.5 mm², of which about half is used for the digital bus interface and control.

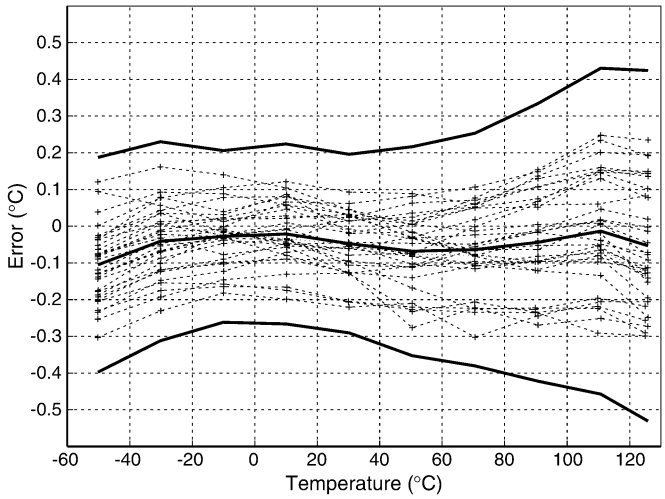

Fig. 12. Measured temperature error of 32 samples from one batch, with average and $\pm 3\sigma$ values.

TABLE I
Performance Summary

Technology	0.5μm CMOS
Chip size	2.5mm²
Supply voltage	2.7V – 5.5V
Temperature range	-50°C – 125°C
Conversion rate	0.125 – 30 conversions/s
Noise level	$0.03^{\circ}\mathrm{C_{rms}}$
Supply current	130μA at 10 conversions/s
Power supply rejection	0.3°C/V from 3.0V to 3.6V
Inaccuracy (3σ)	$\pm 0.3^{\circ}$C at 25°C $\pm 0.5^{\circ}$C from -50°C to 120°C

Fig. 12 shows the measured temperature error of 32 samples from one processing batch, operated at a supply voltage of 3.3 V. These samples were packaged in 8-pin ceramic packages. They were calibrated and trimmed at room temperature using the described procedure, after which they were placed in an oven along

TABLE II
COMPARISON OF INACCURACY WITH PREVIOUS WORK

Reference	Inaccuracy	Range	Conditions	Calibration
Bakker, 1996 [2]	$\pm 1.0^{\circ}$C	-40°C to 120°C	min/max of 3 samples	after packaging, 2 points
Tuthill, 1998 [3]	$\pm 1.5^{\circ}$C	-50°C to 125°C	min/max of 6 samples	wafer-level, 1 point
Pertijs, 2001 [4]	$\pm 1.5^{\circ}$C	-50°C to 125°C	$\pm 3\sigma$ of 32 samples	batch-calibration
LM92 [5]	$\pm 0.33^{\circ}$C	30°C	min/max	unknown
	$\pm 1.5^{\circ}$C	-25°C to 150°C	min/max	unknown
DS1626 [6], ADT7301 [7]	$\pm 0.5^{\circ}$C	0°C to 70°C	min/max	unknown
	$\pm 2.0^{\circ}$C	-55°C to 125°C	min/max	unknown
SMT160-30 [8]	$\pm 0.7^{\circ}$C	-30°C to 100°C	min/max	wafer-level, 1 point
	$\pm 1.2^{\circ}$C	-45°C to 130°C	min/max	wafer-level, 1 point
This work	$\pm 0.3^{\circ}$C	25°C	$\pm 3\sigma$ of 32 samples	after packaging, 1 point
	$\pm 0.5^{\circ}$C	-50°C to 125°C	$\pm 3\sigma$ of 32 samples	after packaging, 1 point

with a platinum resistor calibrated to 20 mK. Their 3σ inaccuracy in the temperature range of $-50\,^{\circ}$C to $120\,^{\circ}$C is $\pm 0.5\,^{\circ}$C. The performance of the chips is summarized in Table I.

Table II compares the inaccuracy with that of previous work. Though many smart temperature sensors have been published, only a few publications provide sufficient measurement results for a proper comparison [2]–[4]. Since most work in this field is done in industry, the inaccuracy specifications of four leading commercial temperature sensors have also been included in the table [5]–[8]. At room temperature, the presented sensor performs as well as the best-performing previous work, while over a wide temperature range it performs significantly better.

VII. CONCLUSION

A CMOS temperature sensor with integrated second-order sigma-delta ADC and bus interface has been presented. A high initial accuracy is achieved by applying dynamic offset cancellation and dynamic element matching in the front-end circuitry, and by applying a linearization technique that eliminates the second-order curvature. With these measures, the spread on the base-emitter voltage is the dominant source of errors. This is trimmed based on the results of a single-point calibration, which takes place after packaging. The chip temperature is determined from the electrical characteristics of an additional on-chip transistor, which are measured using external electronics. Thus a fast and accurate calibration can be performed. After calibration at room temperature and trimming, the sensor has a 3σ inaccuracy of $\pm 0.5\,^{\circ}$C in the temperature range of $-50\,^{\circ}$C to $120\,^{\circ}$C, which is, to date, the highest reported accuracy for this type of sensors.

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REFERENCES

[1] D. Marsh, "Silicon sensors harness thermal management," *EDN*, pp. 43–55, Dec. 2003.

[2] A. Bakker and J. H. Huijsing, "Micropower CMOS temperature sensor with digital output," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 933–937, Jul. 1996.

[3] M. Tuthill, "A switched-current, switched-capacitor temperature sensor in 0.6-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1117–1122, Jul. 1998.

[4] M. A. P. Pertijs, A. Bakker, and J. H. Huijsing, "A high-accuracy temperature sensor with second-order curvature correction and digital bus interface," in *Proc. ISCAS*, May 2001, pp. 368–371.

[5] (2000) LM92 Data Sheet. National Semiconductor Corporation. [Online]. Available: http://www.national.com

[6] (2003) DS1626 Data Sheet. Maxim Int. Products. [Online]. Available: http://www.maxim-ic.com

[7] (2003) ADT7301 Data Sheet. Analog Devices Inc. [Online]. Available: http://www.analog.com

[8] (2003) SMT160-30 Data Sheet. Smartec B.V. [Online]. Available: http://www.smartec.nl

[9] M. Pertijs *et al.*, "A CMOS temperature sensor with a 3σ inaccuracy of $\pm 0.5\,^{\circ}$C from $-50\,^{\circ}$C to $120\,^{\circ}$C ," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2003, pp. 200–201, 488.

[10] G. C. M. Meijer, "Thermal sensors based on transistors," *Sensors and Actuators*, vol. 10, pp. 103–125, Sep. 1986.

[11] G. Wang and G. C. M. Meijer, "Temperature characteristics of bipolar transistors fabricated in CMOS technology," *Sensors and Actuators A*, vol. 87, pp. 81–89, Dec. 2000.

[12] G. C. M. Meijer, G. Wang, and F. Fruett, "Temperature sensors and voltage references implemented in CMOS technology," *IEEE Sensors J.*, vol. 1, no. 3, pp. 225–234, Oct. 2001.

[13] F. Fruett, G. C. M. Meijer, and A. Bakker, "Minimization of the mechanical-stress-induced inaccuracy in bandgap voltage references," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1288–1291, Jul. 2003.

[14] M. A. P. Pertijs, G. C. M. Meijer, and J. H. Huijsing, "Precision temperature measurement using CMOS substrate pnp transistors," *IEEE Sensors J.*, vol. 4, no. 3, pp. 294–300, Jun. 2004.

[15] F. Fruett, G. Wang, and G. C. M. Meijer, "The piezojunction effect in npn and pnp vertical transistors and its influence on silicon temperature sensors," *Sensors and Actuators A*, vol. 85, pp. 70–74, Aug. 2000.

[16] A. Bakker and J. H. Huijsing, *High-Accuracy CMOS Smart Temperature Sensors*, ser. Int. Series in Engineering and Computer Science. Boston, MA: Kluwer, 2000, vol. 595.

[17] G. C. M. Meijer *et al.*, "A three-terminal integrated temperature transducer with microcomputer interfacing," *Sensors and Actuators*, vol. 18, pp. 195–206, Jun. 1989.

[18] A. Bakker, K. Thiele, and J. H. Huijsing, "A CMOS nested-chopper instrumentation amplifier with 100-nV offset," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1877–1883, Dec. 2000.

[19] J. Robert and P. Deval, "A second-order high-resolution incremental A/D converter with offset and charge injection compensation," *IEEE J. Solid-State Circuits*, vol. SSC-23, no. 3, pp. 736–741, Jun. 1988.

[20] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters: Theory, Design and Simulation*. Piscataway, NJ: IEEE Press, 1997.

[21] M. A. P. Pertijs and J. H. Huijsing, "Transistor temperature measurement for calibration of integrated temperature sensors," in *Proc. IMTC*, May 2002, pp. 755–758.

[22] J. M. Audy and B. Gilbert, "Multiple sequential excitation temperature sensing method and apparatus," U.S. Patent 5,195,827, Mar. 4, 1993.

Michiel A. P. Pertijs (S'99) was born in Roosendaal, The Netherlands, on May 31, 1977. He received the M.Sc. degree in electrical engineering (*cum laude*) from Delft University of Technology in 2000. He is currently working toward the Ph.D. degree at the Electronic Instrumentation Laboratory of the same university, on the subject of high-accuracy CMOS smart temperature sensors.

In 2000, he was an intern with Philips Semiconductors, Sunnyvale, CA, working on analog circuit design. From 1997 to 1999, he worked part-time for EARS B.V., Delft, The Netherlands, on the production and development of a handheld photosynthesis meter. His research interests include analog and mixed-signal interface electronics and smart sensors.

Andrea Niederkorn was born on November 14, 1969, in San Diego, CA. She received the B.S.E.E. degree from the University of Texas, El Paso, in 1991, and the M.S.E.E. degree from Arizona State University, Tempe, in 1996.

Her professional experience has been with electronic sensors, and she is currently with Zoran Corporation developing CMOS image sensors for the mobile communications market.

Xu Ma was born in Beijing, China. He received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, in 1996 and 1999, respectively. He received a second M.S. degree in solid-state circuit design from Arizona State University, Tempe, in 2002.

He joined Philips Semiconductors North America, Tempe, in 2000, where he was engaged in the development of high-accuracy temperature sensor project. He joined Microchip Technology Inc., Chandler, AZ, in 2003. His current interests include micro-controller and mixed- signal circuit design.

Bill McKillop (M'01) received the B.S.E.E. and M.S.E.E. degrees from the University of Arizona, Tucson, in 1997 and 2000.

In 1999, he worked as a Design Engineer in the Magnetic Storage Division for Cirrus Logic, Austin, TX. From 2000 to 2004, he worked as a Design Engineer for the Standard Analog Group for Philips, Tempe, AZ, specializing in power management. He is currently with On Semiconductor, Phoenix, AZ, in the Amplifier Group.

Anton Bakker (S'95–M'00–SM'01) received the M.Sc. and Ph.D. degrees in electrical engineering from the Delft University of Technology, The Netherlands, in 1991 and 2000, respectively.

He was an Assistant Professor at Delft University from 1991 to 2000. In 1997, he started as a consultant for Philips, Sunnyvale, CA, and became a Senior Design Engineer for Philips in 2000. In early 2004, he joined Analog Devices as a Senior Staff Design Engineer. He is author or co-author of over 25 international papers and holds five patents. He wrote the book *High-Accuracy CMOS Smart Temperature Sensors* (Kluwer, 2000).

Johan H. Huijsing (SM'81–F'97) was born on May 21, 1938. He received the M.Sc. degree in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1969, and the Ph.D. degree from the same University in 1981 for his thesis on operational amplifiers.

He has been an Assistant and Associate Professor in electronic instrumentation with the Faculty of Electrical Engineering of the Delft University of Technology since 1969, where he became a full Professor in the Chair of Electronic Instrumentation in 1990, and Professor Emeritus in 2003. From 1982 to 1983, he was a Senior Scientist at Philips Research Laboratories, Sunnyvale, CA. Since 1983, he has been a consultant for Philips Semiconductors, Sunnyvale, and since 1998 also a consultant for Maxim, Sunnyvale. His research work is focused on the systematic analysis and design of operational amplifiers, analog-to-digital converters, and integrated smart sensors. He is author or co-author of some 200 scientific papers, 40 patents, and 9 books, and co-editor of 11 books.

Dr. Huijsing is a Fellow of the IEEE for contributions to the design and analysis of analog integrated circuits. He was awarded the title of Simon Stevin Meester for Applied Research by the Dutch Technology Foundation. He is initiator and co-chairman of the International Workshop on Advances in Analog Circuit Design, which has been held annually since 1992 in Europe. He was a member of the program committee of the European Solid-State Circuits Conference from 1992 to 2002. He was Chairman of the Dutch STW Platform on Sensor Technology and Chairman of the Biennial National Workshop on Sensor Technology from 1991 to 2002.