

**A CMOS temperature sensor with a voltage-calibrated inaccuracy of  $\pm 0.15^{\circ}\text{C}$  ( $3\sigma$ ) from -55 to  $125^{\circ}\text{C}$**

Souri, K; Chae, Y; Makinwa, KAA

**DOI**

[10.1109/JSSC.2012.2214831](https://doi.org/10.1109/JSSC.2012.2214831)

**Publication date**

2013

**Document Version**

Accepted author manuscript

**Published in**

IEEE Journal of Solid State Circuits

**Citation (APA)**

Souri, K., Chae, Y., & Makinwa, KAA. (2013). A CMOS temperature sensor with a voltage-calibrated inaccuracy of  $\pm 0.15^{\circ}\text{C}$  ( $3\sigma$ ) from -55 to  $125^{\circ}\text{C}$ . *IEEE Journal of Solid State Circuits*, 48(1), 292-301. <https://doi.org/10.1109/JSSC.2012.2214831>

**Important note**

To cite this publication, please use the final published version (if applicable). Please check the document version above.

**Copyright**

Other than for strictly personal use, it is not permitted to download, forward or distribute the text or part of it, without the consent of the author(s) and/or copyright holder(s), unless the work is under an open content license such as Creative Commons.

**Takedown policy**

Please contact us and provide details if you believe this document breaches copyrights. We will remove access to the work immediately and investigate your claim.

# A CMOS Temperature Sensor with a Voltage-Calibrated Inaccuracy of $\pm 0.15^{\circ}\text{C}$ ( $3\sigma$ ) from $-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$

Kamran Souri<sup>1</sup>, Youngcheol Chae<sup>2</sup>, and Kofi Makinwa<sup>1</sup>

<sup>1</sup>Electronic Instrumentation Laboratory / DIMES, TU-Delft, Delft, The Netherlands

<sup>2</sup>Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

E-mail: k.souri@ieee.org

**Abstract**—This paper describes the design of a low power, energy-efficient CMOS smart temperature sensor intended for RFID temperature sensing. The BJT-based sensor employs an energy-efficient 2<sup>nd</sup>-order zoom ADC, which combines a coarse 5-bit SAR conversion with a fine 10-bit  $\Sigma\Delta$  conversion. Moreover, a new integration scheme is proposed that halves the conversion time, while requiring no extra supply current. To meet the stringent cost constraints on RFID tags, a fast voltage calibration technique is used, which can be carried out in only 200msec. After batch calibration and an individual room-temperature calibration, the sensor achieves an inaccuracy of  $\pm 0.15^{\circ}\text{C}$  ( $3\sigma$ ) from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Over the same range, devices from a second lot achieved an inaccuracy of  $\pm 0.25^{\circ}\text{C}$  ( $3\sigma$ ) in both ceramic and plastic packages. The sensor occupies  $0.08\text{mm}^2$  in a  $0.16\mu\text{m}$  CMOS process, draws  $3.4\mu\text{A}$  from a 1.5V to 2V supply, and achieves a resolution of 20mK in a conversion time of 5.3msec. This corresponds to a minimum energy dissipation of 27nJ per conversion.

**Keywords:** temperature sensor, smart sensors, sigma-delta modulation, SAR, calibration, and trimming.

## I. Introduction

Combining integrated temperature sensors with Radio Frequency Identification (RFID) tags opens up a wide range of applications e.g. in environmental monitoring, the monitoring of perishable goods and in implantable medical devices. Depending on their source of energy, RFID tags can be classified into passive and active tags. While passive tags scavenge energy from an external RF field, active tags are powered by an internal battery. In the design of temperature-sensing RFID tag, the power and energy efficiency of the co-integrated temperature sensor are important parameters. In the case of a passive tag, the sensor's power consumption limits the maximum operating distance between the tag and an external reader, while in the case of an active tag, the sensor's energy consumption limits battery lifetime. In practice, this means that temperature-sensing RFID tags require sensors that dissipate only a few micro-Watts and consume only a few tens of nano-Joule per conversion [1], [2]. A further requirement is the need for low-cost calibration techniques, due to the extreme cost constraints on RFID tags.

The required accuracy of a temperature-sensing RFID tag depends on the target application, ranging from  $\pm 0.1^{\circ}\text{C}$  for medical applications [3], [4] to  $\pm 1^{\circ}\text{C}$  for food and environmental monitoring applications [5]. Due to process spread, however, such accuracies are only achievable after calibration and trimming [6]. Temperature sensors are usually calibrated by comparing their output with that of a reference sensor at a number of known temperatures. Since both sensors need to reach thermal equilibrium, such thermal calibration can take several tens of seconds, which is incompatible with the low-cost production of RFID tags. In [7], however, a voltage calibration technique, based on electrical rather than thermal measurements, was proposed for BJT-based sensors. Since electrical measurements can be performed relatively

rapidly, this is a promising low-cost calibration technique, whose utility will be further explored in this work.

Various temperature-sensing elements have been used in CMOS temperature sensors. Thermistor-based sensors can be quite energy-efficient [8] - [10], but the large spread (20 – 30%) and non-linear temperature dependence of on-chip resistors means that they typically require multi-point thermal calibration to achieve inaccuracies below  $\pm 0.5^{\circ}\text{C}$  over the military temperature range ( $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ). MOSFETs can also be used to realize low power and energy-efficient temperature sensors [2], [4], [11]. However, the spread in gate oxide thickness and channel doping means that such sensors require one or even two-point thermal calibration to achieve inaccuracies below  $\pm 1^{\circ}\text{C}$  over the military temperature range. BJT-based sensors are much more accurate, requiring only a one-point thermal calibration to achieve inaccuracies less than  $\pm 0.2^{\circ}\text{C}$  ( $3\sigma$ ) [13] - [16]. However, they are not particularly energy efficient, typically dissipating hundreds of nano-Joules per conversion [12].

In this paper, we describe the design of a low power, energy-efficient, low-cost BJT-based temperature sensor for RFID temperature sensing. Compared to our previous work [16], the main difference is the use of a 2<sup>nd</sup>-order switched-capacitor zoom ADC, which when combined with an improved sampling scheme, results in a 25x improvement in energy efficiency compared to the state-of-the-art [12]. Moreover, the sensor is designed to facilitate low-cost voltage calibration. To study the impact of lot-to-lot spread on sensor inaccuracy, measurements on samples from two different process lots are presented. Measurements on samples in both ceramic and plastic packages are also presented in order to assess the impact of the mechanical stress caused by low-cost plastic packaging. The rest of the paper is organized

as follows: in the next section, the operating principle of BJT-based sensors is briefly explained and the sensor's analog front-end topology is described. Section III is devoted to the design of an energy-efficient readout circuit, while section IV describes the implementation details. Realization and measurement results are shown in section V, and the paper ends with conclusions.

## II. Operating Principle

Fig. 1 illustrates the basic operating principle of BJT-based temperature sensors. Two identical substrate PNPs  $Q_R$  and  $Q_L$  are biased at a 1:  $p$  current ratio. The base-emitter voltage  $V_{BE1}$  of  $Q_R$  is a complementary to absolute temperature (CTAT) voltage and can be expressed as follows:

$$V_{BE1} = \eta \cdot (kT/q) \cdot \ln(I_C / I_S) \quad (1)$$

where  $\eta$  is a process dependent non-ideality factor ( $\eta \approx 1$ ),  $k$  is the Boltzmann constant,  $q$  is the electron charge,  $T$  is the temperature in Kelvin,  $I_C$  is the collector current and  $I_S$  is the PNP's saturation current. In contrast to  $V_{BE}$ , the voltage difference  $V_{BE2} - V_{BE1} = \Delta V_{BE}$  is proportional-to-absolute temperature (PTAT):

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \eta \cdot (kT/q) \cdot \ln(p). \quad (2)$$

Conventionally,  $V_{BE}$  (CTAT) and  $\Delta V_{BE}$  (PTAT) are linearly combined to generate a band-gap reference voltage:

$$V_{REF} = V_{BE1} + \alpha \cdot \Delta V_{BE} \quad (3)$$

where  $\alpha$  is a fixed gain factor. An analog-to-digital converter (ADC) then digitizes the ratio between  $\alpha \cdot \Delta V_{BE}$  (PTAT) and the reference voltage  $V_{REF}$ . The digital ratio  $\mu$  is a linear function of temperature and is given by:

$$\mu = \alpha \cdot \Delta V_{BE} / (V_{BE} + \alpha \cdot \Delta V_{BE}). \quad (4)$$

This can then be linearly scaled to obtain a digital output  $D_{out}$  in degrees Celsius:

$$D_{out} = A \cdot \mu - B \quad (5)$$

where  $A$  and  $B$  are constant coefficients:  $A \approx 600$  and  $B \approx 273$  [13].

A key observation is that  $V_{BE}$  and  $\Delta V_{BE}$  contain all the necessary temperature information. Therefore, spending circuit resources to generate an accurate band-gap reference voltage is actually not necessary. Instead, the ratio of  $V_{BE}$  and  $\Delta V_{BE}$  can simply be used as a measure of temperature [16] - [18]. As shown in Fig. 2 (left), for  $p = 5$  the ratio  $X = V_{BE} / \Delta V_{BE}$  is a monotonic, but non-linear function of temperature, which ranges between 6 and 28 from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . Moreover, by rewriting (4), it can be shown that the PTAT function  $\mu$  can then be expressed in terms of  $X$  as follows:

$$\mu = \alpha \cdot \Delta V_{BE} / (V_{BE} + \alpha \cdot \Delta V_{BE}) = \alpha / (\alpha + X) \quad (6)$$

This calculation can be easily implemented in the digital backend. Since  $\alpha$  is a constant in the digital domain, it is immune to process spread. As shown in Fig. 2, the constant  $\alpha$  may be seen as a mapping coefficient between the non-linear  $X$  and PTAT  $\mu$ , which can even be made variable for trimming purposes [16].

In order to minimize the sensor's energy consumption, a fast, low-power ADC is required. This is no trivial matter, since it must also achieve high resolution and accuracy [13]-[15]. Examination of Fig. 1 shows that the choice of a band-gap voltage as the ADC's reference and  $\alpha \cdot \Delta V_{BE}$  as its input signal fundamentally leads to a full-scale range of about  $600^\circ\text{C}$ . With this approach, state-of-the-art accuracy has been achieved over the military temperature range [13]. So in-line with the sensor's expected  $0.2^\circ\text{C}$  inaccuracy [16], the ADC must achieve 12-bit

accuracy and even better resolution to facilitate calibration and trimming. In the following, an ADC architecture is presented that meets these requirements, while also meeting the power and energy constraints of RFID tags.

### III. Zoom-ADC

In most cases, temperature changes are rather slow, and so  $X$  can be digitized by a two-step or zoom ADC that employs a coarse SAR phase and a fine  $\Delta\Sigma$ -ADC phase [16]. As shown in Fig. 3a, the ratio  $X$  ranges from 6 to 28 ( $p=5$ ) over the military temperature range. It can thus be expressed as  $X=n + \mu'$ , where  $n$  and  $\mu'$  are its integer and fractional parts, respectively. The integer  $n$  can then be determined in five successive approximation steps, (Fig. 3a). During the succeeding fine conversion, the references of a  $\Delta\Sigma$ -ADC are chosen so as to zoom into the range between  $n$  and  $(n+1)$ , whereupon the fraction  $\mu'$  can be determined with higher resolution (Fig. 3b). Due to this zoom-in phase, the resolution requirements on the  $\Delta\Sigma$ -ADC are greatly relaxed, leading to simple, low power analog circuitry.

Fig. 4 illustrates the operation of a zoom ADC during the coarse and fine phases. During the coarse conversion phase, a clocked comparator compares  $V_{BE}$  to integer multiples of  $\Delta V_{BE}$  (Fig. 4. a). In five steps, the SAR logic in the feedback loop adjusts the gain factor  $k$  until the integer  $n$  is found. The references of a  $\Delta\Sigma$ -ADC are then set to  $n \cdot \Delta V_{BE}$  and  $(n+1) \cdot \Delta V_{BE}$  as shown in Fig. 4. b. Since the net integrated charge is forced to be approximately zero by the feedback loop, the bitstream average is the desired  $\mu' = (V_{BE} - n \cdot \Delta V_{BE}) / \Delta V_{BE}$ .

In practice, the range in the fine conversion step is doubled so that the input  $X$  is always roughly in the middle of the extended range. This accomodates small errors during the coarse phase and

also ensures that  $X$  lies within the useable range of the  $\Delta\Sigma$  modulator. The necessary information is obtained during a guard-band step, in which  $V_{BE}$  is compared to  $(n+0.5) \cdot \Delta V_{BE}$  [17]. Depending on the result, the references of the  $\Delta\Sigma$ -ADC are then set to either  $(n-1) \cdot \Delta V_{BE}$  and  $(n+1) \cdot \Delta V_{BE}$ , or  $n \cdot \Delta V_{BE}$  and  $(n+2) \cdot \Delta V_{BE}$ . In the rest of the paper, for simplicity, we shall assume that the former is the case.

### A. Improving Conversion Speed

In previous work, a zoom-ADC based on a 1<sup>st</sup>-order  $\Delta\Sigma$ -ADC was used in a low power temperature sensor [16]. Its energy-efficiency, however, was limited by the inherently low conversion rate of its 1<sup>st</sup>-order modulator. Furthermore, to achieve the required 13-bit resolution, an opamp with a DC gain in excess of 80dB was necessary, which in the target 0.16 $\mu$ m CMOS process led to a topology with limited power efficiency.

In this work we propose a 2<sup>nd</sup>-order zoom ADC, which is about 8x faster and requires integrators with lower gain than its 1<sup>st</sup>-order counterpart, thus leading to significantly improved power and energy efficiency. As shown in Fig. 5, it is based on a single-bit feed-forward 2<sup>nd</sup>-order  $\Delta\Sigma$ -ADC. Since  $V_{BE} \sim n \cdot \Delta V_{BE}$  during the fine conversion step, the error signal processed by the loop filter is quite small, thus reducing the output swing of the two opamps. As a result, no extra feed-forward path between the input terminal and the quantizer's input is required, as is the case in the well-known low-swing feed-forward architecture [19]. This simplifies the modulator's implementation, reduces the loading on the analog front-end that generates  $V_{BE}$ , and eliminates a potential source of parasitic coupling into the summing node at the quantizer's input.



## B. An Energy-Efficient Integration Scheme

During the fine conversion, as shown in Fig. 5, every  $\Delta\Sigma$  cycle requires the integration of either  $(V_{BE} - (n-1) \cdot \Delta V_{BE})$  or  $(V_{BE} - (n+1) \cdot \Delta V_{BE})$ , when the comparator's output  $bs$  is either 0 or 1, respectively. For simplicity, let's assume that a charge proportional to  $(V_{BE} - k \cdot \Delta V_{BE})$  is integrated during one  $\Delta\Sigma$  cycle, where  $k$  is either  $(n-1)$  or  $(n+1)$  depending on the polarity of  $bs$ . In [16], this was performed in two clock cycles by a SC integrator. In a first clock cycle a charge proportional to  $V_{BE}$  was integrated, while in a second clock cycle a charge proportional to  $-k \cdot \Delta V_{BE}$  was integrated.

In this work, the two clock cycles are combined i.e. both  $V_{BE}$  and  $\Delta V_{BE}$  are simultaneously sampled and then integrated in *one* clock cycle. As shown in Fig. 6, during the sampling phase  $\phi_1$ ,  $V_{BE}$  is sampled on  $C_S$  while  $-\Delta V_{BE}$  is simultaneously sampled on  $k \cdot C_S$ , thus a charge proportional to  $(V_{BE} - k \cdot \Delta V_{BE})$  is stored on the sampling capacitors. The polarity of both input voltages is swapped during  $\phi_2$ , and therefore a charge proportional to  $2 \cdot (V_{BE} - k \cdot \Delta V_{BE})$  is integrated during *each* clock cycle. Due to the charge cancellation between  $V_{BE}$  and  $-k \cdot \Delta V_{BE}$ , the integrated charge difference is quite small, and can be accommodated by a low-swing, and power-efficient telescopic opamp. This is in contrast with [16], where a folded-cascode opamp was required. Moreover, this approach also halves the conversion time, thus improving the energy efficiency by another factor of two.

## IV. Implementation

### A. Circuit Diagrams

Fig. 7 shows the simplified circuit level diagram of the proposed 2<sup>nd</sup>-order zoom ADC. A

capacitor DAC with 28, 120fF unit capacitances realizes the gain factor  $k$  required for  $\Delta V_{BE}$  amplification, while an extra capacitor  $C_G = 0.5 \cdot C_S$  is used during the guard-band step. To simultaneously sample  $V_{BE}$ , the number of unit elements in the capacitor DAC is increased to 29. During the coarse conversion step, a switch  $S_{bp}$  bypasses the 2<sup>nd</sup> integrator, thus directly connecting the output of the first integrator to the comparator. Moreover, at the start of each comparison step, the first integrator is reset, and therefore it acts as a sample-and-hold.

The first integrator is built around a power-efficient, fully differential telescopic opamp, which draws 600nA, has a gain of 76dB, and a maximum swing of about  $\pm 200$ mV. As shown in Fig. 7, a pseudo-differential inverter-based OTA forms the second integrator [20]. At 25°C, it draws 140nA, occupies only 0.002mm<sup>2</sup>, and has a gain of  $\sim 44$ dB. During  $\phi_2$ , when the output of 1<sup>st</sup> integrator is sampled on capacitors  $C_S$ , the two inverter-based OTAs are in unity-gain configuration and auto-zeroed via offset storing capacitors  $C_{OS}$ . Due to the feedback path through the integration capacitors in  $\phi_1$ , a virtual ground is formed, thus pushing the sampled charge into the integration capacitors  $C_{int2} = 2 \cdot C_S$ . Fig. 8 shows the implementation details of one of the inverter-based OTAs. To decrease the inverter's sensitivity to power supply and process spread, a dynamic current-biasing technique is proposed. During the auto-zeroing phase  $\phi_2$ ,  $M_{NI}$  and  $M_{PI}$  are diode-connected and biased with two current sources (45nA each), while their operating bias voltages are stored on offset storing capacitors  $C_{OS}$ . The bias voltages  $V_{b1}$  and  $V_{b2}$  are chosen such that  $M_{N2}$ ,  $M_{P2}$  are essentially "off" during  $\phi_2$ . The two currents are mirrored from the front-end's precision bias circuit to ensure robustness to supply and process variations. After disconnecting the two current sources in  $\phi_1$ ,  $M_{NI}$  and  $M_{PI}$  are configured as common-source and form a class-AB amplifier, with a virtual ground at  $V_{in}$ . Since the output

voltage swing requirement is reduced to about  $\pm 100\text{mV}$  by the prior coarse conversion step, cascoding of  $M_{NI}$  and  $M_{PI}$  is readily possible, thus enhancing the inverter's output resistance, and hence its DC gain. A passive summation network at the input of quantizer combines the output of 2<sup>nd</sup> integrator with that of the 1<sup>st</sup> integrator via the feed-forward capacitor  $C_{FI}$ , as shown in Fig. 7. To set-up the various biasing voltages, the ADC requires a startup time of 120  $\mu\text{sec}$  (3 clock cycles) before each conversion.

### B. Precision Techniques

During the fine conversion, the accuracy of the ratio  $k$  is determined by the matching between the unit capacitor that samples  $V_{BE}$  and the  $k$  capacitors which sample  $\Delta V_{BE}$ . Any mismatch will lead to a non-linear ADC transfer function. The matching of the references should, therefore, be commensurate with the ADC's target resolution, i.e. 13-bit. Since this cannot be achieved by layout alone, a dynamic element matching (DEM) scheme was used.

Fig. 9 shows the block diagram of the sensor and the timing of a full temperature conversion. The analog front-end consists of a bias circuit and a bipolar core. The bias circuit generates a PTAT current  $I = 90\text{nA}$  (at  $25^\circ\text{C}$ ) with the help of a low power, self-biased chopped opamp and two auxiliary PNPs [16]. Since the transistor's current gain  $\beta_F$  ( $\sim 5$  in the process used) will be impacted by process spread, a  $\beta_F$ -compensation technique is employed to ensure that  $Q_R$  and  $Q_L$  are biased with  $\beta_F$ -independent *collector* currents, thus improving the robustness of the resulting  $V_{BE}$  to process spread. This only requires the addition of a resistor  $R_b/5$  in series with the base of  $Q_{BL}$  [13]. Furthermore, the six current sources and the two bipolar transistors in the bipolar core are dynamically matched to achieve (on average) the accurate 1:5 current ratio

required to generate an accurate  $\Delta V_{BE}$  [13].

A major source of inaccuracy, the offset and  $1/f$  noise of integrators, is reduced by employing correlated-double sampling (CDS) during the coarse and fine conversions [13]. In order to minimize the effect of charge injection, both integrators use differential topologies with minimum-size switches around the integration capacitors. In contrast to [16], a digital rather than the conventional analog implementation of system-level chopping is employed, in order to further lower the modulator's residual offset. As shown in Fig. 9, after an initial coarse conversion, the  $\Delta\Sigma$  conversion is performed twice with swapped input voltage polarities, and the two digital results are then averaged [20]. This eliminates the need for state-preserving choppers around the integration capacitors [13], [16] which simplifies the layout and eliminates a potential source of charge injection, which could otherwise cause ADC non-linearity. Compared to the conventional analog approach, however, this results in a small loss in resolution: up to 0.5 bits if the ADC is quantization-noise limited.

## V. Realization and Measurements

The sensor was realized in a standard 0.16 $\mu\text{m}$  CMOS process with five metal layers, and has an active area of 0.08mm<sup>2</sup>, as shown in Fig. 10. For flexibility, the digital back-end, the control logic and the fine conversion's sinc<sup>2</sup> decimation filter [21] were implemented off-chip. At 25°C, the sensor draws 3.4 $\mu\text{A}$  and operates from a 1.5V to 2V supply with a supply sensitivity of 0.5°C/V. Running at a clock frequency of 25kHz, it requires a conversion time of 5.3msec (128  $\Delta\Sigma$  cycles) to achieve a  $kT/C$  limited resolution of 20mK (rms), which improves to about 5mK (rms) if the conversion time is extended to 100msec. For characterization, 18 devices from one

batch were packaged in ceramic DIL packages and measured over the military temperature range from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . As shown in Fig. 11 the resulting inaccuracy after batch calibration was  $\pm 0.6^{\circ}\text{C}$  ( $3\sigma$ ), with a residual curvature of only  $\pm 0.03^{\circ}\text{C}$ . To further improve the sensor's accuracy, individual calibration and trimming is essential. In the following, two different approaches based on thermal and electrical measurements are presented.

### *A. Thermal Calibration*

Individual calibration of an integrated temperature sensor requires accurate information about its die temperature. Conventionally, this is obtained by bringing the device under test (DUT) and a reference temperature sensor to exactly the same temperature, whereupon the outputs of both devices are logged. In this work, the reference sensor is a platinum Pt-100 resistor calibrated to an inaccuracy of 20 mK. Both sensors are embedded in a large metal block, which acts as a thermal low-pass filter and facilitates measurements with milli-Kelvin stability [22].

Three different single-parameter trimming methods were investigated. First, for each sensor, the offset parameter  $B$  in (5) was adjusted so as to cancel the error at the calibration temperature ( $30^{\circ}\text{C}$ ). After this offset trim, the sensor's inaccuracy is less than  $\pm 0.25^{\circ}\text{C}$  ( $3\sigma$ ) from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . Alternatively, the parameter  $\alpha$  in (6) can be adjusted, as in [16], [17]. The resulting inaccuracy, however, is almost exactly the same as that obtained with offset trim. Since the dominant source of sensor inaccuracy, i.e. the spread in  $V_{BE}$ , is PTAT in nature (see Fig. 11), a digital PTAT trim can also be employed [23]. This is carried out in the digital backend by modifying (5) as follows:

$$D_{out} = A \cdot \frac{\mu}{1 - \gamma_D \mu} - B \quad (7)$$

Here  $\gamma_D$  is a calibration constant that is determined as follows:

$$\gamma_D = \frac{1}{\mu} - \frac{1}{\mu_{ideal}} \quad (8)$$

where  $\mu_{ideal}$  is the desired ratio at the calibration temperature. The resulting inaccuracy is then less than  $\pm 0.15^\circ\text{C}$  ( $3\sigma$ ), as shown in Fig. 12.

### B. Voltage Calibration

Although thermal calibration can be performed very accurately, the long stabilization time required for the DUT and the reference sensor to reach thermal equilibrium prohibits its use as a low-cost calibration method. In [7], a voltage calibration method was proposed, in which die temperature is established by measuring an on-chip  $\Delta V_{BE}$ . By applying DEM to the six current sources and the two PNPs (see Fig. 9), the collector current ratio  $p$ , and therefore  $\Delta V_{BE}$  can be made robust to process spread. The process-dependent non-ideality factor  $\eta$  ( $=1.0042$ ) can also be extracted by batch calibration. As shown in Fig. 13, the die temperature can then be determined by the following procedure. First,  $V_{BE}$  is replaced by an accurate external voltage  $V_{ext}$  (see Fig. 13a). The on-chip ADC then digitizes the ratio  $X_{ext} = V_{ext} / \Delta V_{BE}$  accurately and with high resolution, whereupon the actual die temperature  $T_D$  can be calculated:

$$\begin{aligned} \Delta V_{BE} &= \eta \cdot \frac{kT_D}{q} \cdot \ln(p), & X_{ext} &= \frac{V_{ext}}{\Delta V_{BE}} \\ \Rightarrow T_D &= \frac{V_{ext}}{C_m \cdot X_{ext}}, & C_m &= \eta \cdot \frac{k}{q} \cdot \ln(p) \end{aligned} \quad (9)$$

In a second step,  $V_{ext}$  is replaced by the on-chip  $V_{BE}$  and a normal conversion is performed to

determine  $X = V_{BE} / \Delta V_{BE}$ , and hence the sensor's untrimmed output (see Fig. 13b). In contrast to thermal calibration, this approach can be performed at room temperature, and is much faster, requiring only two ADC conversions. Since the sensor achieves a resolution of 5mK in a conversion time of 100msec, which is commensurate with the expected  $\pm 0.15^\circ\text{C}$  inaccuracy, this means that the total calibration time is only 200msec.

Compared to the results of thermal calibration, the results of voltage calibration followed by an offset or digital PTAT trim are only slightly worse around room temperature. The worst-case inaccuracy from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ , however, is almost exactly the same as shown in Fig. 14. This confirms the fact that the inaccuracy of  $\Delta V_{BE}$  is negligible, and so voltage calibration is a robust alternative to thermal calibration.

### C. Lot-to-lot Spread

To verify the effect of lot-to-lot spread on sensor inaccuracy, devices from a different process lot were characterized. As before, 18 devices from one batch were packaged in ceramic DIL packages and measured from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . Table I compares the resulting inaccuracy and calibration parameters (i.e.  $A$ ,  $B$ , and  $\alpha$ ) of the two lots. As shown, the resulting inaccuracy after batch calibration has increased to  $\pm 0.25^\circ\text{C}$  ( $3\sigma$ ). Moreover, the obtained gain and offset parameters  $A$ ,  $B$  after batch calibration show a lot-to-lot spread of about 0.4% and 0.3%, respectively. Since at room temperature the PTAT ratio  $\mu \approx 0.5$ , this translates to a temperature shift of about  $-0.5^\circ\text{C}$ , from (5). However, the optimal mapping coefficient  $\alpha$  changes by less than 0.1% from lot-to-lot. This small variation can be readily compensated by modifying the calibration parameters ( $A$  and  $B$ ) without sacrificing accuracy, and so  $\alpha$  can be regarded as a digital constant. Finally, the non-ideality factor  $\eta$  only changes by about 0.02% from lot-to-lot,

which corresponds to a maximum calibration error of about 50mK.

#### *D. Plastic Packaging*

In production, low-cost plastic packages are preferred to ceramic packages. The associated mechanical stress, however, impacts the sensor's accuracy, an effect which is referred to as packaging shift [24], and results in a fairly systematic modification to the base-emitter voltage  $V_{BE}$  [25], [26]. To evaluate this, 22 samples from the same batch of the second lot were packaged in plastic DIP packages and then characterized. As shown in Table II, the untrimmed inaccuracy after batch calibration increased to about  $\pm 0.8^\circ\text{C}$  ( $3\sigma$ ). However, a PTAT trim reduced the inaccuracy to about  $\pm 0.25^\circ\text{C}$  ( $3\sigma$ ), which is equivalent to that obtained with ceramic packaging. The optimal mapping coefficient  $\alpha$  changed by about 0.2%, while the fitting parameters  $A$ ,  $B$  changed by about 0.15% and 0.35% respectively, which corresponds to a packaging shift of about  $-0.36^\circ\text{C}$  at room temperature.

From these measurements, it can be concluded that batch calibration is essential to achieving high accuracy over different lots and different packages. Once the fitting parameters  $A$  and  $B$  are known, individual devices can be trimmed on the basis of a fast voltage calibration, since the non-ideality parameter is essentially constant over different lots and packages.

#### *E. Noise and ADC Characteristic*

As in other two-step ADC structures, mismatch between the references used in the various fine conversion steps could result in discontinuities in the ADC's characteristic. To examine this, the ADC's input range was swept by slowly sweeping the oven temperature from  $-40^\circ\text{C}$  to  $100^\circ\text{C}$  over a three hour period, while continuously logging the sensor's output. This



corresponds to a temperature slope of  $\approx 13\text{mK/sec}$ , which implies that the temperature change between successive measurements is less than  $1\text{mK}$ , much smaller than the sensor's own resolution. Taking the difference between successive sensor outputs then results in a pseudo-DNL function, which reflects the ADC's resolution and possible discontinuities between the various fine conversion segments. As shown in Fig. 15, the sensor achieves a resolution of  $20\text{mK}$  (rms) into  $5.3\text{ms}$  around room temperature ( $X \approx 14.5$ ), which is enough to calibrate it rapidly to  $0.2^\circ\text{C}$  inaccuracy. Moreover, there are no discontinuities between the different fine segments. Lastly, it can be seen that the sensor's resolution is slightly temperature dependent. This is due to the fact that the full-scale range of each fine conversion is not constant, but is equal to  $2 \cdot \Delta V_{BE}$ .

#### *F. Comparison to Previous Work*

The sensor's performance is summarized in Table I and compared to other energy-efficient, low power state-of-the-art temperature sensors. It is the only sensor which employs a low-cost, room-temperature voltage calibration technique, and it also achieves the highest accuracy:  $\pm 0.15^\circ\text{C}$  ( $3\sigma$ ) from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . Compared to the other BJT-based sensor, this work achieves comparable resolution in about 18x less conversion time, while consuming 25% less supply current. Fig. 16 compares the sensor's performance in terms of energy/conversion and resolution with several other smart temperature sensors [12]. For two different resolutions and conversion rates ( $0.02^\circ\text{C}$  @  $5.3\text{msec}$  and  $0.005^\circ\text{C}$  @  $100\text{msec}$ ), the sensor achieves nearly the same resolution FoM:  $11\text{pJ}^\circ\text{C}^2$ . In Fig. 17, the energy/conversion versus relative inaccuracy for the same set of sensors is also shown [12]. It can be seen that this work achieves an accuracy FoM of  $0.75\text{nJ}\%^2$ . For the specific class of BJT-based temperature sensors, this represents over

15x improvement and is in line with the performance of state-of-the-art thermistor- and MOSFET-based sensors.

## VI. Conclusions

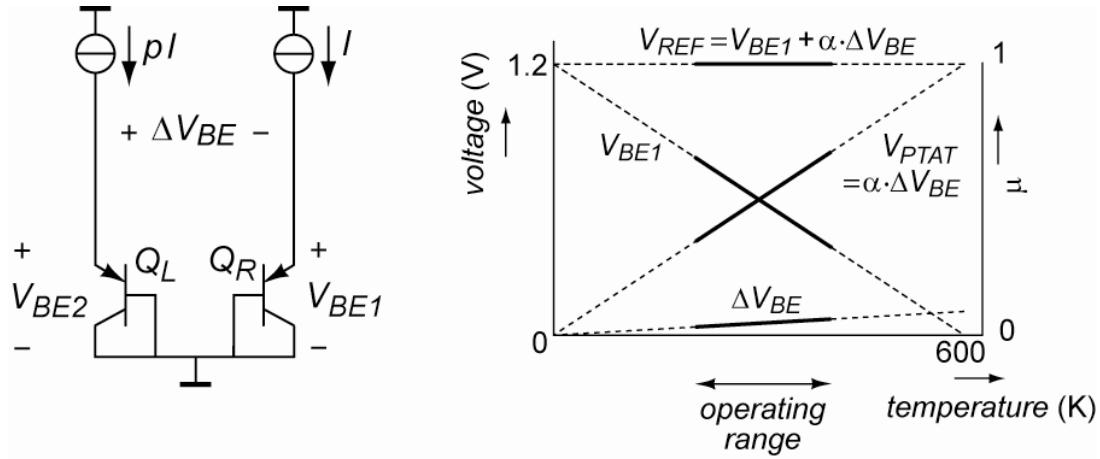
A BJT-based smart temperature sensor for RFID applications has been implemented in a 0.16 $\mu$ m CMOS technology. To meet the extreme low-power, low-energy requirements on RFID tags a 2<sup>nd</sup>-order zoom ADC has been developed. It combines the benefits of SAR- and 2<sup>nd</sup>-order  $\Delta\Sigma$ -ADCs to perform accurate, high resolution readout of the voltages on two sensing BJTs while minimizing power and energy consumption. Moreover, a new charge-balancing scheme is proposed, which reduces ADC conversion time by another factor 2x and allows the use of low-swing, and therefore low-power opamps, thus further improving the sensor's energy efficiency. After an accurate thermal calibration at 30°C and a PTAT trim the sensor achieves an inaccuracy of  $\pm 0.15^\circ\text{C}$  ( $3\sigma$ ) from -55°C to 125°C. To meet the extreme cost constraints on RFID tags, a voltage calibration technique based on electrical measurements was also explored. Compared to thermal calibration, it is significantly faster, requiring only two ADC conversions (200msec), while achieving comparable accuracy.

## References

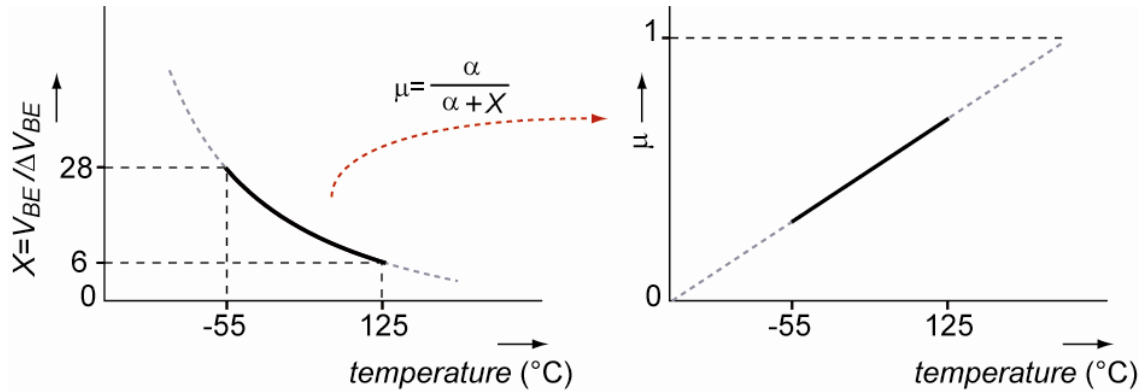
- [1] J. Yin et al., "A System-on-Chip EPC Gen-2 Passive UHF RFID Tag With Embedded Temperature Sensor," *J. Solid-State Circuits*, vol. 45, is. 11, pp. 2404 – 2420, Nov. 2010.
- [2] M. Law, A. Bermark, H.C. Luong, "A Sub- $\mu$ W Embedded Temperature Sensor for RFID Food Monitoring Application," *J. Solid-State Circuits*, vol. 45, is. 6, pp. 1246 – 1255, Dec. 2010.
- [3] G.C.M. Meijer, A.J.M. Boomkamp and R. J. Duguesnoy, "An accurate biomedical temperature transducer with on-chip microcomputer interfacing," *J. Solid-State Circuits*, vol. 23, is. 6, pp. 1405 – 1410, Dec. 1998.
- [4] A. Vaz, et al., "Full Passive UHF Tag With a Temperature Sensor Suitable for Human Body Temperature Monitoring," *TCASII*, vol. 57, is. 2, pp. 95-99, Feb. 2010.
- [5] K. Opasjumruskit et al., "Self-powered wireless temperature sensors exploit RFID technology," *IEEE Pervasive Computing*, vol. 5, pp. 54–61, Mar. 2006
- [6] K.A.A. Makinwa, "Smart Temperature Sensors in Standard CMOS," (*Proc. Eurosenors*) *Procedia Engineering*, pp. 930 – 939, Sept. 2010.
- [7] M.A.P. Pertijs, A.L. Aita, K.A.A. Makinwa and J.H. Huijsing, "Voltage Calibration of Smart Temperature Sensors," *IEEE Sensors*, pp. 756-759, Oct. 2008.
- [8] D. Ruffieux, F. Krummenacher, A. Pezous, G. Spinola-Durante, "Silicon Resonator Based 3.2 $\mu$ W Real Time Clock with  $\pm$ 10ppm Frequency Accuracy," *J. Solid-State Circuits*, vol. 45, is. 1, pp. 224-234, Jan. 2010.
- [9] C-K. Wu, et al., "A 80kS/s 36 $\mu$ W Resistor-based Temperature Sensor using BGR-free SAR ADC with a Unevenly-weighted Resistor String in 0.18 $\mu$ m CMOS," *VLSI*, pp. 222-223, June 2011.
- [10] M. Perrott, et al., "A Temperature-to-Digital Converter for a MEMS-Based Programmable Oscillator with Better Than  $\pm$ 0.5ppm Frequency Stability," *ISSCC*, pp. 206-207, Feb. 2012.
- [11] M. Law, A. Bermark, "A 405-nW CMOS Temperature Sensor based on Linear MOS Operation," *TCAS II*, vol. 56, is. 12, pp. 891 – 895, Dec. 2009.
- [12] K. A. A. Makinwa, "Smart Temperature Sensor Survey", [Online]. Available: [http://ei.ewi.tudelft.nl/docs/TSensor\\_survey.xls](http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls)

- [13] M.A.P. Pertijs, K.A.A. Makinwa, J.H. Huijsing, "A CMOS temperature sensor with a  $3\sigma$  inaccuracy of  $\pm 0.1^\circ\text{C}$  from  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ," *J. Solid-State Circuits*, vol. 40, is. 12, pp. 2805-2815, Dec. 2005.
- [14] A.L. Aita, M.A.P. Pertijs, K.A.A. Makinwa and J.H. Huijsing, "A CMOS Smart Temperature Sensor with a Batch-Calibrated Inaccuracy of  $\pm 0.25^\circ\text{C}$  ( $3\sigma$ ) from  $-70^\circ\text{C}$  to  $130^\circ\text{C}$ ," *ISSCC*, pp. 342-343, Feb. 2009.
- [15] F. Sebastiano et al., "A 1.2-V 10- $\mu\text{W}$  NPN-Based Temperature Sensor in 65-nm CMOS with an Inaccuracy of  $0.2^\circ\text{C}$  ( $3\sigma$ ) From  $70^\circ\text{C}$  to  $125^\circ\text{C}$ ," *J. Solid-State Circuits*, vol. 45, is. 99, pp. 2591-2601, Dec. 2010.
- [16] K. Souri and K.A.A. Makinwa, "A  $0.12\text{mm}^2$  7.4 $\mu\text{W}$  Micropower Temperature Sensor with an Inaccuracy of  $\pm 0.2^\circ\text{C}$  ( $3\sigma$ ) from  $-30^\circ\text{C}$  to  $125^\circ\text{C}$ ," *J. Solid-State Circuits*, vol. 46, is. 7, pp. 1693-1700 July. 2011.
- [17] K. Souri, M. Kashmiri, K.A.A. Makinwa, "A CMOS Temperature Sensor with an Energy-Efficient Zoom ADC and an Inaccuracy of  $\pm 0.25^\circ\text{C}$  ( $3\sigma$ ) from  $-40$  to  $125^\circ\text{C}$ ," *ISSCC*, pp. 310-311, Feb. 2010.
- [18] Y.W. Li et al., "A 1.05V 1.6mW  $0.45^\circ\text{C}$   $3\sigma$ -Resolution  $\Delta\Sigma$ -Based Temperature Sensor with Parasitic-Resistance Compensation in 32nm CMOS," *ISSCC*, pp. 340-341, Feb., 2009.
- [19] K. Y. Nam, S.-M. Lee, D. K. Su and B. A. Wooley, "A Low-Voltage Low-Power Sigma-Delta Modulator for Broadband Analog-to-Digital Conversion," *J. Solid-State Circuits*, vol. 40, is. 9, pp. 1855-1864, Sept. 2005.
- [20] Y. Chae, and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta Sigma Modulator," *J. Solid-State Circuits*, vol. 44, is. 2, pp. 458 – 472, Feb. 2009.
- [21] J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental delta-sigma converters," *TCAS I*, vol. 51, no. 4, pp. 678–690, Apr. 2004.
- [22] K. Souri and K.A.A. Makinwa, "Ramp Calibration of Temperature Sensors," *IWASI*, pp. 282-285, June. 2011.
- [23] M. A. P. Pertijs and J. H. Huijsing, "Precision Temperature Sensors in CMOS Technology," *Springer*, The Netherlands, 2006.
- [24] A. Hastings, The art of analog layout. New Jersey: Prentice Hall, 2001.

- [25] F. Fruett, G. C. M. Meijer, and A. Bakker, "Minimization of the mechanical-stress-induced inaccuracy in bandgap voltage references," *J. Solid-State Circuits*, vol. 38, is. 7, pp. 1288-1291, July. 2003.
- [26] J. F. Creemer, F. Fruett, G. C. Meijer, and P. J. French, "The piezojunction effect in silicon sensors and circuits and its relation to piezoresistance," *IEEE Sensors Journal*, vol. 1, no. 2, pp. 98–108, Aug. 2001.



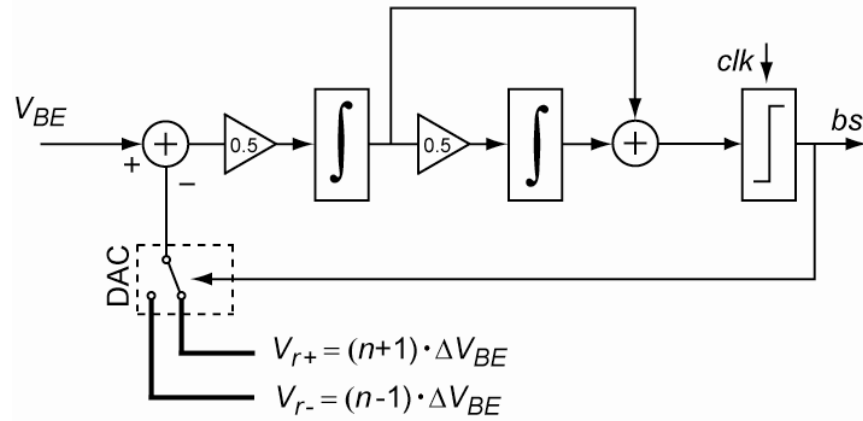
**Fig. 1** Two substrate PNPs generate the required voltages ( $V_{PTAT}$  and  $V_{REF}$ ) for a ratiometric temperature measurement.



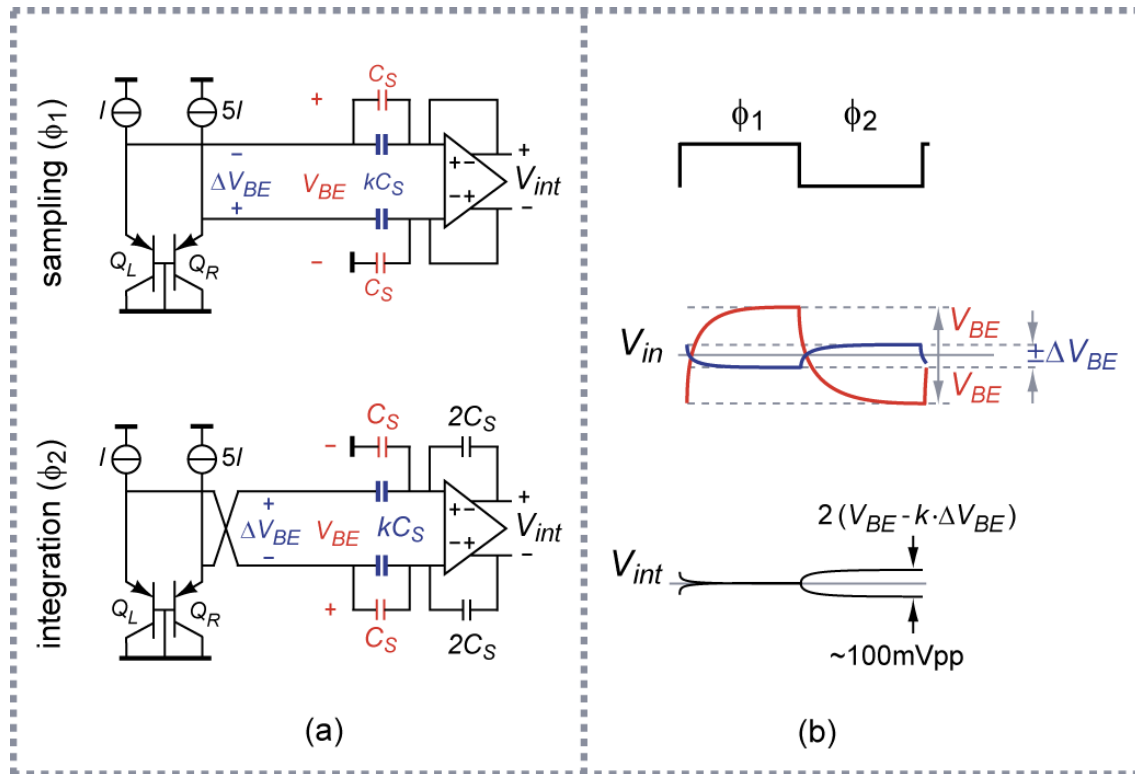
**Fig. 2** Non-linear  $X = V_{BE} / \Delta V_{BE}$  ( $p=5$ ) and linearized  $\mu = \alpha / (\alpha + X)$  as a function of temperature.

**Fig. 3** Temperature dependence of  $X = n + \mu'$  from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The integer  $n$  ranges between 6 and 28 (a) while the fraction  $\mu'$  ranges between 0 and 1 (b).

**Fig. 4** Block diagram of the zoom ADC during the coarse (a) and fine (b) conversions.

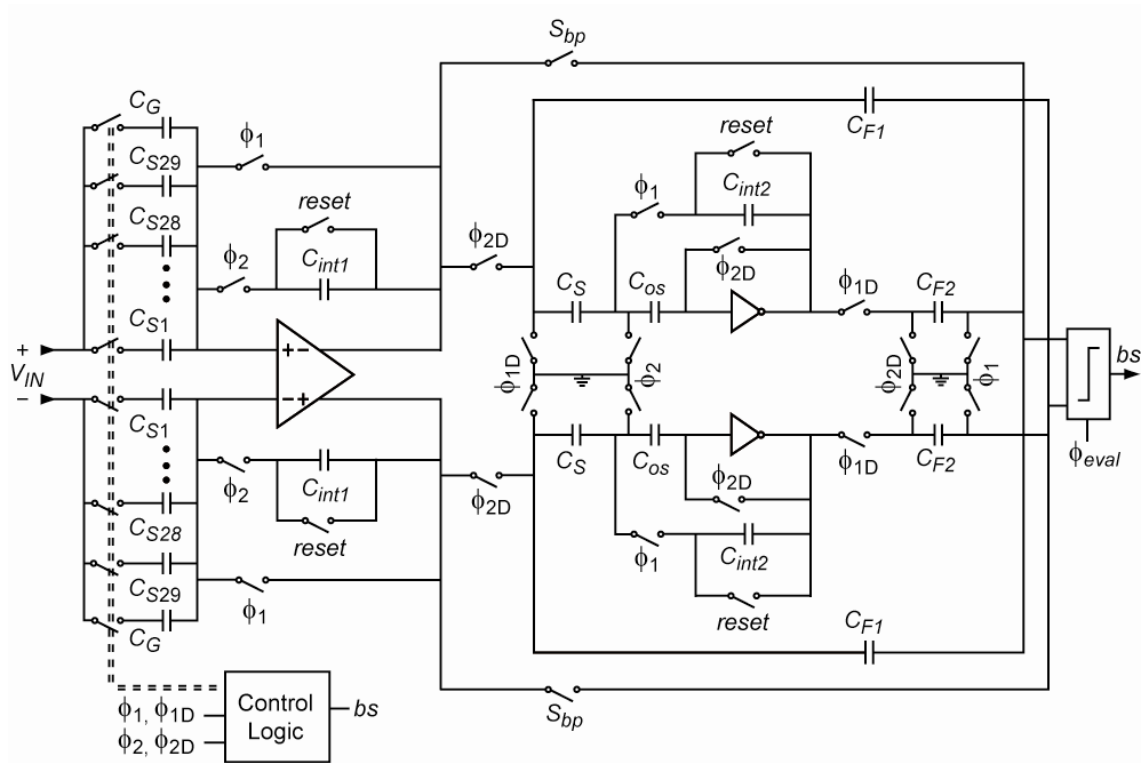


**Fig. 5** Block diagram of the proposed 2<sup>nd</sup>-order zoom ADC during the fine conversion.

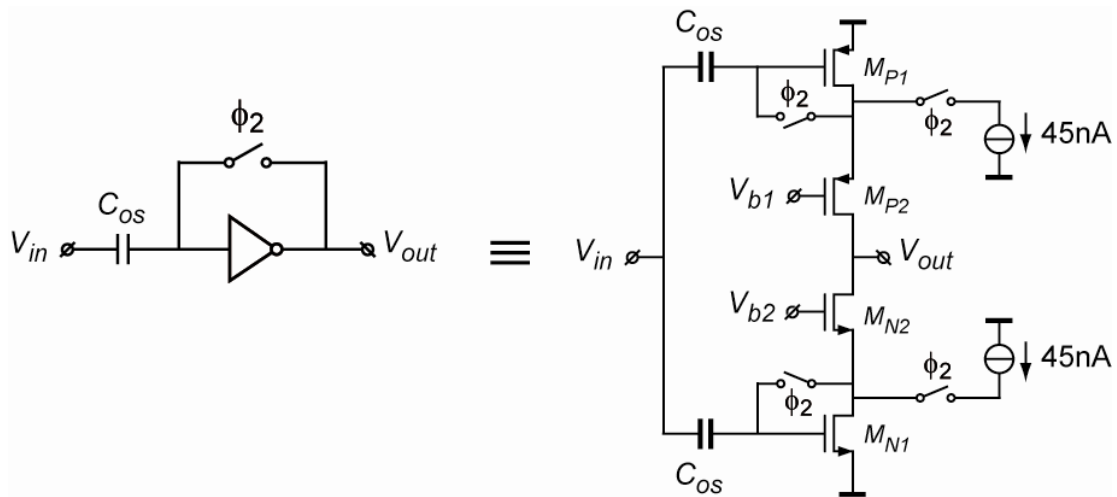


**Fig. 6** (a) Proposed integration scheme during sampling ( $\phi_1$ ) and integration ( $\phi_2$ ) phases. (b) Waveforms of a full SAR/ $\Delta\Sigma$  cycle.  $V_{in}$ : zoom ADC's input voltage,  $V_{int}$ : integrator's output voltage. Parameter  $k$  is set by the SAR logic in the coarse conversion, while  $k = n-1$  or  $n+1$  when  $bs = 0$  or  $1$  in the fine conversion step.

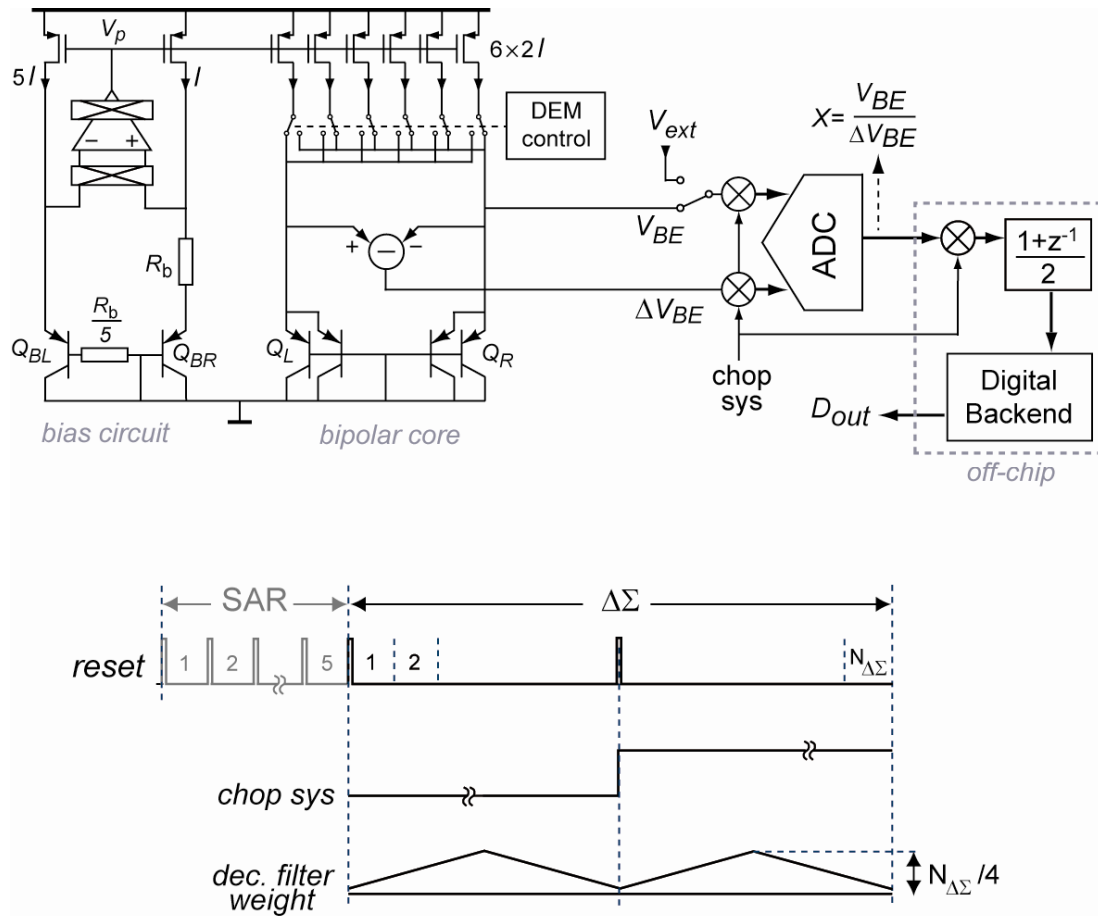




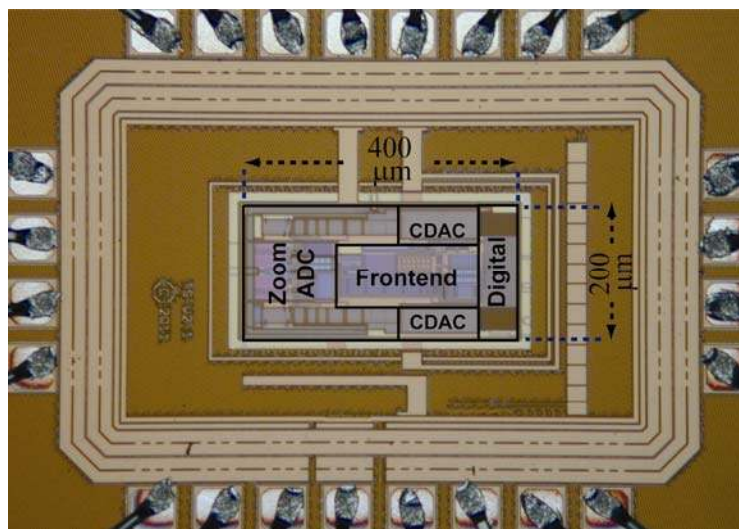
**Fig. 7** Simplified circuit diagram of the proposed 2<sup>nd</sup>-order zoom ADC.



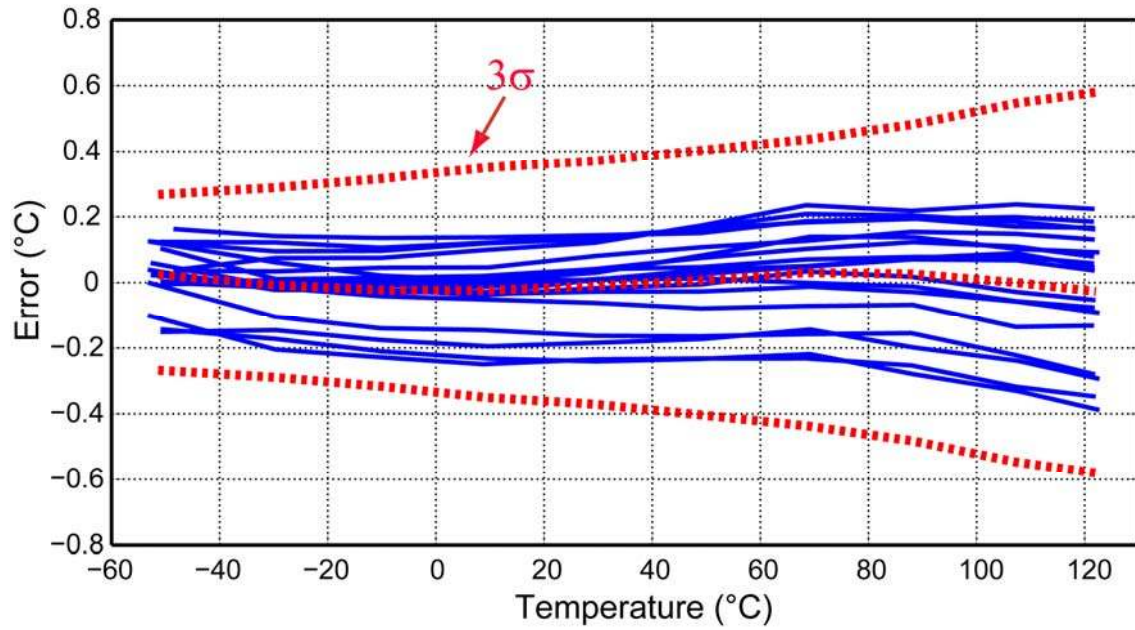
**Fig.8** Circuit diagram of the proposed inverter-based OTA.



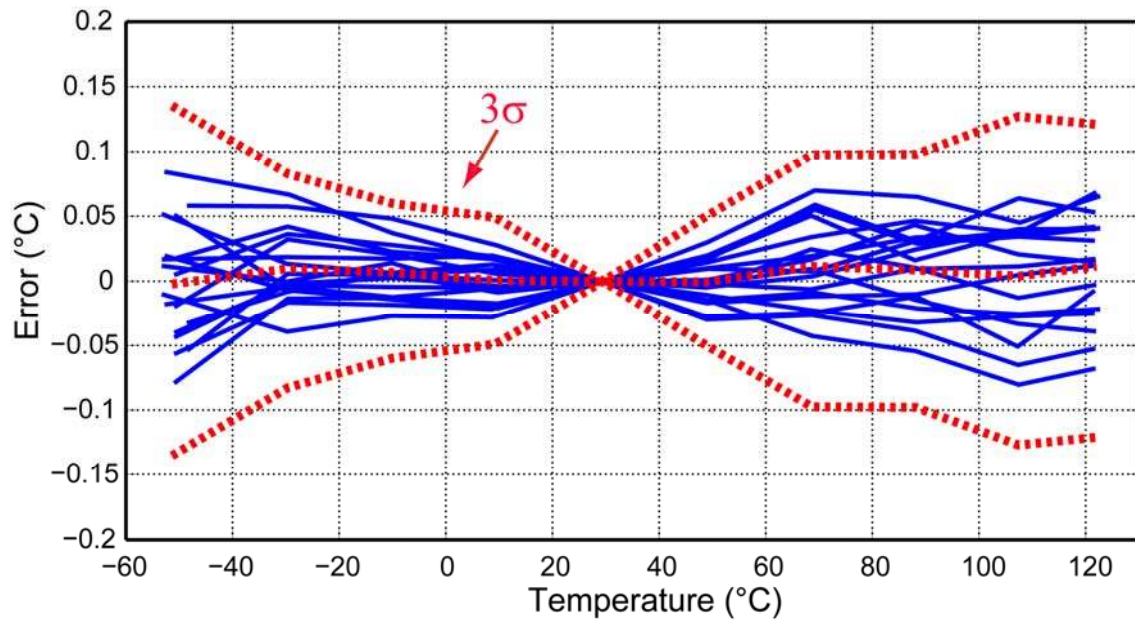
**Fig. 9** Top: Block diagram of the temperature sensor. Bottom: timing diagram of a full temperature conversion.



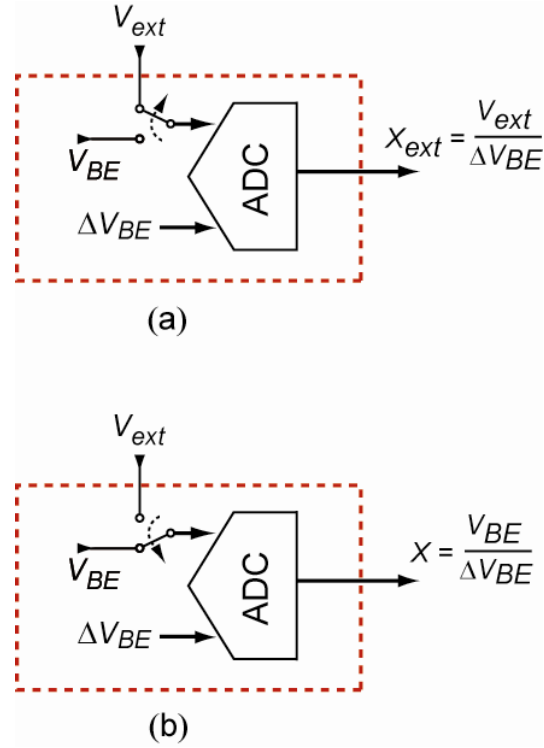
**Fig. 10** Chip micrograph of the sensor.



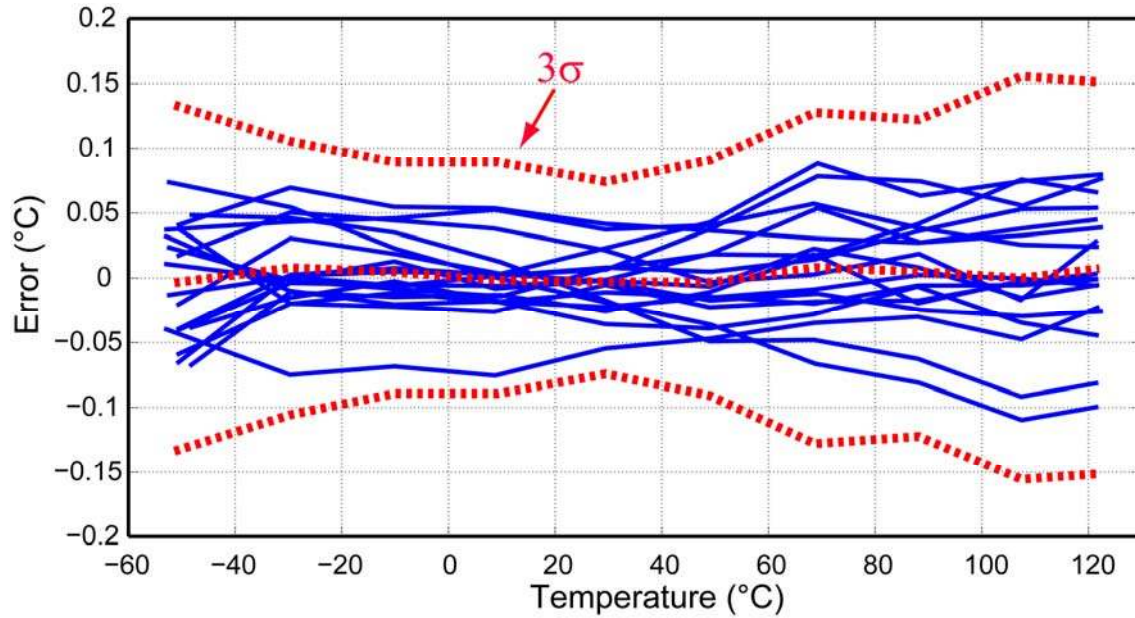
**Fig. 11** Measured temperature error of 18 sensors before trimming; dashed lines refer to the average and  $\pm 3\sigma$  limits.



**Fig. 12** Measured temperature error of 18 sensors after thermal calibration and PTAT trimming at 30°C; dashed lines refer to the average and  $\pm 3\sigma$  limits.



**Fig. 13** Voltage calibration requires only two ADC conversions: first the actual die temperature is obtained (a) and then a normal conversion gives the untrimmed output (b).



**Fig. 14** Measured temperature error of 18 sensors after voltage calibration and PTAT trimming at room temperature; dashed lines refer to the average and  $\pm 3\sigma$  limits.

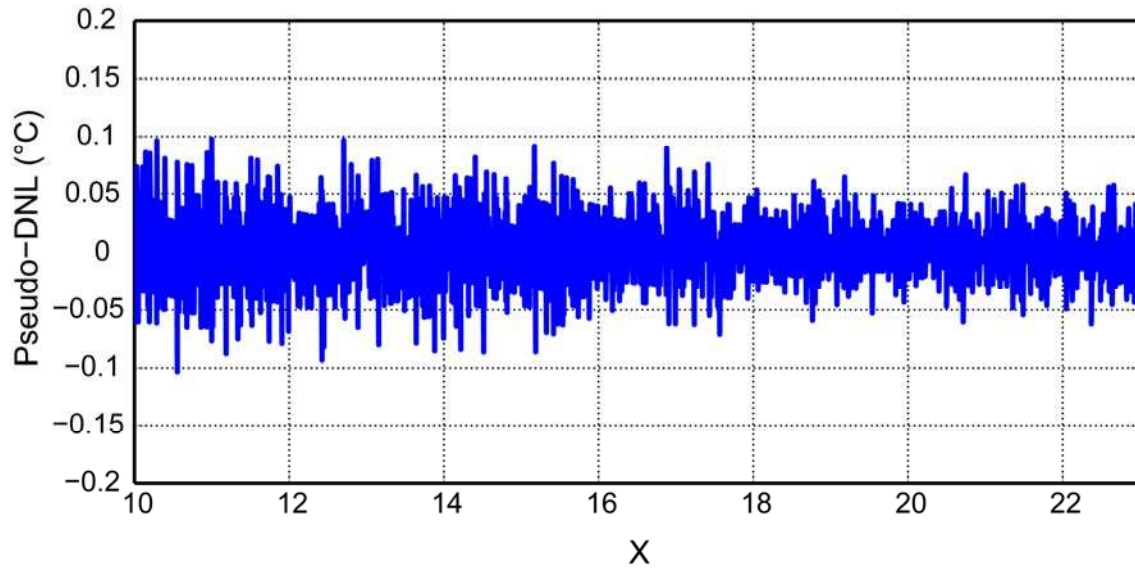
|   | <b>Lot-1</b>               | <b>Lot-2</b>               |
|---|----------------------------|----------------------------|
| <b>Untrimmed inaccuracy (<math>3\sigma</math>)</b>    | $\pm 0.6^{\circ}\text{C}$  | $\pm 0.6^{\circ}\text{C}$  |
| <b>PTAT-trimmed inaccuracy (<math>3\sigma</math>)</b> | $\pm 0.15^{\circ}\text{C}$ | $\pm 0.25^{\circ}\text{C}$ |
| <b><math>\alpha</math> (mapping coefficient)</b>      | 15.44                      | 15.45                      |
| <b>A (gain parameter)</b>                             | 613.31                     | 610.74                     |
| <b>B (offset parameter)</b>                           | 283.70                     | 282.93                     |
| <b><math>\eta</math> (non-ideality factor)</b>        | 1.0042                     | 1.0044                     |

**Table I.** Impact of lot-to-lot spread on sensor accuracy and calibration parameters.

|   | <b>Ceramic Package</b>     | <b>Plastic Package</b>     |
|---|----------------------------|----------------------------|
| <b>Untrimmed inaccuracy (<math>3\sigma</math>)</b>    | $\pm 0.6^{\circ}\text{C}$  | $\pm 0.8^{\circ}\text{C}$  |
| <b>PTAT-trimmed inaccuracy (<math>3\sigma</math>)</b> | $\pm 0.25^{\circ}\text{C}$ | $\pm 0.25^{\circ}\text{C}$ |
| <b><math>\alpha</math> (mapping coefficient)</b>      | 15.45                      | 15.47                      |
| <b>A (gain parameter)</b>                             | 610.74                     | 611.59                     |
| <b>B (offset parameter)</b>                           | 282.93                     | 283.94                     |
| <b><math>\eta</math> (non-ideality factor)</b>        | 1.0044                     | 1.0044                     |

**Table II.** Effect of mechanical stress on sensor accuracy and calibration parameters.





**Fig. 15** Measured Pseudo-DNL versus  $X$ . The sensor's conversion time is 5.3msec.

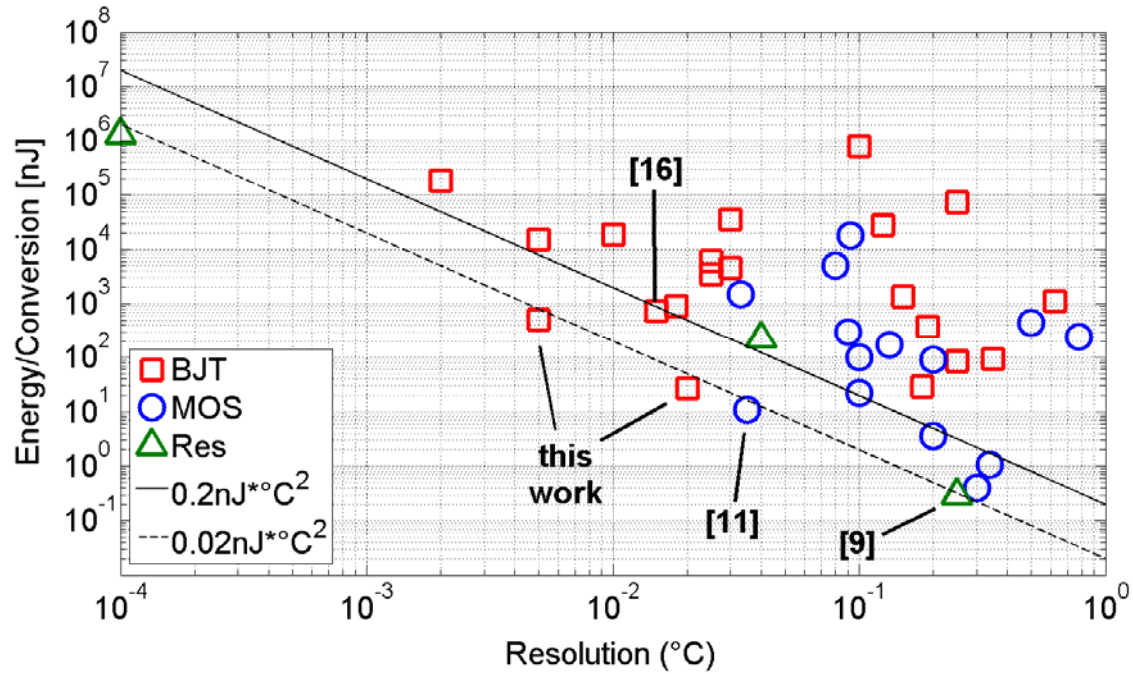
| Parameter                        | This work   | [16]                                       | [9]                                      | [11]                                     |
|----------------------------------|---|--|--|--|
| Sensor type                      | <b>BJT</b>  | BJT  | Resistor                                 | MOSFET                                   |
| CMOS Technology                  | <b>0.16<math>\mu</math>m</b>  | 0.16 $\mu$ m                               | 0.18 $\mu$ m                             | 0.18 $\mu$ m                             |
| Chip area                        | <b>0.08mm<sup>2</sup></b>   | 0.12mm <sup>2</sup>                        | 0.18mm <sup>2</sup>                      | 0.032mm <sup>2</sup>                     |
| Supply current <sup>†</sup>      | <b>3.4<math>\mu</math>A</b>   | 4.6 $\mu$ A                                | 20 $\mu$ A                               | 0.4 $\mu$ A                              |
| Supply voltage                   | <b>1.5V to 2V</b>   | 1.6V to 2V                                 | 1.2-2.0V                                 | 0.9-1.1V                                 |
| Supply sensitivity               | <b>0.5°C/V</b>  | 0.1°C/V                                    | 0.625°C/V                                | 8°C/V                                    |
| Inaccuracy                       | <b><math>\pm 0.15^\circ\text{C}</math> (3<math>\sigma</math>)</b>       | $\pm 0.2^\circ\text{C}$ (3 $\sigma$ )      | $\pm 0.5^\circ\text{C}$ (max)            | $-0.8/+1^\circ\text{C}$ (max)            |
| Temperature range                | <b><math>-55^\circ\text{C}</math> to <math>125^\circ\text{C}</math></b> | $-30^\circ\text{C}$ to $125^\circ\text{C}$ | $0^\circ\text{C}$ to $100^\circ\text{C}$ | $0^\circ\text{C}$ to $100^\circ\text{C}$ |
| Calibration (points)             | <b>voltage (1)</b>  | thermal (1)                                | thermal (1)                              | thermal (2)                              |
| Resolution ( $T_{\text{conv}}$ ) | <b>0.02°C (5.3ms)<br/>0.005°C (100ms)</b>                               | 0.015°C (100ms)                            | 0.25°C (12.5 $\mu$ s)                    | 0.3°C (1ms)                              |
| Resolution FoM <sup>†</sup>      | <b>11pJ°C<sup>2</sup></b>   | 170pJ°C <sup>2</sup>                       | 19pJ°C <sup>2</sup>                      | 32pJ°C <sup>2</sup>                      |
| Accuracy FoM <sup>†</sup>        | <b>0.75nJ%<sup>2</sup></b>  | 49nJ% <sup>2</sup>                         | 0.3nJ% <sup>2</sup>                      | 1.17nJ% <sup>2</sup>                     |

Res. FoM=Energy/Conversion $\times$ (Resolution)<sup>2</sup>, Acc. FoM= Energy/Conversion $\times$ (Relative inaccuracy)<sup>2</sup>

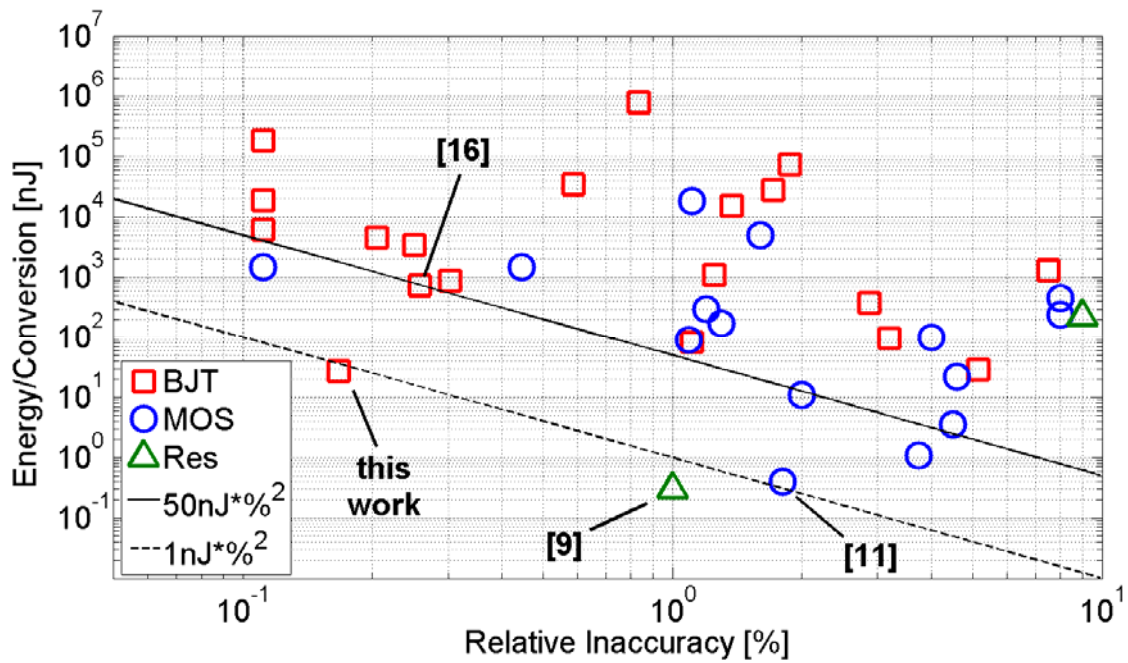
Relative inaccuracy (%) = 100 $\times$ Max Error/Specified temperature range

<sup>†</sup> Excluding the off-chip digital

**Table III.** Performance summary and comparison to previous work.



**Fig. 16** Energy per conversion versus resolution for different smart temperature sensors using different sensing principles [12].



**Fig. 17** Energy per conversion versus relative inaccuracy for different smart temperature sensors using different sensing principles [12].



**Kamran Souri** (S'10) received his B.Sc. in Electronics and M.Sc. in Telecommunications from Amirkabir University of Technology, Iran, in 2001 and 2004, respectively. From 2001 to 2007, he worked at PSP-Ltd, Tehran, Iran, designing embedded systems for use in high quality audio/video teleconferencing systems, KVM switches, and BMS systems.

In Sept. 2007 he joined the Electrical Instrumentation Laboratory, Faculty of Electrical Engineering, Delft University of Technology, Delft, the Netherlands where he received an M.Sc. degree in Microelectronics (*cum laude*) in 2009. Since 2008, he has been an intern with NXP-Semiconductors, Eindhoven. He is currently a Ph.D. candidate at Delft University of Technology focusing on the design of ultra-low-power/energy-efficient CMOS smart temperature sensors for RFID application. His research interests include the design of low-power, energy-efficient sensor interfaces, data converters, and precision analog circuits.

**Affiliation:** Electronic Instrumentation Laboratory / DIMES, Delft University of Technology, Delft, the Netherlands.

**Postal address:** Mekelweg 4, room 13.080, Delft, the Netherlands





**Youngcheol Chae** (M'09) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, Korea in 2003, 2005 and 2009, respectively.

From 2009 to 2011, he was with Delft University of Technology in the Netherlands, as a post doctoral researcher. In 2012, he joined Yonsei University as an Assistant Professor. His main research interests are in the design of precision analog circuits, sensor interface circuits, CMOS image sensors, and delta-sigma ADCs. This has resulted in 12 patents and over 35 technical papers.

Dr. Chae received a Gold Prize (1st) at Human-Tech Thesis Award (14th) from Samsung Electronics in 2008, and the TMS Best Paper Award from Yonsei University in 2007 and 2008, respectively. In 2011, he received a VENI Award from the Netherlands Organization for Scientific Research.

**Affiliation:** Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

**Postal address:** 262, Seongsanno, Seodaemun-gu, Yonsei University, Seoul, Korea



**Kofi A. A. Makinwa** (M'97–SM'05–F'11) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Nigeria in 1985 and 1988 respectively. In 1989, he received the M.E.E. degree from the Philips International Institute, The Netherlands and in 2004, the Ph.D. degree from Delft University of Technology, The Netherlands.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, The Netherlands, where he worked on interactive displays and on front-ends for optical and magnetic recording systems. In 1999, he joined Delft University of Technology, where he is now an Antoni van Leeuwenhoek Professor in the Faculty of Electrical Engineering, Computer Science and Mathematics. His main research interests are in the design of precision analog circuitry, sigma-delta modulators, smart sensors and sensor interfaces. This has resulted in 3 books, 18 patents and over 150 technical papers.

Kofi Makinwa is on the program committees of the European Solid-State Circuits Conference (ESSCIRC) and the Advances in Analog Circuit Design (AACD) workshop. He has also served on the program committee of the International Solid-State Circuits Conference (ISSCC), as a guest editor of the Journal of Solid-State Circuits (JSSC) and as a distinguished lecturer of the IEEE Solid-State Circuits Society (2008 to 2011). He is a co-recipient of several best paper awards: from the JSSC, ISSCC, Transducers and ESSCIRC, among others. In 2005, he received a Veni Award from the Netherlands Organization for Scientific Research and the Simon Stevin Gezel Award from the Dutch Technology Foundation. He is an alumnus of the Young Academy of the Royal Netherlands Academy of Arts and Sciences and an elected member of the IEEE Solid-State Circuits Society AdCom, the society's governing board.

**Affiliation:** Electronic Instrumentation Laboratory / DIMES, Delft University of Technology, Delft, the Netherlands.

**Postal address:** Mekelweg 4, room 13.270, Delft, the Netherlands

## IEEE COPYRIGHT AND CONSENT FORM

To ensure uniformity of treatment among all contributors, other forms may not be substituted for this form, nor may any wording of the form be changed. This form is intended for original material submitted to the IEEE and must accompany any such material in order to be published by the IEEE. Please read the form carefully and keep a copy for your files.

**TITLE OF PAPER/ARTICLE/REPORT, INCLUDING ALL CONTENT IN ANY FORM, FORMAT, OR MEDIA (hereinafter, "the Work"):**

*A CMOS Temperature Sensor with a Voltage-Calibrated Inaccuracy of 0.25°C From -55 to 125°C*

**COMPLETE LIST OF AUTHORS:** *Kamran Souri - Youngcheol Chae - Kofi Makinwa*

**IEEE PUBLICATION TITLE (Journal, Magazine, Conference, Book):** *Journal of Solid-State Circuits*

### COPYRIGHT TRANSFER

1. The undersigned hereby assigns to The Institute of Electrical and Electronics Engineers, Incorporated (the "IEEE") all rights under copyright that may exist in and to: (a) the above Work, including any revised or expanded derivative works submitted to the IEEE by the undersigned based on the Work; and (b) any associated written or multimedia components or other enhancements accompanying the Work.

### CONSENT AND RELEASE

2. In the event the undersigned makes a presentation based upon the Work at a conference hosted or sponsored in whole or in part by the IEEE, the undersigned, in consideration for his/her participation in the conference, hereby grants the IEEE the unlimited, worldwide, irrevocable permission to use, distribute, publish, license, exhibit, record, digitize, broadcast, reproduce and archive, in any format or medium, whether now known or hereafter developed: (a) his/her presentation and comments at the conference; (b) any written materials or multimedia files used in connection with his/her presentation; and (c) any recorded interviews of him/her (collectively, the "Presentation"). The permission granted includes the transcription and reproduction of the Presentation for inclusion in products sold or distributed by IEEE and live or recorded broadcast of the Presentation during or after the conference.

3. In connection with the permission granted in Section 2, the undersigned hereby grants IEEE the unlimited, worldwide, irrevocable right to use his/her name, picture, likeness, voice and biographical information as part of the advertisement, distribution and sale of products incorporating the Work or Presentation, and releases IEEE from any claim based on right of privacy or publicity.

4. The undersigned hereby warrants that the Work and Presentation (collectively, the "Materials") are original and that he/she is the author of the Materials. To the extent the Materials incorporate text passages, figures, data or other material from the works of others, the undersigned has obtained any necessary permissions. Where necessary, the undersigned has obtained all third party permissions and consents to grant the license above and has provided copies of such permissions and consents to IEEE.

☐ Please check this box if you do not wish to have video/audio recordings made of your conference presentation.  
See reverse side for Retained Rights/Terms and Conditions, and Author Responsibilities.

### GENERAL TERMS

- The undersigned represents that he/she has the power and authority to make and execute this assignment.
- The undersigned agrees to indemnify and hold harmless the IEEE from any damage or expense that may arise in the event of a breach of any of the warranties set forth above.
- In the event the above work is not accepted and published by the IEEE or is withdrawn by the author(s) before acceptance by the IEEE, the foregoing copyright transfer shall become null and void and all materials embodying the Work submitted to the IEEE will be destroyed.
- For jointly authored Works, all joint authors should sign, or one of the authors should sign as authorized agent for the others.

(1) *Kamran Souri*  
Author/Authorized Agent for Joint Authors

*10-August-2012*  
Date

### U.S. GOVERNMENT EMPLOYEE CERTIFICATION (WHERE APPLICABLE)

This will certify that all authors of the Work are U.S. government employees and prepared the Work on a subject within the scope of their official duties. As such, the Work is not subject to U.S. copyright protection.

(2) \_\_\_\_\_  
Authorized Signature

\_\_\_\_\_  
Date

(Authors who are U.S. government employees should also sign signature line (1) above to enable the IEEE to claim and protect its copyright in international jurisdictions.)

### CROWN COPYRIGHT CERTIFICATION (WHERE APPLICABLE)

This will certify that all authors of the Work are employees of the British or British Commonwealth Government and prepared the Work in connection with their official duties. As such, the Work is subject to Crown Copyright and is not assigned to the IEEE as set forth in the first sentence of the Copyright Transfer Section above. The undersigned acknowledges, however, that the IEEE has the right to publish, distribute and reprint the Work in all forms and media.

(3) \_\_\_\_\_  
Authorized Signature

\_\_\_\_\_  
Date

(Authors who are British or British Commonwealth Government employees should also sign line (1) above to indicate their acceptance of all terms other than the copyright transfer.)  
rev. 020711