A CMOS Transconductance-C Filter Technique for Very High Frequencies

Bram Nauta, *Student Member, IEEE*

Abstract—**This paper presents CMOS circuits for integrated analog filters at very high frequencies, based on transconductance-C integrators. First a differential transconductance element based on CMOS inverters is described. With this circuit a linear, tunable integrator for very-high-frequency integrated filters can be made. This integrator has good linearity properties (1% relative *gm* error for 2-$V_{p\text{-}p}$ input signals, V_{dd} = 10 V) and nondominant poles in the gigahertz range owing to the absence of internal nodes. The integrator has a tunable dc gain, resulting in a controllable integrator quality factor. Experimental results of a VHF CMOS transconductance-C low-pass filter realized in a 3-μm CMOS process are given. Both the cutoff frequency and the quality factors can be tuned. The cutoff frequency was tuned from 22 to 98 MHz and the measured filter response is very close to the ideal response of the passive prototype filter. Furthermore, a novel circuit for automatically tuning the quality factors of integrated filters built with these transconductors is described. The *Q*-tuning circuit itself has no signal-carrying nodes and is therefore extremely suitable for these filters at very high frequencies.**

I. Introduction

SEVERAL MOS continuous-time high-frequency integrated filters have been reported in the literature [1]–[7]. Most filters are built with transconductance elements and capacitors, to take advantage of these structures for making integrators at high frequencies. The maximal cutoff frequencies were, however, limited to the lower megahertz range. Krummenacher and Joehl [1], for example, reported a 4-MHz low-pass filter and Kim and Geiger [2] reported a bandpass filter, programmable up to 16 MHz. Pu and Tsividis [3] have described another approach: minimal transistor-only VHF filters. With this technique very compact filters at very high frequencies (10–100 MHz) can be made, but these filters have restricted quality factors and accuracy. This paper describes a filter technique for accurate filters at very high frequencies. The basic building block is an integrator and general filter synthesis techniques remain applicable.

The integrator is the main building block of integrated active filters. In this paper the integrator will be implemented by a transconductance element loaded with a capacitor. One of the major problems in high-frequency active filters is the phase error of the integrators [4], [8]. The quality factors Q of the poles and zeros in the filter are highly sensitive to the phase of the integrators at the pole and zero frequencies. To avoid errors in the filter characteristic, a sufficiently high integrator dc gain is required, while the parasitic poles should be located at frequencies much higher than the cutoff frequency of the filter, in order to keep the integrator phase close to $-90°$. For the filter to be presented, this implies a dc gain of roughly at least 40 dB and parasitic poles located at least a factor of 100 beyond the cutoff frequency. This is a strong constraint for filters at very (up to 100 MHz) high frequencies: the transconductor should have a bandwidth of approximately 10 GHz.

Two techniques can be used to make a combination of a high integrator dc gain with a very large bandwidth possible.

1) Consider the balanced transconductance-C integrator of Fig. 1(a). If the transconductance element has *no internal nodes*,[1] then the transconductor circuit has no parasitic poles or zeros influencing the transfer function of the integrator. This is true under the condition that the capacitors C_i (or C_i') and C_L (or C_L') are functional for the filter transfer. The feedforward currents through the capacitances C_{ov} are canceled in a fully balanced gyrator structure [4].

2) Consider the balanced integrator of Fig. 1(b). The dc gain of the integrator is $gm \times r_{out}$, where r_{out} is the parasitic output resistance of the transconductor. For short-channel MOS transistors in high-frequency applications, this dc gain is normally very low (≈ 20). The dc gain can be increased by loading the transconductor—at least for differential signals—with a *negative resistance* (r_{load}) that compensates r_{out}. The dc gain is now gm times the parallel combination of r_{out} and r_{load}. For $r_{load} = -r_{out}$ the dc gain becomes, theoretically, infinite. Note that the implementation of the dc-gain enhancement technique does not require any internal node. Cascoding or cascading of stages, on the contrary, will always introduce additional internal nodes resulting in phase errors.

A combination of these two techniques for the design of a transconductance element results in an integrator with

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The author was with MESA Twente, University of Twente, 7500 AE, Enschede, The Netherlands. He is now with Philips Research Laboratories, 5600 JA, Eindhoven, The Netherlands.

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[1] An internal node is a node in the circuit schematic that has no direct connection to either an input or an output terminal or a bias or supply terminal of the circuit.

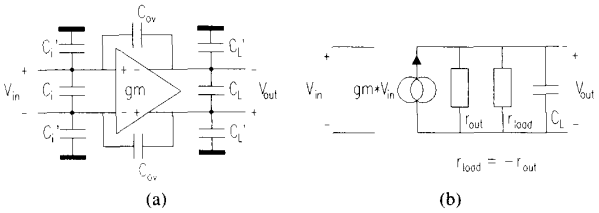


Fig. 1. (a) A transconductor without internal nodes will have no parasitic poles or zeros and will be therefore of infinite bandwidth. (b) Loading the output of an integrator with a negative load resistance makes a infinite dc gain possible, without requiring internal nodes.

theoretically infinite dc gain and infinite bandwidth. As a result, the integrator quality factor will also be infinite.

In this paper, first a tranconductor circuit with an excellent high-frequency behavior is described (Section II). Then, for demonstration, a third-order elliptic filter with a cutoff frequency tunable up to 98 MHz is described (Section III). For this transconductor a Q-tuning circuit with high-speed potential (Section IV) and a supply voltage buffer (Section V) are also presented. Finally, the experimental results of the circuits are discussed (Section VI).

II. Transconductor

In this section, first the linear V-to-I conversion of the transconductor is described and then the common-mode control, dc-gain enhancement, bandwidth, distortion, and noise are discussed.

A. V–I Conversion

The transconductor [9] is based upon the well-known CMOS inverter. This CMOS inverter has no internal nodes and has a good linearity in V–I conversion if the β factors of the n-channel and p-channel transistors are perfectly matched. Consider first the inverter of Fig. 2(a). If the drain currents of an n- and a p-channel MOS transistor in saturation are written as

$$I_{dn} = \frac{\beta_n}{2}(V_{gsn} - V_{tn})^2, \qquad \text{with } \beta_n = \frac{\mu_n C_{ox} W_n}{L_n} \tag{1a}$$

$$I_{dp} = \frac{\beta_p}{2}(V_{gsp} - V_{tp})^2, \qquad \text{with } \beta_p = \frac{\mu_p C_{ox} W_p}{L_p} \tag{1b}$$

then the output current of the single inverter can be written as

$$I_{\text{out}} = I_{dn} - I_{dp} = a(V_{\text{in}} - V_{tn})^2 + b \cdot V_{\text{in}} + c \tag{2}$$

with

$$a = \tfrac{1}{2}(\beta_n - \beta_p) \tag{2a}$$

$$b = \beta_p(V_{dd} - V_{tn} + V_{tp}) \tag{2b}$$

$$c = \tfrac{1}{2}\beta_p(V_{tn}^2 - (V_{dd} + V_{tp})^2). \tag{2c}$$

All devices are assumed to operate in strong inversion and in saturation. If $\beta_n \neq \beta_p$, i.e., $a \neq 0$, the V-to-I conversion will not be linear. The error is in fact a square-law term, that can be canceled if a balanced structure is used.

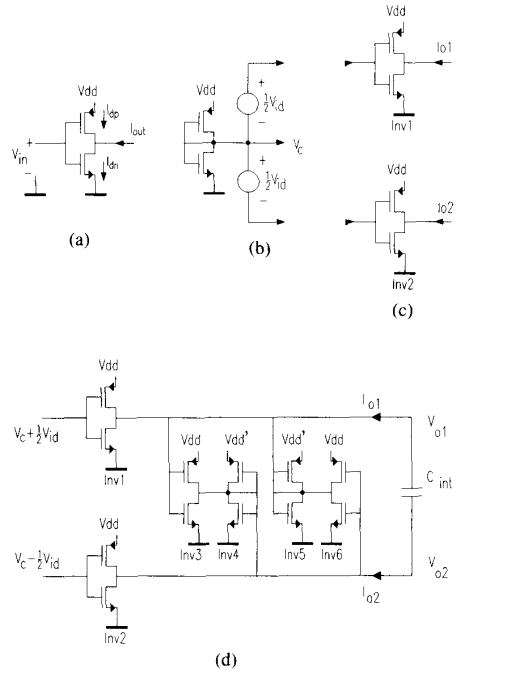


Fig. 2. (a) Single inverter. (b) Generation of the common-mode voltage level V_c. (c) Two balanced inverters performing linear V-to-I conversion if driven by the circuit of Fig. 2(b). (d) The complete transconductance element.

The output current is zero when $V_{\text{in}} = V_c$ (see Fig. 2(b)), with

$$V_c = \frac{V_{dd} - V_{tn} + V_{tp}}{1 + \sqrt{\dfrac{\beta_n}{\beta_p}}} + V_{tn}. \tag{3}$$

Note that for $\beta_p = \beta_n$ and $V_{tn} = -V_{tp}$, then $V_c = 1/2\,V_{dd}$ as can be easily verified.

Fig. 2(c) shows the balanced version of the circuit of Fig. 2(a). The two matched inverters Inv1 and Inv2 are driven by a differential input voltage V_{id}, balanced around the common-mode voltage level V_c (see (3)). The output currents I_{o1} and I_{o2} can be calculated, and subtraction results in the differential output current I_{od}:

$$I_{o1} = a(V_c - V_{tn} + \tfrac{1}{2}V_{id})^2 + b(V_c + \tfrac{1}{2}V_{id}) + c$$

$$I_{o2} = a(V_c - V_{tn} - \tfrac{1}{2}V_{id})^2 + b(V_c - \tfrac{1}{2}V_{id}) + c$$

$$I_{o1} - I_{o2} = a((V_c - V_{tn} + \tfrac{1}{2}V_{id})^2 - (V_c - V_{tn} - \tfrac{1}{2}V_{id})^2) + bV_{id}$$

or

$$I_{o1} - I_{o2} = V_{id}(b + 2a(V_c - V_{tn})) = V_{id}(\beta_p(V_{dd} - V_c + V_{tp}) + \beta_n(V_c - V_{tn})). \tag{4}$$

Hence, the differential output current is linear with the differential input voltage. Using (3) for eliminating V_c, (4) can be written as

$$I_{od} = I_{o1} - I_{o2}$$
$$= V_{id}(V_{dd} - V_{tn} + V_{tp})\sqrt{\beta_n \cdot \beta_p} = V_{id} \cdot gm_d. \quad (5)$$

Equation (5) is valid as long as the transistors operate in strong inversion and saturation. The differential transconductance (gm_d) is linear, even with nonlinear inverters, i.e., if $\beta_n \neq \beta_p$. To reduce common-mode output currents, however, β_n should be chosen close to β_p. The linearity in *V–I* conversion is obtained by explicitly making use of the square law and matching properties of the MOS transistors. Normally the transistors have no ideal square-law behavior; these effects will be treated in the section on distortion. The transconductance can be tuned by means of the supply voltage V_{dd}. For this purpose a tunable power-supply unit needs to be implemented on chip.

The schematic of the complete transconductor is given in Fig. 2(d). It consists of six CMOS inverters, which are for the moment all assumed to be equal ($V_{dd} = V'_{dd}$). The basic *V–I* conversion is performed by Inv1 and Inv2. Note that the circuit of Fig. 2(d) has indeed no internal nodes, except for, of course, the supply nodes.

B. Common-Mode Control and DC-Gain Enhancement

The common-mode level of the output voltages V_{o1} and V_{o2} is controlled by the four inverters Inv3–Inv6 of Fig. 2(d). For simplicity the transconductances gm of these inverters are assumed for the moment to be linear ($\beta_n = \beta_p$). Inv4 and Inv5 are shunted as resistances connected between the output nodes and the common-mode voltage level V_c. The values of these resistances are $1/gm_4$ and $1/gm_5$. Inv3 and Inv6 inject currents $gm_3(V_c - V_{o1})$ and $gm_6(V_c - V_{o2})$, respectively, into these resistances.

The result for common-mode output signals is that the "V_{o1}" node is virtually loaded with a resistance $1/(gm_5 + gm_6)$ and the "V_{o2}" node with a virtual resistance $1/(gm_3 + gm_4)$. For differential output signals the "V_{o1}" node is loaded with a resistance $1/(gm_5 - gm_6)$ and the "V_{o2}" node is loaded with a resistance $1/(gm_4 - gm_3)$. If the four inverters have the same supply voltage and are perfectly matched, all the gm's are equal. Thus the network Inv3–Inv6 forms a low-ohmic load for common signals and a high-ohmic load for differential signals, resulting in a controlled common-mode voltage level of the outputs. The quiescent common-mode voltage will be equal to V_c of (3). The common and differential load resistances at the nodes V_{o1} and V_{o2} are recapitulated in Table I.

If the four inverters Inv3–Inv6 are not exactly linear ($\beta_n \neq \beta_p$), but still perfectly matched, it can be shown that the load resistance is nonlinear only for common-mode signals; for differential signals all even and odd nonlinear terms are canceled [18].

The dc gain of the transconductor-C integrator can be increased by loading the differential inverters Inv1 and Inv2 with a negative resistance for differential signals as described in Section I. By choosing $gm_3 > gm_4$, $gm_5 = gm_4$, and $gm_6 = gm_3$, this negative resistance $1/\Delta gm = 1/(gm_4 - gm_3) = 1/(gm_5 - gm_6)$ is simply implemented without adding extra nodes to the circuit. The width of the transistors in Inv4 and Inv5 can be designed slightly smaller than those of Inv3 and Inv6.

TABLE I
COMMON AND DIFFERENTIAL LOAD RESISTANCES SEEN ON NODES V_{o1} AND V_{o2}, REALIZED BY THE TRANSCONDUCTANCES gm_3–gm_6 OF Inv3–Inv6

Output Node	Common Resistance	Differential Resistance
V_{o1}	$\frac{1}{gm_5 + gm_6}$	$\frac{1}{gm_5 - gm_6}$
V_{o2}	$\frac{1}{gm_4 + gm_3}$	$\frac{1}{gm_4 - gm_3}$

To obtain a more exact filter response, the dc gain of the integrators can be fine-tuned during operation (Q-tuning) with a separate supply voltage V'_{dd} for Inv4 and Inv5 as shown in Fig. 2(d). If in a filter all inverters Inv4 and Inv5 have identical V'_{dd} and the matching of all inverters is ideal, then the dc gain of every integrator can theoretically become infinite if $\Delta gm = -3/r_{oi}$, where r_{oi} is the output resistance of one inverter. However, the maximal dc gain of an integrator will be degraded by mismatch. Assume for simplicity $gm_4 = gm_5 = gm_0$ and $gm_3 = gm_6 = gm_0 - \Delta gm - \delta gm$. Here Δgm is the desired transconductance difference and equal to $-3/r_{oi}$. For simplicity reasons it is assumed that the mismatch δgm is equal for gm_3 and gm_6. The dc gain of the transconductance-C integrator for differential output signals now becomes

$$A_o = \frac{gm_d}{g_{\text{out}}} = \frac{gm_d}{\frac{3}{r_{oi}} + gm_4 - gm_3}$$
$$= \frac{gm_d}{\frac{3}{r_{oi}} + \Delta gm + \delta gm} = \frac{gm_d}{\delta gm}. \quad (6)$$

Normally $gm_d \approx gm_3 \approx gm_4$. The dc gain is therefore equal to the reciprocal value of the relative transconductance error ($\delta gm/gm$) due to mismatch. This error is a local mismatch error and can be kept small by using proper layout techniques [19]. The measured relative transconductance error over 20 chips was less than 0.5%. Consequently, the dc gain is larger than 200 (46 dB), which is high enough for many applications. In the analysis it was assumed that the mismatch δgm is equal for gm_3 and gm_6 ($gm_4 = gm_5$ and $gm_3 = gm_6$). If this is not the case, the conclusion of the calculation remains valid; however, the two outputs of the integrator will be slightly asymmetrical.

If no dc-gain enhancement was applied ($\Delta gm = \delta gm = 0$), the dc gain would have been 20 (13 dB). The con-

clusion is that by choosing gm_3 and gm_6 larger than gm_4 and gm_5, a significant improvement of the integrator dc gain is obtained, without affecting the bandwidth.

If $\delta gm < 0$ the net load resistance will become negative. A stand-alone integrator then would become unstable due to the right-half-plane pole. However, a more detailed analysis [18] and practical experiments show that a gyrator or biquad section built with these building blocks will remain stable. This is owing to the feedback loops inherent to a filter structure constructed with gyrators or biquad sections.

C. Bandwidth

The transconductor presented here has a large bandwidth because of the absence of internal nodes, as stated in Section I. In filter structures where all the parasitic capacitances are shunted parallel to the integration capacitors, the only parasitic poles are due to the finite transit time of the carriers in the MOST channel, which are, according to [10], located in the gigahertz range. It can be shown that the series resistances in capacitors even have a compensating effect on the effects of the finite transit time in the MOS channel [18].

D. Distortion

Using the ideal square-law transistor model of (1), the V-to-I conversion will be perfectly linear. However, a more detailed analysis shows that nonlinearities due to mobility reduction occur. In first-order approximation this may be modeled as

$$\mu = \frac{\mu_o}{1 + \theta|V_{gs} - V_T|}. \tag{7}$$

In order to obtain a manageable expression, simplifications have been made. Assuming $\beta_n = \beta_p = \beta$, and therefore, $V_c - V_{tn} = V_{dd} - V_c + V_{tp} = V_o$, and also assuming $(\theta V_o)^2 \ll 1$, yields

$$I_{od} \approx \frac{\beta V_o(5V_o(\theta_n + \theta_p) + 4)}{1 + 2V_o(\theta_n + \theta_p)} \frac{1}{2} V_{id} - \frac{\beta(8V_o\theta_n\theta_p + \theta_n + \theta_p)}{1 + 4V_o(\theta_n + \theta_p)} \frac{1}{8} V_{id}^3. \tag{8}$$

This expression can again be simplified if $\theta V_o \ll 1$:

$$I_{od} \approx 2\beta V_o V_{id} - \frac{\beta}{8}(\theta_n + \theta_p) V_{id}^3. \tag{9}$$

The mobility reduction of both the n- and p-channel devices therefore causes mainly third-order distortion. The second-order distortion due to $\beta_n \neq \beta_p$ combined with mismatch between Inv1 and Inv2 is negligibly small in practice. Normally, channel-length modulation is also a source of distortion in circuits with "square-law linearization" [11]. Owing to the compensation of the output resistances in the tranconductor (the dc-gain enhancement), channel-length modulation is no source of distortion in this circuit.

E. Noise

The thermal drain current noise of a single transistor can be written as

$$\bar{i}_{dt}^2 = 4 \cdot k \cdot T \cdot c \cdot gm \cdot \Delta f, \qquad \text{with} \quad 1 < c < 2. \tag{10}$$

The differential output noise of the transconductor of Fig. 2(d) can now be written as

$$\bar{i}_{od}^2 = 4kTc\,\Delta f \sum gm_i \tag{11}$$

where $\Sigma\, gm_i$ is the sum of all transconductances of the six inverters and $c = c_n = c_p$ is the thermal noise coefficient of the n- and p-channel transistors $1 < c < 2$.

Note that the transconductor of Fig. 2(d) has a class-AB behavior; the supply currents will therefore also be dependent of the input signal. This makes an on-chip (low ohmic) power-supply tuning circuit more complex. In Section V of this paper a method for implementing an integrated supply voltage regulation is described.

Summarizing, we can say that we have a linear transconductor without internal nodes and with a tunable output resistance. The dc gain is only limited by mismatch: the measured transconductance mismatch of less than 0.5% gives a dc gain of at least 200, which is high enough for many filters. The parasitic poles are located in the gigahertz range and are due to the finite transit times in the MOS channels. The transconductance can be tuned by means of the supply voltage V_{dd} and the output resistance can be fine-tuned with a separate supply voltage V'_{dd}. Tuning the transconductance results in tuning of the cutoff frequency of a filter and tuning of the output resistance results in tuning of the integrator phase and thus of the quality factors of a filter built with this transconductor.

III. Filter

A third-order elliptic filter [12], [13] has been realized with the transconductance of Fig. 2(d). The filter is derived from a passive ladder filter since ladder filters have good sensitivity and dynamic range properties. The normalized passive prototype filter [14] is given in Fig. 3. The pole quality factor is equal to 3. The active implementation is shown in Fig. 4(a). The filter is a direct implementation of the ladder filter using a gyrator ($G3$–$G6$) loaded with a capacitor (C_2, C_2') to simulate the inductor. The resistors are also implemented with transconductance elements ($G2$ and $G7$).

The W/L ratios of the n-channel devices in the transconductors are 24 μm/3 μm for Inv1, Inv2, Inv3, and Inv6 and 21 μm/3 μm for Inv4 and Inv5. The widths of the p-channel devices are in all cases a factor of 3 ($\approx \mu_n/\mu_P$) larger. The threshold voltages are $V_{tn} = 0.75$ V and $V_{tp} = -0.80$ V.

To achieve a high cutoff frequency, the filter operates mainly on parasitic capacitances. This is possible since the parasitic capacitances are all at nodes where a capacitance is desired in the filter. The parasitic capacitances consist for roughly 70% of gate oxide capacitance C_{ox} and

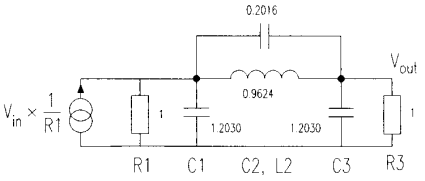


Fig. 3. Passive prototype filter [14].

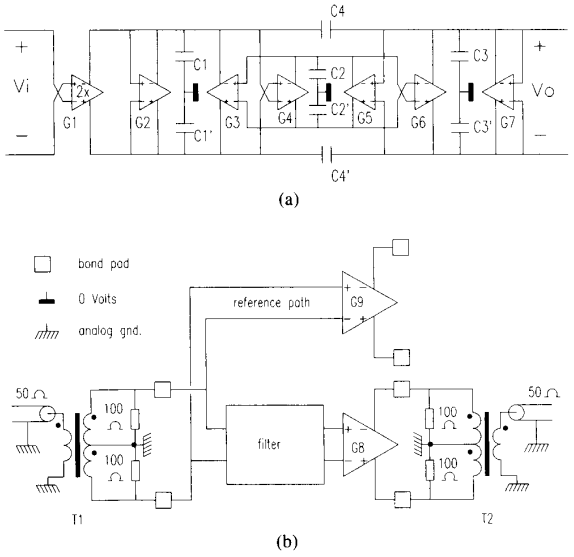


Fig. 4. (a) Active implementation of the filter of Fig. 3. (b) Test circuit that makes compensation for the parasitic elements outside the filter possible during measurements.

are consequently quite linear. C_1 and $C_{1'}$ are fully determined by parasitic capacitances. The other capacitances, C_2–C_4 are designed by adding small extra capacitors. These extra capacitors are polysilicon n-well capacitors with gate oxide dielectricum. The time constants of the filter can be written as $\tau = C/gm_d$, with C a capacitance in Fig. 4(a) and gm_d the transconductance of the transconductor. Both C and gm_d are approximately proportional to C_{ox}. The result of this is that the spread in τ due to spread in C_{ox} is small. This results in quite accurate time constants even if the filter operates mainly on its own parasitic capacitances.

No tuning circuitry has been integrated for this test chip. The tuning of both cutoff frequency (with V_{dd}) and quality factors (with V'_{dd}) is done manually with external voltage sources.

A. Experimental Setup

Measurement of the filter characteristic up to very high frequencies requires special precautions in the design of the filter IC. This is illustrated in the experimental setup of Fig. 4(b). The balanced input voltage of the filter is generated from a single-ended signal by means of an off-chip transformer ($T1$). The output voltages of the filter are converted to output currents by means of $G8$. These currents are converted to voltages by means of two off-chip 100-Ω resistors. The differential output voltage is converted to a single-ended voltage in 50 Ω by means of a transformer ($T2$). An on-chip reference path, also buffered with a matched transconductor ($G9$), is used to compensate for all parasitic elements, apart from mismatch, outside the filter during measurements. With this technique, accurate measurements up to several hundreds of megahertz can be done.

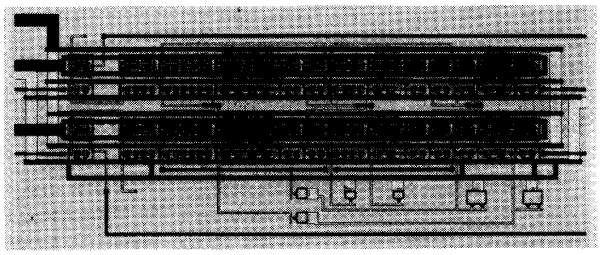


Fig. 5. Chip photograph. Area of the filter is 0.63 mm^2.

V_{dd} and V'_{dd} are applied externally. An off-chip capacitor of 4.7 μF has been connected between the V_{dd} and V'_{dd} pins and ground.

The chip was processed in a 3-μm CMOS process. A chip photograph is given in Fig. 5. The area of the filter is 0.63 mm^2. The experimental results obtained from this test chip are discussed in Section VI.

IV. Tuning

To correct the frequency response of an integrated filter for process and temperature variations, tuning of the cutoff frequency [15] (f-tuning) is generally applied. Several filters are also provided with automatic tuning of the quality factors (Q-tuning) [16]. Combined f- and Q-tuning can be applied with either a master voltage-controlled filter (VCF) [5], [16] or a master voltage-controlled oscillator (VCO) [6].

In Fig. 6 the method using a master VCO is illustrated. The VCO consists of two undamped integrators and has a controllable frequency and quality factor. Consider first the Q-tuning loop. If the Q of the VCO is infinite, then the VCO will oscillate harmonically with a constant amplitude (the poles are exactly on the $j\omega$ axis of the complex plane). The Q-loop controls the amplitude of the VCO in such a way that it will oscillate with a constant amplitude. By copying the voltage, used for tuning the Q of the two integrators in the master VCO, to the (matched) integrators in the slave filter, the quality factors of the filter will also be correct. The amplitude of the VCO signal is uncritical as long as the integrators in the VCO operate in their linear region.

The f-control loop is a well-known phase-locked loop (PLL) which locks the oscillating frequency to an external reference frequency. The voltage used for tuning the frequency of the VCO is copied to the slave filter.

The combination of f- and Q-tuning is possible if the f- and Q-control loops are independent. This is difficult in

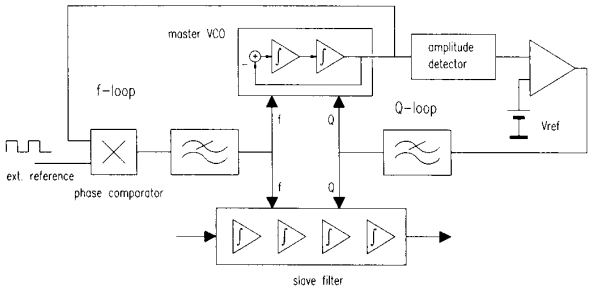


Fig. 6. Combined frequency- and Q-tuning loops.

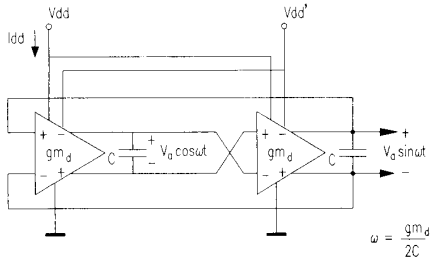


Fig. 7. Voltage-controlled oscillator for the frequency- and Q-tuning circuit.

practice. If the Q-tuning loop is much faster than the f-tuning loop, the f-tuning loop will be quasi-static and then the f- and Q-loops become practically independent. For VHF filters the Q loop must be fast enough to tune the VCO, which oscillates at least at the cutoff frequency of the filter, which can be up to 100 MHz. The Q-tuning loop must therefore be very fast.

This paper describes a Q-tuning technique without a physical loop, so that it is very fast and therefore suitable for very high frequencies [17].

A. Automatic Q-Tuning

With the transconductor described in Section II, the master VCO of Fig. 7 can be made. If the Q of the VCO is infinite, it will oscillate harmonically at a frequency determined by V_{dd}.

For every value of V_{dd} there is only one value of V'_{dd} resulting in correct Q. The inverse is also true: for each V'_{dd} there is only one value of V_{dd} so that the Q is correct. It follows that the frequency can as well be tuned with V'_{dd} if the Q loop controls V_{dd}. V_{dd} and V'_{dd} will then be related correctly. This is very important for the Q-tuning circuit described here.

Consider the VCO is oscillating harmonically with an amplitude V_a at a frequency ω. Using (1) and (3), the supply current I_{dd} is calculated (see Fig. 7). This results in

$$I_{dd} = 2\beta_p\left(2\left(\frac{\sqrt{\beta_n/\beta_p}}{1+\sqrt{\beta_n/\beta_p}}(V_{dd} - V_{tn} + V_{tp})\right)^2 + \frac{1}{4}V_a^2(\sin^2\omega t + \cos^2\omega t)\right) \quad (12)$$

and since $\sin^2 \omega t + \cos^2 \omega t = 1$, this can be written as

$$I_{dd} = 2\beta_p\left(2\left(\frac{\sqrt{\beta_n/\beta_p}}{1+\sqrt{\beta_n/\beta_p}}(V_{dd} - V_{tn} + V_{tp})\right)^2 + \frac{1}{4}V_a^2\right). \quad (13)$$

If $V_a = 0$, therefore no oscillation, then I_{dd} consists of the quiescent current of eight inverters, biased in their linear region. In the case of oscillation, $V_a \neq 0$, the current is larger but remains constant. Note that the current I_{dd} is dependent on the amplitude of the VCO output signal (V_a).

The transconductor therefore has an intrinsic wide-band amplitude detection function hidden in its supply current. This can be exploited as follows. If the node V_{dd} is supplied by means of a dc current source with a value given by (13) instead of by a voltage source with value V_{dd}, the oscillator will oscillate with a constant and well-controlled amplitude V_a. The controlling mechanism can be explained as follows.

1) Suppose the poles of the VCO are in the right complex half plane. Therefore, the amplitude V_a tends to increase. With a constant I_{dd} this implies from (13) that V_{dd} must decrease. With a (quasi-static) constant V'_{dd} this implies that gm_3 and gm_6 (Fig. 2(d)) decrease while gm_4 and gm_5 remain constant so that the oscillation is damped until the poles are forced on the imaginary axis. Hence, this ensures a feedback control for the amplitude.

2) Suppose the poles of the VCO are in the left complex half plane. The amplitude V_a tends to decrease. With a constant I_{dd} this implies that V_{dd} must increase. With a (quasi-static) constant V'_{dd} this implies that gm_3 and gm_6 increase while gm_4 and gm_5 remain constant, so that the oscillation is undamped until the poles are forced on the imaginary axis. This leads to the same conclusion about a feedback control for the amplitude.

The result of this mechanism is that, for a given V'_{dd}, V_{dd} is controlled in such a way that the poles of the VCO will always be on the imaginary axis; the Q factor of the VCO is then infinite.

If the resulting voltage V_{dd} of the master VCO is copied to the filter by means of a buffer, the quality factors of the slave filter will automatically be correct. It is concluded that the whole Q-tuning circuit can consist of only one dc current source with a current as specified by (13).

The problem now is how to realize the current source I_{dd} with the value given by (13). This can be done as follows.

Usually $V_{dd} \approx V'_{dd}$; with this in mind the current I_{dd} can be made from V'_{dd}, which in turn is determined by the frequency control loop. This is shown in Fig. 8. The current I_o is determined by V'_{dd}, V_b, and the inverter parameters.[2] The inverter in Fig. 8 is matched to those connected to V_{dd} in the VCO, all n-channel transistors have

[2]The sources V_b can be made on chip by driving a current through a resistorlike circuit.

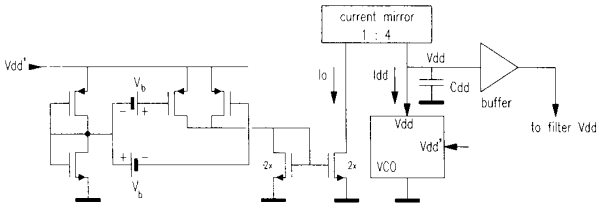


Fig. 8. Circuit that generates I_{dd} from V'_{dd} and V_b such that the amplitude of the VCO is constant and the Q is correct.

equal geometries, and all p-channel transistors have equal geometries. The current I_o can be calculated, which results in

$$I_o = \frac{1}{2}\beta_p\left(2\left(\frac{\sqrt{\beta_n/\beta_p}}{1+\sqrt{\beta_n/\beta_p}}(V'_{dd} - V_{tn} + V_{tp})\right)^2 + 2V_b^2\right). \tag{14}$$

Comparing (13) and (14) it can be seen that for

$$V_b = \tfrac{1}{4}\sqrt{2}\,V_a \tag{15}$$

the current I_o has only to be multiplied with a factor of 4 to obtain the current given by (13), as long as $V_{dd} \approx V'_{dd}$. This multiplication is simply performed with a 1:4 current mirror. The voltage buffer copies the voltage V_{dd} to the slave filter.

If V_{dd} deviates somewhat from V'_{dd} or if there is little mismatch in the circuit of Fig. 8, then only the amplitude of the oscillation will be different from the value predicted by (15). The quality factor, however, will remain correct. Normally the transistors deviate from ideal square-law behavior. This results in a current I_{dd} of the VCO which is not exactly constant. I_{dd} will contain higher harmonics of the oscillation frequency ω.

The capacitance C_{dd}, however, will drain these currents, so that the ripple in V_{dd} remains very small. The capacitance C_{dd} is the n-well-to-substrate capacitance of the p-channel transistors, which will be on chip. If necessary the buffer can in addition be preceded by a simple low-pass filter.

Note that temperature effects are compensated if the circuit of Fig. 8, the VCO, and the slave filter all have the same temperature.

This Q-tuning circuit needs no fast amplitude detectors or rectifiers, owing to the intrinsic wide-band amplitude detection provided by the transconductance element of Fig. 2(d) (see also (12)). The circuit of Fig. 8 has no signal-carrying nodes. All nodes have a (quasi-static) dc voltage during operation. For this reason the oscillating frequency of the VCO is not a limiting factor and the circuit is suitable for very high frequencies. Furthermore, the circuit is extremely simple; it only consists of one current source, two current mirrors, and a buffer. The circuit of Fig. 8 and the VCO have been realized on a breadboard. The experimental results are discussed in Section VI.

V. Supply Voltage Buffer

The cutoff frequency and quality factors of a filter built with the transconductor of Fig. 2(d) are tuned with the two supply voltages V_{dd} and V'_{dd}. These two supply voltages are generated by the f- and Q-tuning loops, and need to be buffered before being applied to the filter. This section deals with the design of these supply voltage buffers.

Consider a filter built with the transconductors of Fig. 2(d). These transconductors in turn consist of three inverter pairs, all driven balanced around the common-mode voltage level V_c of (3). The inverter pairs can be either connected to the supply voltages V_{dd} or V'_{dd}. In Fig. 9 the inverter pairs connected to V_{dd} are shown schematically (ignore for the moment the dashed current sources). The supply voltage V_{dd} of the inverter pairs is applied by an on-chip supply voltage buffer, modeled with a voltage source $V_{dd,\text{ideal}}$ with series impedance Z_{dd}.

In order to obtain insight into the supply current I_{dd}, a simplification can be made by considering first only one inverter pair connected to V_{dd}. The inverter pair is driven with an input voltage V_{id} balanced around the common-mode level V_c as shown in Fig. 9. Using (1) and (3), and assuming all transistors operating in strong inversion and saturation, the supply current $I_{dd,2\text{inv}}$ of the two inverters can be calculated:

$$I_{dd,2\text{inv}} = \underbrace{\beta_p\left(\frac{\sqrt{\beta_n/\beta_p}}{1+\sqrt{\beta_n/\beta_p}}(V_{dd} - V_{tn} + V_{tp})\right)^2}_{\text{I}} + \underbrace{\frac{1}{4}\beta_p V_{id}^2}_{\text{II}}. \tag{16}$$

This supply current consists of a quiescent part (part I of (16)) and a signal-dependent part (part II of (16)). The sum of these signal-dependent supply currents (I_{dd}) of all inverter pairs connected to V_{dd} will cause a ripple in V_{dd} in the configuration of Fig. 9 if Z_{dd} is not low enough.

Since this occurs both for V_{dd} and V'_{dd}, the effect on complete filters will be modulation of both cutoff frequency and quality factors if the supply voltages are applied by buffers with a too high series impedance. The consequence will be distortion in the filter transfer and crosstalk causing deterioration of the stopband attenuation.

For low-frequency variations in I_{dd}, the source $V_{dd,\text{ideal}}$ with series impedance Z_{dd} can operate satisfactorily since Z_{dd} can be made low for these frequencies by using well-known feedback techniques. However, these feedback techniques are not sufficient to make Z_{dd} low for high-frequency variations in I_{dd}. For correct high-frequency operation additional current sources (Fig. 9, dashed lines) are added to the inverter pairs. The purpose of $I_{cc,2\text{inv}}$, for example, is to inject the required supply current for high-

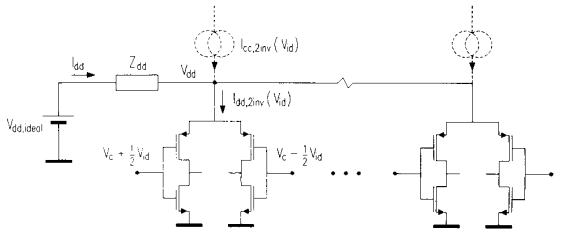


Fig. 9. A filter is built with inverter pairs which need to be supplied by a supply voltage buffer. The series impedance Z_{dd} of this buffer can be made low for low-frequency variations in I_{dd} by using feedback techniques. The high-frequency variations in the supply currents of the inverter pairs are compensated by additional (dashed) current sources. Therefore no high-frequency current flows through Z_{dd} resulting in a well-controlled V_{dd}, even for high frequencies.

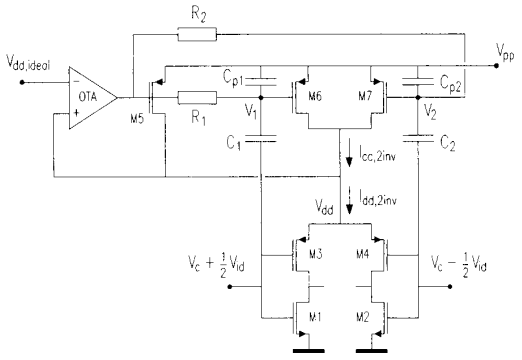


Fig. 10. Implementation of the supply current compensation technique with p-channel transistors.

frequency variations in $I_{dd,2inv}$. Since all inverter pairs are provided with such a compensation current source, this implies that no high-frequency current will flow through Z_{dd} and the requirements for Z_{dd} are relaxed for these frequencies. The result is a well-controlled V_{dd}, even for high-frequencies.

The basic idea is therefore the use of feedback for low frequencies and compensation for high-frequency variations in supply currents.

The compensation sources have to be implemented for each inverter pair in the filter. Since many inverter pairs will have the same input voltages and thus the same supply currents, a combination of compensation sources is possible for these inverter pairs.

In the rest of this section two possible implementations of the supply voltage buffers with high-frequency supply current compensation are given. For simplicity only circuitry for supplying one inverter pair connected to V_{dd} is discussed. Therefore, the feedback mechanism and only one compensation current source will be described.

A. Version I

Consider first the configuration of Fig. 10. $M1 = M2$ and $M3 = M4$ is the inverter pair that requires supply current compensation.

Neglecting for low frequencies all capacitors in Fig. 10, the OTA drives the gates of $M5$, and via $R1$ and $R2$ the gates of identical transistors $M6$ and $M7$. The result is a low-ohmic supply voltage buffer for low frequencies. At high frequencies the capacitive load of the OTA causes a degradation in the OTA voltage gain and thus $|Z_{dd}|$ increases.

For high frequencies the current $I_{cc,2inv}$, the sum of the drain currents of $M6$ and $M7$, compensates $I_{dd,2inv}$, the sum of the drain currents[3] of $M3$ and $M4$. The compensation mechanism works as follows. The gate voltages V_1 and V_2 of $M6$ and $M7$, respectively, can be written as

$$V_1 = V_{cc} + \tfrac{1}{2} V_{cd} \tag{17a}$$

$$V_2 = V_{cc} - \tfrac{1}{2} V_{cd} \tag{17b}$$

where V_{cc} is the common-mode voltage and V_{cd} is the differential-mode voltage of V_1 and V_2. Using (17) and (1) $I_{cc,2inv}$ can be expressed as

$$I_{cc,2inv} = \underbrace{\beta_{p6,7}(V_{pp} - V_{cc} + V_{tp})^2}_{\text{I}} + \underbrace{\tfrac{1}{4}\beta_{p6,7} V_{cd}^2}_{\text{II}} \tag{18}$$

where $\beta_{p6,7}$ is the β factor of $M6$ and $M7$ and V_{pp} is the "outside world" supply voltage. Comparison with (16) shows that the high-frequency ripple in $I_{dd,2inv}$ is compensated if for these frequencies part II of (18) is equal to part II of (16). The differential input signal of the two inverters needs therefore to be transferred to the gates of $M6$ and $M7$. This is done by the capacitive voltage dividers C_1, C_{p1} and C_2, C_{p2}. C_{p1} and C_{p2} are the equal parasitic (gate-source) capacitances of $M6$ and $M7$. $C_1 = C_2$ are added floating capacitors. The transfer from V_{id} to V_{cd} is

$$V_{cd} = V_{id} \frac{C_1}{C_1 + C_{p1}}, \qquad \text{for } \omega \gg 1/R_1 C_{p1}. \tag{19}$$

$R_1 = R_2$ serve only for dc biasing the gates of $M6$ and $M7$ (resulting in correct V_{cc}) and are assumed to be large.

Note that the transfer of the capacitive voltage divider of (19) is frequency independent. The conversion from V_{id} of V_{cd} is of very large bandwidth. Capacitor series resistances, etc. can cause deviations from the transfer of (19) only in the gigahertz range.

The capacitors C_1 and C_2 in series with C_{p1} and C_{p2} form an extra capacitive load for the filter. The filter capacitors will need to be corrected for this.

The required voltage drop across the supply voltage buffer, that is the minimal value of $V_{pp} - V_{dd}$, is equal to $|V_{gs} - V_{tp}|$ of $M5$, $M6$, and $M7$. This value depends on the W/L ratio of these transistors. A typical value of $|V_{gs} - V_{tp}|$ ranges from 200 to 500 mV.

[3]Actually $I_{dd,2inv}$ is the sum of the source currents of $M3$ and $M4$. The capacitive gate and bulk currents do not contribute to $I_{dd,2inv}$ if the inverter inputs are driven balanced and the capacitances are assumed to be linear. The sum of the source currents is therefore equal to the sum of the drain currents of $M3$ and $M4$.

If the matching is perfect the ripple in $I_{dd,2inv}$ is fully compensated for the frequency range of interest. Limitations in frequency are due to capacitor nonidealities. Mismatch will cause an error in $I_{cc,2inv}$ resulting in a nonzero ripple in V_{dd}. At the end of this section simulation results are given for the case of 10% mismatch in $I_{cc,2inv}$.

In the description of the circuit of Fig. 10 it was assumed that the "outside-world" supply voltage V_{pp} is constant. This can be realized by applying a large off-chip capacitor across V_{pp}. If V_{pp} cannot be made constant, a ripple in V_{pp} is transferred to the nodes V_1 and V_2 via C_{p1} and C_{p2}. This causes an extra undesired ripple in $I_{cc,2inv}$ and thus a ripple in V_{dd} at high frequencies.

B. Version II

To circumvent this poor power supply rejection at high frequencies, an alternative solution is given in Fig. 11. The principle is the same as in Fig. 10, however, n-channel transistors instead of p-channel transistors are used for the supply voltage buffer.

The operation of the low-frequency feedback mechanism is obvious. The high-frequency compensation is similar to that of Fig. 10. First, consider that V_{dd} is constant (later it will appear that V_{dd} will be constant indeed). C_{p1} and C_{p2} are the parasitic gate-source capacitors of $M6$ and $M7$. The gate voltages of $M6$ and $M7$, V_1 and V_2, respectively, can again be written in the form of (17). V_{id} is converted to V_{cd}, by means of capacitive voltage division, as described by (19). The result is an $I_{cc,2inv}$, now generated by the n-channel transistors $M6$ and $M7$, of the form:

$$I_{cc,2inv} = \underbrace{\beta_{n6,7}(V_{cc} - V_{cd} - V_{tn})^2}_{\text{I}} + \underbrace{\tfrac{1}{4}\beta_{n6,7}V_{cd}^2}_{\text{II}}. \quad (20)$$

Compensation of the high-frequency part of $I_{dd,2inv}$ is possible if part II of (20) is equal to part II of (16).

The advantage of the n-channel compensation is that there is no significant capacitance present between the V_{pp}-node and the signal path, resulting in an improved power supply rejection. A serious disadvantage is a larger voltage drop across the supply voltage buffer. Simulation results of the circuit under 10% mismatch in $I_{cc,2inv}$ are given below.

C. Simulations

The performance of the circuits of Figs. 10 and 11 has been evaluated with SPICE (level 3) simulations.

Consider first the circuit of Fig. 10. The transistor dimensions of the two inverters are the same as Inv1 and Inv2 of the transconductors used in the filter, as described in Section III. $M5 = M6 = M7 = 2 \times M3$, $G_{OTA} = 80$ μA/V, and $R_{OTA} = 5$ MΩ. The voltages V_{pp} and V_{dd} are chosen as 5 V and 3 V, respectively. The input voltage V_{id} is a sine wave with an amplitude of 0.5 V with variable frequency. Note that the frequency of the ripple in $I_{dd,2inv}$ will be twice the frequency of V_{id}.

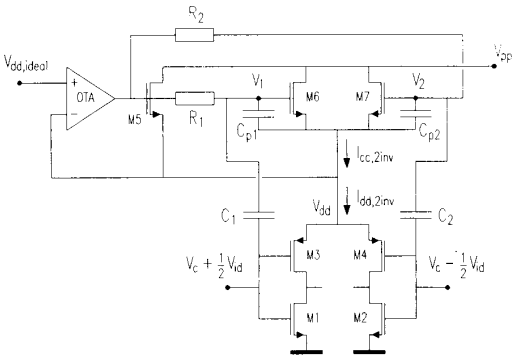


Fig. 11. Implementation of the supply current compensation technique with n-channel transistors.

To investigate the ripple in V_{dd} due to variations of V_{id}, transient simulations were carried out. For comparison, first the case of a simple feedback supply voltage buffer is analyzed by setting $R_1 = R_2 = 0$ and $C_1 = C_2 = 0$. The result can be found in curve a of Fig. 12. For low frequencies the ripple is small due to sufficient loop gain in the feedback loop. For very high frequencies the ripple is also small thanks to the capacitance present at the V_{dd} node. For the intermediate frequencies the ripple becomes much larger.

Using the supply current compensation ($C_1 = C_2 = 610$ fF and R_1 and R_2 of the same order of magnitude as R_{OTA})[4] makes zero ripple in V_{dd} possible for the case of perfect matching. Since this is not realistic in practice, an artificial error of 10% is introduced in the simulations. The result is plotted in curve b of Fig. 12. The improvement with respect to curve a is obvious. The ripple in V_{dd} is several millivolts, which is small enough [18].

Consider now the circuit of Fig. 11. $M5 = M6 = M7 = 2 \times M1$ and the rest the parameters are equal to those mentioned above.

The case of only feedback ($R_1 = R_2 = C_1 = C_2 = 0$) is plotted in curve c of Fig. 12 and a similar behavior as in curve a is found. Using the supply current compensation ($C_1 = C_2 = 200$ fF) with an artificial mismatch of 10% in $I_{cc,2inv}$ gives curve d and thus a significant improvement.

The difference in performance of the circuits of Figs. 10 and 11 becomes clear when considering the crosstalk from the "outside-world" supply voltage V_{pp} to the internally generated V_{dd}. For the circuit of Fig. 10 the transfer of variations in V_{pp}-to-V_{dd} variations has a high-pass character. For frequencies below 200 kHz the gain is -44 dB. For frequencies beyond 20 MHz the capacitances C_{p1} and C_{p2} have enabled crosstalk and the gain becomes -0.5 dB. For these frequencies[5] the power supply rejection is poor and a large off-chip capacitor across V_{pp} will be nec-

[4]Such a large resistor can be made actively, with a unity feedback differential pair in weak inversion.

[5]Note that a 20-MHz ripple in V_{pp} corresponds to a 10-MHz sine wave at the inputs of the inverter pairs.

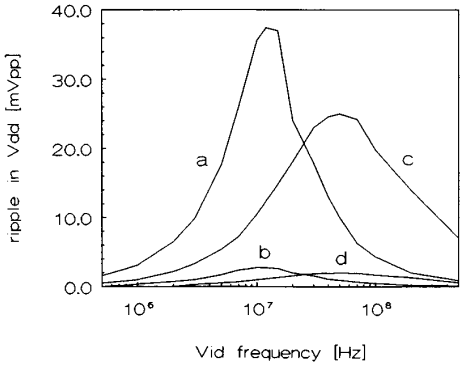


Fig. 12. Simulated ripples in V_{dd}(mV$_{peak\text{-}peak}$) versus frequency of input signal V_{id} for: (*a*) the circuit of Fig. 10 with feedback only ($C_1 = C_2 = R_1 = R_2 = 0$); (*b*) the circuit of Fig. 10 also with compensation, however, with 10% mismatch in $I_{cc,2inv}$; (*c*) same as curve (*a*) but now for the circuit of Fig. 11; (*d*) same as curve (*b*) but now for the circuit of Fig. 11.

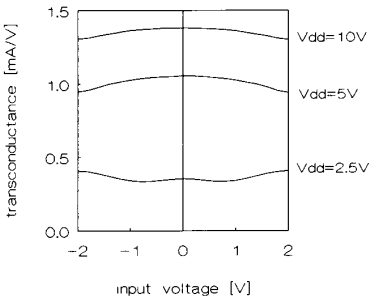


Fig. 13. Measured transconductance versus differential input voltage (V_{id}) for three values of V_{dd}.

essary. The circuit of Fig. 11 has a similar behavior, however simulations show that the transfer from V_{pp} to V_{dd} is 30 dB lower for all frequencies compared to the circuit of Fig. 10. The circuit of Fig. 11 therefore has a much better (30 dB) power-supply rejection.

VI. Experimental Results

In this section the experimental results of the transconductor, filter, and Q-tuning circuit are discussed.

A. Transconductor

The transconductor of Fig. 2(d) has been realized on chip. The measured transconductance for different supply voltages is given in Fig. 13. The nonlinearities are mainly of the third order and due to mobility reduction as expected from (8). For V_{dd} = 10 V, 1% relative error in transconductance[6] occurs at a differential input voltage (V_{id}) of 1 V. If V_{dd} = 2.5 V, it can be seen that not all transistors operate in strong inversion for differential input voltages larger than 1 V.

B. Filter

The measured filter responses are given in Fig. 14 for three values of V_{dd}: V_{dd} = 2.5, 5, and 10 V. In Fig. 14(a) the corresponding responses of the ideal passive prototype of Fig. 3 (same cutoff frequency) are plotted as well. The cutoff frequency is varied from 22 MHz (V_{dd} = 2.5 V) to 98 MHz (V_{dd} = 10 V). From Fig. 14(a) a close matching with the ideal response is seen. The notch at 214 MHz is 60 dB deep and is very well positioned. Fig. 14(b) is a passband detail of Fig. 14(a). However, from this figure it can be seen that the dc filter gain is too high and the ripple in the passband is too large compared to the ideal response of the passive prototype filter, especially at higher values of V_{dd}. The reason appeared to be a layout error in the filter chip. In fact, the inverters Inv1 and Inv2 of $G2$ and $G7$ of Fig. 4(a) have a supply voltage V'_{dd} instead of V_{dd}. The result of this is that, especially for higher supply voltages, the transconductances of $G2$ and $G7$ become somewhat lower than their nominal values. In Fig. 14(c) the measured filter response is compared to that of the passive prototype filter with R_1 and R_3 (see Fig. 3) chosen slightly too large, corresponding to the situation caused by the layout error. From this figure it can be seen that the curves now do match very closely. Fig. 14(d) shows a passband detail of Fig. 14(c). The dc filter gain and the passband ripple of the measured responses and the responses of the passive prototype now are almost equal.

Taking the layout error into account, we may conclude that the filter response is very close to the response of the passive prototype filter. The 98-MHz filter curve matches well to that of the prototype filter up to 350 MHz. This implies that the integrator has indeed a sufficiently high dc gain and only parasitic poles far enough in the gigahertz region. The total intermodulation distortion (TIMD) of the filter for the three values of V_{dd} is plotted in Fig. 15. The TIMD was measured with a two-tone input signal with frequencies around half of the cutoff frequency of the filter.

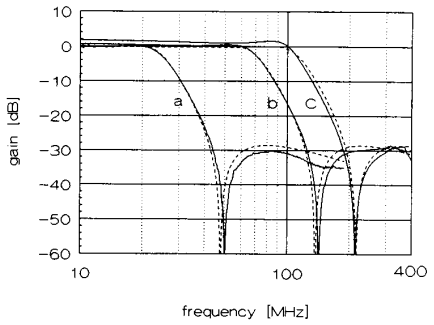
The other experimental results are summarized in Table II. The lower limit for the dynamic range was chosen as the total passband noise and the upper limit was the 1% TIMD input rms voltage level. As can be seen from Table II the filter has a high dynamic range: 72 dB for V_{dd} = 10 V.

C. Q-Tuning

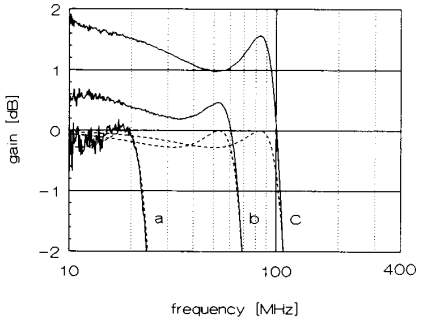
The circuit of Fig. 8 and the VCO have been realized on breadboard, using commercially available CA3600 CMOS arrays. The voltage V_b was chosen as 0.5 V. Using (15), the amplitude V_a of the VCO is expected to be $0.5 \cdot 2\sqrt{2} = 1.4$ V.

The VCO oscillates at frequencies up to 7 MHz. The results are plotted in Fig. 16. The voltage V_{dd} varies with V'_{dd} in such a way that the VCO oscillates with a constant amplitude of almost 1.4 V, as expected. The frequency varies almost linearly with V_{dd} as predicted by (5).

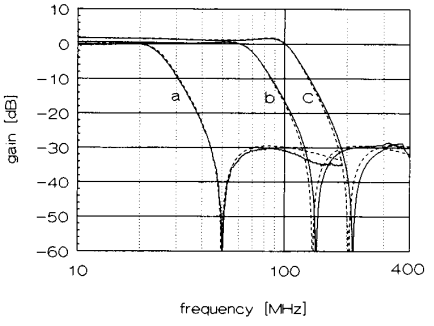
[6]A 1% relative transconductance error corresponds to 0.083% THD, assuming only third-order distortion.



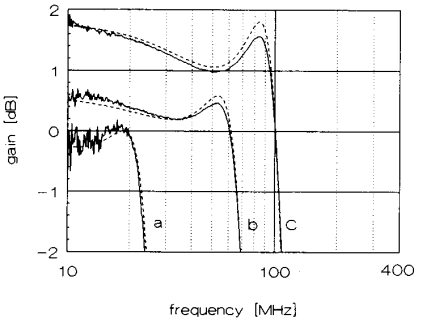
(a)



(b)



(c)



(d)

Fig. 14. (a) Measured filter response (——) and ideal response of the passive prototype filter (– – –): (*a*) V_{dd} = 2.5 V, (*b*) V_{dd} = 5 V, (*c*) V_{dd} = 10 V. (b) Passband detail of Fig. 14(a). (c) Measured filter response (——) and ideal response of the passive prototype filter corrected for the layout error (– – –): (*a*) V_{dd} = 2.5 V, (*b*) V_{dd} = 5 V, (*c*) V_{dd} = 10 V. (d) Passband detail of Fig. 14(c).

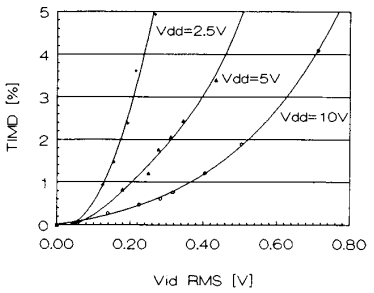


Fig. 15. Total intermodulation distortion of the filter versus rms input voltage ($f \approx \frac{1}{2} f_{cutoff}$).

TABLE II
EXPERIMENTAL RESULTS OBTAINED FROM THE FILTER TEST CHIP

Parameter	V_{dd} = 2.5 V	V_{dd} = 5 V	V_{dd} = 10 V
Cutoff frequency	22 MHz	63 MHz	98 MHz
Total passband input noise	?	81 μV_{rms}	96 μV_{rms}
Dynamic range*	?	68 dB	72 dB
CMRR passband	40 dB	40 dB	40 dB
Transconductance	0.35 mA/V	1.06 mA/V	1.38 mA/V
Power dissipation	4 mW	77 mW	670 mW
V'_{dd}	2.50 V	4.76 V	8.10 V

*See text.

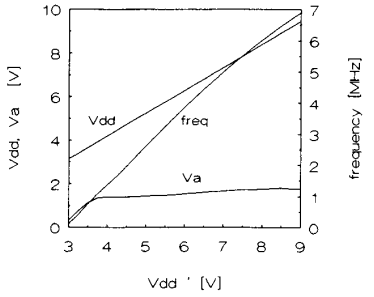


Fig. 16. Experimental results of Q-tuning circuit obtained from a breadboard realization: V_a (amplitude), V_{dd}, and frequency of the VCO versus V'_{dd}. The voltage V_b was chosen to be 0.5 V.

Simulations indicate that an on-chip realization of the circuit will be able to operate at very high frequencies (over 100 MHz). The tuning circuit is not connected to the filter because of the poor matching between breadboard components and on-chip components.

VII. CONCLUSIONS

In this paper principles and circuits for integrated filters at very high frequencies in full CMOS technology have been described.

The CMOS transconductor circuit presented has a bandwidth in the gigahertz region thanks to the absence of internal nodes. Owing to the used square-law linearization technique, the linearity is good and the transconductance can be tuned by means of the supply voltage V_{dd}. The parasitic output resistance of all the MOS transistors

is compensated and the resulting net output resistance can be fine-tuned by means of a separate supply voltage V'_{dd}. Thus, Q-tuning becomes possible.

A 100-MHz CMOS continuous-time low-pass filter realized in a 3-μm process has been presented. The filter is constructed with transconductance elements and capacitors. The measured filter frequency response is close to the theoretical response for frequencies up to 350 MHz. The notch in the response is 60 dB deep and well positioned. The filter operates mainly on parasitic capacitances while the accuracy is not affected and the dynamic range is high (72 dB). The cutoff frequency and the Q factors can be tuned by means of two supply voltages.

A special Q-tuning technique for very-high-frequency filters, based on a VCO, has been presented. The Q-tuning circuit is very simple (it is, in fact, only a special dc current source) and contains no signal-carrying nodes. Therefore, no bandwidth limitations are imposed by the Q-tuning circuit, resulting in a well-controlled Q for very high frequencies. Experimental results of a breadboard realization of the Q-tuning circuit were presented, giving results that are in accordance with the theory.

A technique for making an on-chip low-ohmic supply voltage buffer for controlling V_{dd} and V'_{dd} of the transconductors has been presented. The basic idea is the use of feedback for low frequencies and compensation for high-frequency variations in supply currents. The very large bandwidth (in theory infinite) of a capacitive voltage divider is exploited for implementing ultrafast supply current compensation. Two circuit realizations have been presented and are illustrated with simulation results.

It is expected that lower supply voltages and even higher frequencies are achievable if a more advanced (smaller channel lengths) CMOS process is used. The results obtained with these transconductor, filter, and Q-tuning techniques demonstrate that accurate integrated CMOS filters at very high frequencies are possible. Applications can be found in the field of TV IF filtering [18] and other VHF filters.

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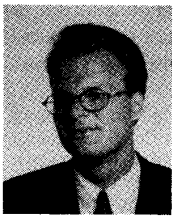

Bram Nauta was born in Hengelo (Ov.), The Netherlands, on January 20, 1964. He received the M.S. degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands, in 1987 on the subject of BiMOS OTA design. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very-high frequencies.

In 1990 he co-founded Chiptronix consultancy and gave several courses on analog CMOS circuit design in the industry. He is now with Philips Research Laboratories, Eindhoven, The Netherlands. His main interests are in the field of analog integrated circuits.