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A CMOS VGA With DC Offset Cancellation for Direct-Conversion Receivers

Yuanjin Zheng, *Member, IEEE*, Jiangnan Yan, and Yong Ping Xu, *Senior Member, IEEE*

***Abstract*—A CMOS dB-linear variable gain amplifier (VGA) with a novel I/Q tuning loop for dc-offset cancellation is presented. The CMOS dB-linear VGA provides a variable gain of 60 dB while maintaining its 3-dB bandwidth greater than 2.5 MHz. A novel exponential circuit is proposed to obtain the dB-linear gain control characteristics. Nonideal effects on dB linearity are analyzed and the methods for improvement are suggested. A varying-bandwidth LPF is employed to achieve fast settling. The chip is fabricated in a 0.35-μm CMOS technology and the measurement results demonstrate the good dB linearity of the proposed VGA and show that the tuning loop can effectively remove dc offset and suppress I/Q mismatch effects simultaneously.**

***Index Terms*—dB-linear variable-gain amplifier (VGA), dc offset, direct-conversion receiver, I/Q tuning, pre-distortion compensation.**

I. Introduction

DIRECT-CONVERSION receivers (DCRs) have become very attractive because of their low power consumption, small die size, and low cost. The simplicity of direct conversion, however, comes with a number of design issues, namely, dc offset, I/Q mismatch, even-order distortion, flicker noise, and LO leakage [1]. Among them dc offset may be the most critical problem which is introduced by self-mixing in the mixer. DC offset may substantially degrade the bit error rate (BER) performance and saturate the following stages.

In DCR architecture, the variable gain amplifier (VGA) is an important block in the baseband circuit. The main function of the VGA is to provide a fixed voltage output for different input signal levels, and thus the dynamic range of the overall system is greatly improved. It has been widely used in wireless RF transceivers such as Bluetooth, wireless local area networks (WLANs), GSM WCDMA, ultra-wideband (UWB), and magnetic disk-drive read channel applications [2], [3], [5], [15], [19]. The VGA should meet requirements of large dynamic range and good dB linearity. For DCR applications, it should also be able to efficiently suppress the dc offset. In CMOS technology, basically there are three methods to control the gain of a VGA, namely, by varying: 1) the transconductance of a MOS device operated in the saturation region [2]; 2) the load resistance [3]; and 3) the source degeneration resistance which is often implemented by a MOS device operated in the linear region [4]. Among them, the last method has the advantages of good linearity, low noise figure, and low power dissipation because the source degeneration does not impose any penalty on voltage headroom. Thus, in this paper, the differential amplifier with source degeneration is chosen to implement three linear VGA stages.

DB linearity, which is an exponential gain control characteristic, may be required to achieve a quick settling time in the automatic gain control (AGC) loop and a large dynamic control range [5]. However, in CMOS technology, it is difficult to realize the exponential or logarithmic function because of its inherent square-law or linear characteristics. Therefore, some approximation methods are needed. Some of the reported CMOS dB-linear VGAs are based on a pseudo-exponential function [6], [26]. Alternatively, the Taylor's series can be utilized to approximate the exponential function [7]. The approximation error of Taylor's series can be less than 5% for a relative large input range [8]. Therefore, this method is chosen to implement the proposed novel pseudo-exponential voltage generator.

Due to he large dynamic range of the VGA, dc offset may be amplified to a large value and saturate the following amplifier. Thus, dc-offset cancellation is indispensable in DCR baseband circuit design. One approach to remove the offset is to employ ac coupling, i.e., high-pass filtering, in the downconverted signal path. However, since the desired signal spectrum extends to dc, the signal may be corrupted if the low corner frequency of the high-pass filter (HPF) is too high. Also, a low corner frequency in the HPF may also lead to temporary loss of data [1]. Digital signal processing (DSP) is also an effective approach to compensate for dc offset, as reported in [9]–[11] and [27]. However, these approaches necessitate digital-to-analog conversion and consume a considerable amount of power. Several other dc-offset cancellation techniques have been reported in [12] and [13], but these solutions require off-chip components such as large blocking capacitors.

A novel dc-offset cancellation technique is thus proposed in this paper. The proposed tuning loop is able to cancel dc offset and suppress I/Q mismatch simultaneously. This tuning loop eliminates the need for DAC or any external components, thus low power consumption can be achieved.

This paper is organized as follows. Section II describes the system configuration and the gain distribution. A dB-linear VGA is presented in Section III, which is composed of a linear VGA and a novel pseudo-exponential voltage circuit. Pre-distortion techniques are employed to attain good linearity. A novel I/Q tuning loop for dc-offset cancellation is proposed in

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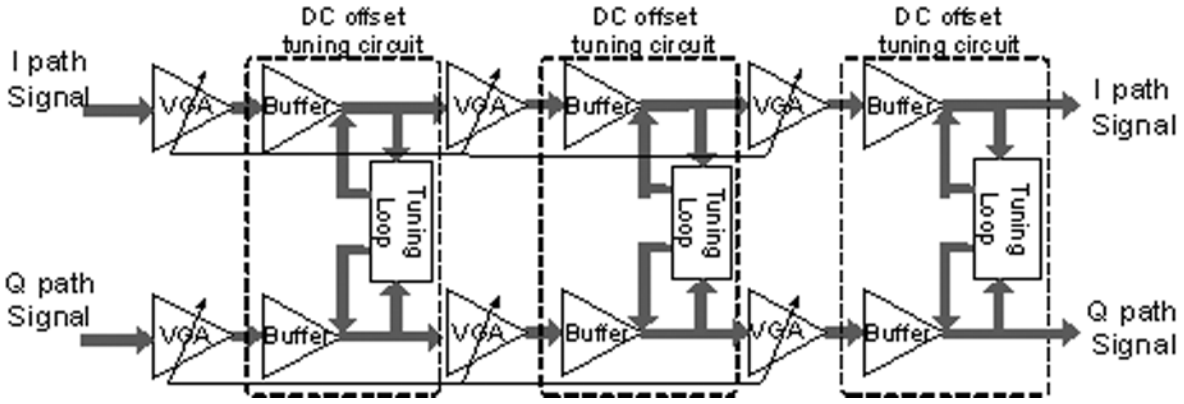

Fig. 1. System diagram of VGA circuits and dc-offset cancellation loop.

Section IV. DC offset detection issues are investigated and solutions are proposed. The performance of the tuning is analyzed in Section V. Simulation and measurement results are presented in Section VI. We present a conclusion in Section VII.

II. System Configuration

Generally, the microvolt input signal from the antenna needs to be amplified around 100 dB to a level that can be digitized by an analog-to-digital converter (ADC) with reasonable resolution. Of this gain, typically 25–30 dB is realized by the combination of LNA and mixer. The LPF may also provide a gain of about 10 dB if needed. Thus, the VGA may need to provide the remaining maximum gain of 60 dB. On the other hand, the typical value of the dc offset produced at the output of the mixer is on the order of 10 mV. Thus, if directly amplified by such a high gain (60 dB) provided by the VGA, the offset voltage will saturate the following circuits and hence prohibit the amplification of the desired signal [1]. In addition, to prevent the dc offset from corrupting the demodulation of the desired signal, it is desirable to constrain the dc offset at the output of the VGA within a limited range, say, less than 10 mV.

The architecture of the VGA circuit is depicted in Fig. 1. In each branch, three stages of the proposed VGA are cascaded to provide a total variable gain of 60 dB. A unity gain buffer is employed after each VGA stage. The buffer is part of the dc-offset tuning loop. Thus, signal amplification and dc-offset cancellation are separated. In each stage, one tuning loop is used for both I and Qbranches. The tuning loop is essentially a feedback structure. The detection and tuning of the dc offset take place at the same node, and the tuning is performed in the current domain. With such a tuning scheme, it is possible to achieve quick settling.

III. dB-Linear VGA

The specifications for the VGA proposed in this paper are listed in Table I. With some minor modifications, this proposed VGA can also be used for different wireless communication applications, such as DCS, WLAN, and WCDMA. In this paper, a CMOS dB-linear VGA that meets these specifications is described. A novel exponential circuit is proposed to obtain the dB-linear control characteristics. The nonideal effects on dB linearity are analyzed and the remedies are proposed.

TABLE I
Specifications of the Proposed VGA

Input Level (dBV)		Output Level (dBV)	
High Gain Mode	Low Gain Mode	High Gain Mode	Low Gain Mode
-63	-3	-3	-3
Other Figures			
-3 dB Bandwidth (MHz)	IIP3 (dBm)	IIP2 (dBm)	DC offset rejection (dB)
2.5	10	40	50

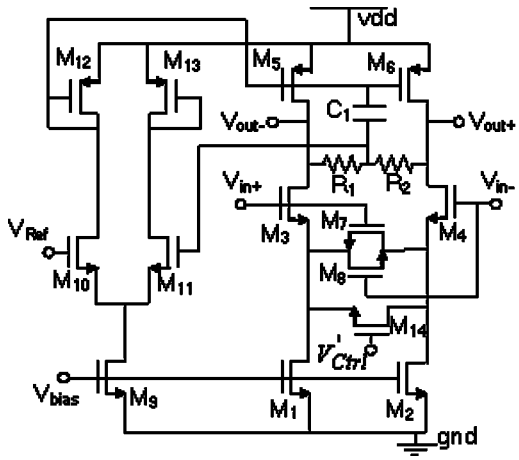

Fig. 2. Linear VGA.

A. Differential Linear VGA

One stage of the differential linear VGA is shown in Fig. 2. M_3 and M_4 form the linear transconductance pair. M_5 and M_6 act as the active load to provide high gain. M_7 and M_8 are used to improve the linearity [4]. The common-mode feedback circuit consists of R_1, R_2, and $M_{10} - M_{13}$. The gain of the VGA can be adjusted continuously over a large range (~ 20 dB) through the source degeneration transistor M_{14}. The gain of the VGA can be expressed as

$$A_v = -G_s R_d \frac{g_m}{g_m + G_s} \tag{1}$$

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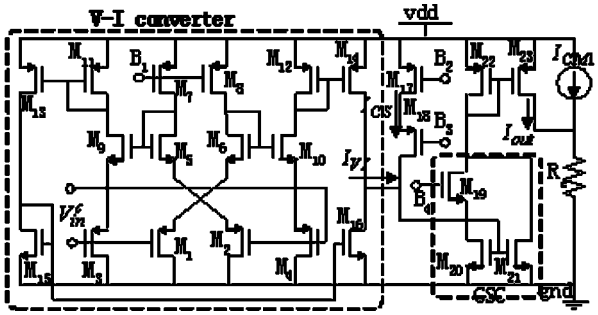

Fig. 3. Exponential control circuit (B1–B4 denote four different dc bias voltages).

where g_m, G_s, and R_d represent the transconductance of the input transistor M_3 and M_4, the conductance of source degeneration transistor M_{14}, and the load resistance of M_5 and M_6, respectively, and

$$G_s = \mu_n C_{\rm ox}\left(\frac{W}{L}\right)(V_{\rm gs} - V_{\rm th}). \tag{2}$$

Obviously, if $g_m \gg G_s$ and $g_m/(g_m+G_s)(g_m+G_s) \approx 1$, A_v can be rewritten as

$$A_v \approx -\mu_n C_{\rm ox}\left(\frac{W}{L}\right)_{14}(V_{\rm gs14} - V_{\rm th})\,R_d. \tag{3}$$

Therefore, the gain of the VGA can be linearly controlled by the gate voltage of M_{14}.

B. Exponential Function Generation Circuit

The Taylor's series expansion of a general exponential function can be expressed as

$$e^{(b/a)x} = 1 + \frac{b}{a}x + \frac{1}{2!}\left(\frac{b}{a}x\right)^2 + \frac{1}{3!}\left(\frac{b}{a}x\right)^3 + \cdots \frac{1}{n!}\left(\frac{b}{a}x\right)^n + \cdots \tag{4}$$

where a and b are two constants. If $|bx/a| \ll 1$, the higher order terms are negligible, and (4) becomes

$$2a^2 e^{(b/a)x} \approx a^2 + (a+bx)^2. \tag{5}$$

A large range of x in (3) can be attained if the constant a and b are carefully chosen to ensure $-0.575 < bx/a < 0.815$ with allowance for up to 5% approximation error. Based on (5), a wide-range exponential voltage generation circuit is proposed and shown in Fig. 3. It includes three building blocks, namely, a linear V–I converter, a constant current source and a current square circuit (CSC), where the V–I converter and CSC are realized with similar circuits as in [14] and [15], respectively. Assuming the an input current of $I_{\rm in}$, the output current of the CSC can be written as

$$I_{\rm out} = 2I_0 + \frac{I_{\rm in}^2}{8I_0}. \tag{6}$$

The output current of the V–I converter can be expressed as $I_{VI} = 2g_b V_{\rm in}^c$, where g_b is the equivalent transconductance of the V–I converter [14]. By adding a constant current $I_{\rm CS} = 4I_0$ to I_{VI} and assuming that the input current of CSC to be $I_{\rm in} = I_{VI} + I_{CS}$, as shown in Fig. 3, the output current of CSC can be rewritten as

$$\begin{aligned} I_{\rm out} &= 2I_0 + \frac{(I_{VI} + I_{\rm CS})^2}{8I_0} \\ &= \frac{1}{8I_0}\left[(4I_0)^2 + (4I_0 + 2g_b V_{\rm in}^c)^2\right]. \end{aligned} \tag{7}$$

By properly sizing the transistors, the condition of $-0.575 < 2g_b V_{\rm in}^c/4I_0 < 0.815$ can be ensured for the entire operation range of $V_{\rm in}^c$. Using this condition and (5), (7) can be rewritten as

$$I_{\rm out} \approx \frac{1}{8I_0} 2\,(4I_0)^2 \exp\left(\frac{2g_b}{4I_0}V_{\rm in}^c\right) = 4I_0 \exp\left(\frac{g_b}{2I_0}V_{\rm in}^c\right). \tag{8}$$

Thus, an approximately exponential current is realized. Furthermore, the exponential control voltage $V_{\rm Ctrl}$ can be easily generated by passing the CSC output current through a resistor R_e, i.e.,

$$V_{ctrl} = R_e I_{\rm out} = 4R_e I_0 \exp\left(\frac{g_b}{2I_0}V_{\rm in}^c\right). \tag{9}$$

This voltage is used to control the gain of the linear VGA in Fig. 2, and hence a dB-linear VGA is realized.

C. dB Linearity Compensation

Ideally, a linear VGA whose gain is controlled by an exponential function voltage would exhibit good dB linearity. However, in practice, it is affected by two factors: 1) the nonzero source and the threshold voltage of the degeneration transistor M_{14} and 2) the increase of G_s with $V_{\rm in}^c$.

First, considering the effect of gate–source voltage and the threshold voltage of M_{14}, we can rewrite (3) as

$$\begin{aligned} A_v &= -\mu_n C_{ox}\left(\frac{W}{L}\right)(V_g - V_s - V_{\rm th})\,R_d \\ &= -K\,(V_{\rm Ctrl} - V_{\rm st})\,R_d \end{aligned} \tag{10}$$

where $V_{\rm st} = V_s + V_{\rm th}$ and $K = \mu n C_{\rm ox}(W/L)$. Substituting (9) into (10) and taking the logarithm of both sides yields

$$\begin{aligned} 20\log|A_v| = {} & 20\log KR_d \\ & +20\log\left[4R_e I_0 \exp\left(\frac{g_b V_{\rm in}^c}{2I_0}\right) - V_{\rm st}\right]. \end{aligned} \tag{11}$$

Since $V_{\rm st}$ is nonzero, the gain of the VGA will not be dB-linearly proportional to $V_{\rm in}^c$. To compensate for this nonlinearity, a fixed current $I_{\rm CM1} = V_{\rm st}V_{\rm st}R_eR_e$ is added to $I_{\rm out}$, and the control voltage becomes

$$V'_{\rm Ctrl} = (I_{\rm out} + I_{\rm CM1})\,R_e = V_{\rm Ctrl} + V_{\rm st}. \tag{12}$$

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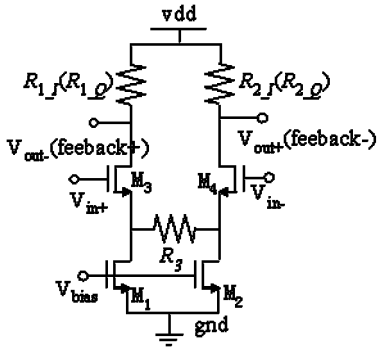

Fig. 4. Schematic of the buffer.

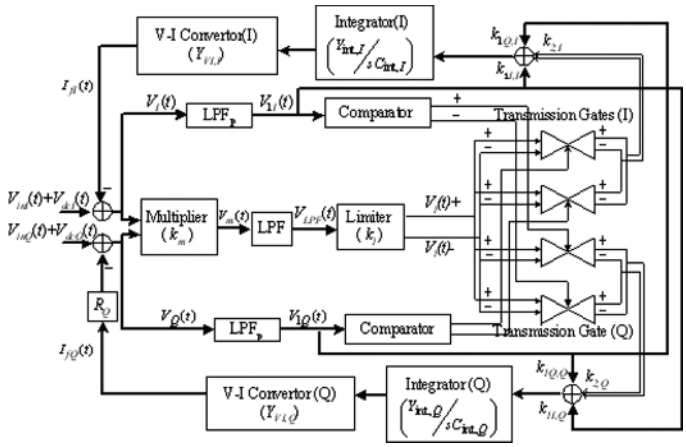

Fig. 5. Diagram of the tuning loop.

Substituting it into (10) and taking the logarithm of both sides yields

$$20\log|A_v| = 20\log KR_d + 20\log\left[4R_eI_0\exp\left(\frac{g_bV_{\rm in}^c}{2I_0}\right)\right] = 20\log\left(4KR_eR_dI_0\right) + \frac{10g_b}{I_0}V_{\rm in}^c. \quad (13)$$

The effect of V_{st} is removed.

Second, the gain linearity of the VGA is also affected by the dependence of G_s on $V_{\rm in}^c$. Substituting (2) and (9) into (1) and assuming that the nonlinearity caused by V_{st} has been removed yields

$$A_v = -R_dg_m\frac{4KR_eI_0\exp\left(\frac{g_bV_{\rm in}^c}{2I_0}\right)}{g_m + 4KR_eI_0\exp\left(\frac{g_bV_{\rm in}^c}{2I_0}\right)}. \quad (14)$$

When taking the logarithm of both sides, (14) becomes

$$20\log|A_v| = 20\log 4I_0KR_eR_dg_m + 10\frac{g_bV_{\rm in}^c}{I_0} - 20\log\left\{g_m + K\left[4I_0\exp\left(\frac{g_bV_{\rm in}^c}{2I_0}\right)\right]\right\}. \quad (15)$$

Similar to (11), the third term in (15) deteriorates the dB linearity. This effect becomes more severe when the input control voltage $V_{\rm in}^c$ is high. To compensate for this effect, the rate of the gain variation with respect to the control voltage $V_{\rm ctrl}$ when $V_{\rm in}^c$ is high may be purposely made faster than that defined by the exponential function. This is essentially a pre-distortion technique that, to some extent, compensates for the nonlinearity introduced by the third term in (15). One of the possible implementations of this pre-distortion is to make $I_{\rm CS} \gg 4I_0$. It can be proved that, with such an implementation, the output voltage of the exponential circuit $V_{\rm ctrl}$ increases with a faster rate than the ideal exponential case when $V_{\rm in}^c$ is high.

IV. DC Offset Tuning System

The dc-offset tuning system consists of a buffer and tuning loop (Fig. 1). This section will address the sensing of dc offset, which is performed by the tuning loop. DC offset is subtracted through the buffer in the current domain. Schematic of the buffer is shown in Fig. 4. It is a linearized transconductance providing unity gain. R_3 is used to improve linearity. R_1 and R_2 are the loads of the buffer where the dc offset is cancelled by the tuning current.

A. Tuning Loop Configuration

The proposed dc-offset tuning loop is shown in Fig. 5. It is based on a feedback structure that is similar to the phase-locked loop (PLL). A multiplier is used to sense the dc offset embedded in the incoming signals in the I and Q path. A low-pass filter (LPF) is employed to suppress the residual ac signals at multiplier output and leaves mainly the dc offset. Thus, a detected signal including dc offset, the multiplied components, and attenuated I and Q signal, is obtained. This detected signal is then fed to the respective integrator in the I and Q path. The integrator removes the ac components in the detected signal and accumulates the dc component to provide a voltage for dc-offset tuning. The tuning voltage is converted to a tuning current I_f by a V–I converter. By applying the converted current to the output resistor of the buffer, a feedback voltage is generated and then subtracted from the dc offset. A polarity detection branch, including another LPF and a comparator, is employed in each path, to determine the sign of the dc offset so as to switch to a correct branch which guarantees a negative feedback loop.

Let us assume that the dc offset of I and Q paths are $V_{\rm dcI}$ and $V_{\rm dcQ}$, and the input signal of I and Q path are $V_{\rm inI}$ and $V_{\rm inQ}$, respectively. After the multiplier, V_m is

$$\begin{aligned} V_m &= k_m \times (V_{\rm dcI} + V_{\rm inI}) \times (V_{\rm dcQ} + V_{\rm inQ}) \\ &= k_m \times [V_{\rm dcI} \times V_{\rm dcQ} + (V_{\rm inI} \times V_{\rm dcQ} \\ &\qquad + V_{\rm inQ} \times V_{\rm dcI} + V_{\rm inI} \times V_{\rm inQ})] \\ &= U + W \end{aligned} \quad (16)$$

where k_m denotes the scaling factor coefficient of the multiplier and

$$U = k_m \times V_{\rm dcI} \times V_{\rm dcQ} \quad (17)$$

$$W = k_m \times (V_{inI} \times V_{\rm dcQ} + V_{\rm inQ} \times V_{\rm dcI} + V_{\rm inI} \times V_{\rm inQ}). \quad (18)$$

Typically, U is a dc signal and W is an ac signal. The high-frequency components of W will be suppressed by the LPF.

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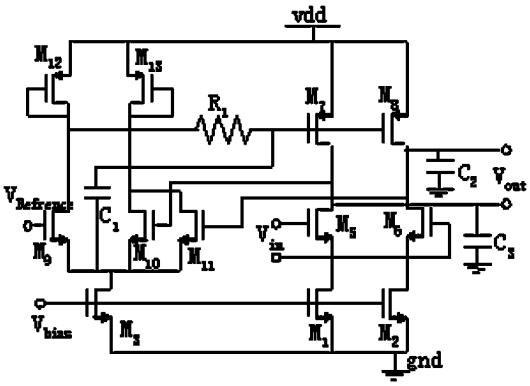

Fig. 6. Schematic of the LPF.

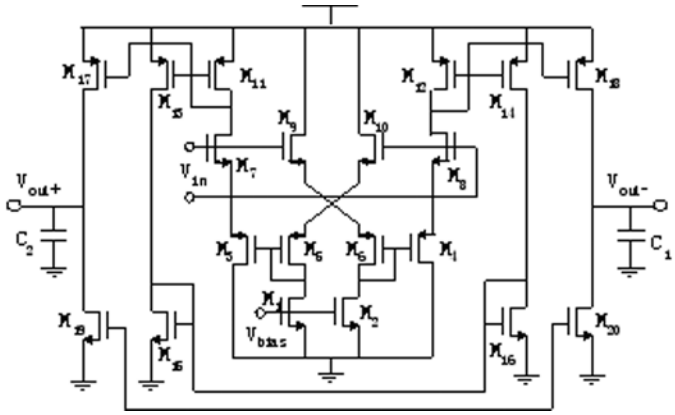

Fig. 7. Schematic of the integrator.

Thus, after LPF, only some low-frequency components of W and U remain. The low frequency of W will be further removed by the integrator. After the integration, the signal V_m becomes

$$V_s = \int V_m dt = \int U dt + \int W dt. \tag{19}$$

In most of the applications, the I and Q path signals are independent and have zero mean. If the tuning time is sufficiently long, we have

$$\int V_{\rm inI} dt = 0 \tag{20}$$

$$\int V_{\rm inQ} dt = 0 \tag{21}$$

$$\int (V_{\rm inI} \times V_{\rm inQ}) dt = 0. \tag{22}$$

From (20)–(22), the output of the integrator becomes

$$V_s = k_m \int (V_{\rm dcI} \times V_{\rm dcQ}) dt \tag{23}$$

which is proportional to the dc-offset energy, and can be used to tune the dc offset. Moreover, since the residue of low-frequency components of W can be further removed by the integrator, the requirements of the LPF are greatly relaxed.

B. Circuit Implementation

The dc-offset tuning loop can be fully integrated without any external components. In the proposed implementation, the multiplier is designed based on the one in [16]. The active $g_m - C$ LPF is shown in Fig. 6. M_5 and M_6 form the linear transconductor with common mode feedback circuit consisting of $M_9 - M_{13}$. M_7 and M_8 are the active loads with an equivalent resistance R_L, which can be expressed as $1/\lambda I_b$. Here, λ is the channel-length modulation coefficient and I_b is the bias current of the LPF. Therefore, with an on-chip capacitor I_b, the cutoff frequency of the $g_m - C$ LPF is

$$\omega_{\rm LPF} = \frac{\lambda I_b}{C_L}. \tag{24}$$

Our design shows that a low cutoff frequency of 10 kHz can be realized with an on-chip capacitance of 3 pF. The designed differential $g_m - C$ integrator is shown in Fig. 7. Transistors $M_1 - M_{20}$ work as a linear V–I converter [10] and, together with an on-chip capacitor $C_{\rm int}$, a $g_m - C$ integrator is realized.

TABLE II
POLARITY DECISION FOR TUNING DIRECTION

P(V_{dcI})	P(V_{dcQ})	P(U)	PI	PQ
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	1	1

C. DC-Offset Detection Issue

The proposed dc-offset detection scheme using a multiplier and an LPF has some merits, but potential problems may occur due to the hazards of positive feedback and insufficient phase margin.

First, positive feedback may occur due to the unrecognizable polarity of the dc offset. To ensure negative feedback of the tuning loop, the following conditions should be satisfied:

$$V_{\rm dcI} \times I_{fI} < 0 \tag{25}$$

$$V_{\rm dcQ} \times I_{fQ} < 0. \tag{26}$$

Since the source of the feedback signal U is the product of $V_{\rm dcI}$ and $V_{\rm dcQ}$, in some cases, (25) and (26) may not be satisfied. For example, when both $V_{\rm dcI}$ and $V_{\rm dcQ}$ change their polarity concurrently, U keeps its polarity unchanged. In this case, $V_{\rm dcI} \times I_{fI} > 0$ and positive feedback occurs. Hence, polarity detection branches are needed to maintain a negative feedback loop.

The interaction among the polarity-related quantities is investigated in Table II. Here, the $P(\cdot)$ equal to 1 or 0 denotes positive or negative polarity, respectively. PI (PQ) can be equal to 1 or 0 indicating whether the tuning voltage of the $I(Q)$ path should be subtracted from or added to the signal, respectively so as to guarantee the negative feedback. From Table II, it can be derived that PI should follow the sign of $P(V_{\rm dcQ})$, that is, $\rm PI = P(V_{dcQ})$, and similarly, $\rm PQ = P(V_{dcI})$, which suggest a cross connection scheme, shown in Fig. 5, the control signal of the transmission gate in the I (Q) path comes from the output of comparator in the Q (I) path.

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Based on the derivation above, the polarity decision branch is implemented by another LPF (LPF_P), a comparator, and transmission gates. The LPF_P is used to obtain the desired dc component V_{1I} and V_{1Q}, so that the comparator can decide the polarity of the dc offset. Control signals of the transmission gates are cross connected and the results are shown in Table II.

Second, insufficient phase margin may occur and cause instability. As mentioned above, U becomes an extremely large value as dc offset increases. This may raise such a high open-loop gain, and insufficient phase margin may occur. To ensure the loop stability, a limiter is employed after the multiplier. The output of the limiter is constrained within a moderate range, and so is the loop gain. As long as the loop works properly in its most hostile situation (the highest open-loop gain mode), the loop stability can be ensured.

D. I/Q Mismatch Issues

I/Q mismatch will affect the tuning result. For example, the integrator input U may become zero when either V_{dcI} or V_{dcQ} is first tuned to zero due to the mismatch. In this case, tuning of the remaining path ceases because of the zero input to the integrator.

The modified scheme is to add another two signals to the input of integrator, which are the dc offset of the I and Q paths taken from the polarity decision branches, or V_{1I} and V_{1Q}, respectively. Thus, the integrator has three input signals

$$V_{\mathrm{int}} = k_2 \times V_{\mathrm{dcI}} \times V_{\mathrm{dcQ}} + k_{1I} \times V_{1I} + k_{1Q} \times V_{1Q} \quad (27)$$

where the first term is the output from the multiplier, and the second and third terms are the dc offsets from the I and Q paths, respectively. k_2, k_{1I}, and k_{1Q} are the scaling factors in the respective paths. k_2 is chosen to be much larger than k_{1I} and k_{1Q} so that the newly introduced terms $k_{1I} \times V_{1I}$ and $k_{1Q} \times V_{1Q}$ will not affect the stability and the negative feedback of the tuning loop. V_{1I} and V_{1Q} taken from the polarity decision branch need not be critical dc voltages because the ac components will be further removed by the integrator. In the modified scheme, V_{int} will become zero if and only if both V_{dcI} and V_{dcQ} are zero. If V_{sum} does become zero, subsequently, the tuning loop will be locked. Therefore, by (27), the tuning loop can cancel dc offsets and suppress the effects of I/Q mismatch simultaneously.

E. Adaptive Bandwidth Varying

Loop settling time is an important parameter in integrated circuit design. The settling time of the tuning loop is closely related to ω_{LPF}, which is the -3 dB bandwidth of the LPF. The larger the ω_{LPF}, the quicker the settling rate [17]. However, in the dc-offset tuning loop for DCR architecture, ω_{LPF} cannot be made too large. This is because the closed-loop frequency response has a high-pass characteristic, and an excessively large ω_{LPF} will lead to the corruption of the desired signal. Therefore, there is a tradeoff between settling time and the integrity of the desired signal when choosing ω_{LPF}.

To overcome this problem, a varying ω_{LPF} is employed. Since the VGA in a DCR needs some time to adjust its gain to an appropriate level. During this period, the performance of signal demodulation will be degraded. Hence, large ω_{LPF} can be used to accelerate the dc-offset tuning initially. With dc offset being suppressed, ω_{LPF} is decreased gradually. When the gain of VGA has settled to a desired value, ω_{LPF} shrinks accordingly to a size that is small enough so that it removes dc offset without affecting the desired signal much. Since the LPF is an active filter, its cutoff frequency can be varied by the bias current which changes the value of the active resistance. The bandwidth-varying circuit is shown in Fig. 8, when a step signal $V_c u(t)$ is applied at the input, assuming that the initial value of V_p is 0 (i.e., S1 is closed during initial state), $V_p(t)$ can be expressed as

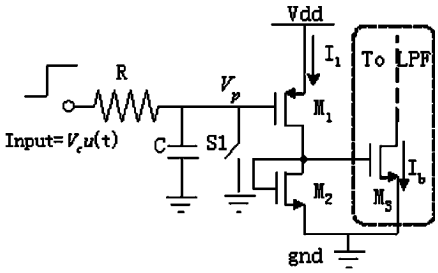

Fig. 8. Implementation of bandwidth-varying circuit.

$$V_p(t) = V_c(1 - e^{-t/RC}). \quad (28)$$

Accordingly, the drain current of M_1 is

$$\begin{aligned} I_1 &= \frac{1}{2}\mu_n C_{\mathrm{ox}} \left(\frac{W}{L}\right) (Vdd - V_p - |V_{\mathrm{thp}}|)^2 \\ &= \eta (Vdd - V_p - |V_{\mathrm{thp}}|)^2 \end{aligned} \quad (29)$$

where $\eta = 1/2\mu_n C_{\mathrm{ox}}(W/L)$. I_1 is mirrored to serve as the bias current of LPF, $I_b = k_b I_1$, where k_b denotes the gain of the current mirror. In practice, V_c can be switched in when the receiver is powered on. If V_c is set equal to Vdd, according to (28) and (29), ω_{LPF} can be expressed in terms of R and C as

$$\begin{aligned} \omega_{\mathrm{LPF}}(t) &= \frac{\lambda k_b \eta (Vdd - V_p - |V_{\mathrm{thp}}|)^2}{C_L} \\ &= \frac{\lambda k_b \eta}{C_L} (Vdd \cdot e^{-t/RC} + |V_{\mathrm{thp}}|)^2. \end{aligned} \quad (30)$$

By choosing the appropriate value of R and C, the ω_{LPF} will decrease exponentially with time from its initial value, towards an ω_{LPF} value which can be decided by the static frequency response of the dc-offset tuning loop. Thus, the setting time is improved during start-up and dc offset can be removed efficiently when the tuning loop locks. A more detailed analysis shows that the initial bandwidth of the LPF is determined by the transistor size, mirror ratio, load capacitance, and *RC* time constant according to (30). However, as $t \to \infty$, the steady-state bandwidth is not affected by the *RC* time constant. Thus, the *RC* time constant chosen should be small so that the initial bandwidth is large enough (possible suggestion is ~ 10 times the steady bandwidth) for fast tuning, while the I_b can be chosen so that the steady bandwidth is inversely proportional to the tuning convergence time of the dc-offset tuning loop.

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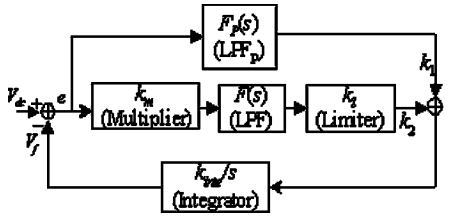

Fig. 9. Linearized model of dc-offset tuning loop.

V. Performance Analysis of the Tuning Loop

Large-signal dynamic behavior of the proposed tuning system can be modeled as a set of differential equations. Refer to Appendix A for details. Unfortunately, it is difficult to obtain analytical solutions for them. In Section VI-A, a numerical solution is provided that verifies the convergence of the proposed system in large-signal behavior.

On the other hand, although both I and Q feedback tuning for dc-offset cancellation is adopted in the proposed system, only one loop (I or Q) is used for small-signal steady-state performance analysis since the other loop has the same behavior. The linearized feedback tuning system of one loop is shown in Fig. 9.

Assuming that $V_{\rm dc}$ represents the dc offset introduced to the tuning loop and a first-order loop filter is used to suppress the multiplied signal and also in polarity decision branch, that is,

$$F(s) = \frac{g_m R_L}{1 + \frac{s}{\omega_{\rm LPF}}} \tag{31}$$

$$F_P(s) = \frac{g_{mP} R_{\rm LP}}{1 + \frac{s}{\omega_{\rm LPFP}}}. \tag{32}$$

We assume the output of the LPF is not too large so that the limiter can be regarded as an amplifier. When the loop is in the vicinity of the steady state, the dc offset has been tuned to close to a constant value and so does the gain of the multiplier. Based on these assumptions, the closed-loop transfer function of the loop can expressed as (33), shown at the bottom of the page, where $A_1 = k_m k_1 k_{\rm inte} g_m R_L$ and $A_2 = k_{\rm inte} k_1 g_{mP} R_{LP}$ denote the loop gains. A reasonable assumption is that $V_{\rm dc}(0)$ is bounded by a finite value, thus we have (34), shown at the bottom of the page.

Typically, the dc offset is a step signal, i.e., $V_{dc}(s) = 1/s$, and hence it can be derived that

$$\lim_{t\to\infty} e(t) = 0. \tag{35}$$

From (35), we can see that the dc offset can be fully cancelled when the tuning loop converges.

VI. Simulation and Experiment Result

A. Large-Signal Simulation

Based on the modified scheme described above, the large-signal behavior of the tuning loop [(36)–(40)] is simulated in MATLAB. For comparison, the tuning loop with varying- and fixed-bandwidth LPFs are evaluated separately and the results are shown in Fig. 10(a), where the x-axis is the number of iteration steps which is representative of the time. DC offset is introduced at $n = 100$, and the result shows that the varied LPF bandwidth is an efficient way to achieve faster settling time. Fig. 10(b) shows the tuning result when dc offset of the I and Q path has different polarity. It can be seen that the dc-offset tuning functions correctly and tuning speed is not affected by the polarities. In both cases, the tuning loop can remove dc offset even with 10% I/Q mismatch, which shows the tuning loop can cancel dc offset and suppress I/Q mismatch simultaneously.

B. Circuit-Level Simulation

Simulations of the dc-offset tuning loop at circuit-level have been done extensively with HSPICE. A typical simulation result is shown in Fig. 11. The setup for the simulation is as follows. The VGA is set to the highest gain of 20 dB. DC offset in the differential input of VGA is set to 10 mV [1], and 10% mismatch is introduced to I/Q transconductance transistors. The dc offset is introduced at $t = 4$ μs. The circuit simulation result shows that it takes approximately 8 μs for the tuning loop to suppress the differential dc offset to a level less than 3 mV.

C. Measurement Results

The full three-stage VGA with three tuning loops has been fabricated in a standard 0.35-μm CMOS technology and is

$$\frac{e}{V_{\rm dc}}(s) = \frac{s\left(1+\frac{s}{\omega_{\rm LPF}}\right)\left(1+\frac{s}{\omega_{\rm LPFP}}\right)}{s\left(1+\frac{s}{\omega_{\rm LPF}}\right)\left(1+\frac{s}{\omega_{\rm LPFP}}\right) + A_1\left(1+\frac{s}{\omega_{\rm LPFP}}\right) + A_2\left(1+\frac{s}{\omega_{\rm LPF}}\right)} \tag{33}$$

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} se(s) = \lim_{s\to 0} \frac{s\left(1+\frac{s}{\omega_{\rm LPF}}\right)\left(1+\frac{s}{\omega_{\rm LPFP}}\right)}{\left(1+\frac{s}{\omega_{\rm LPF}}\right)\left(1+\frac{s}{\omega_{\rm LPFP}}\right) + A_1\left(1+\frac{s}{\omega_{\rm LPFP}}\right) + A_2\left(1+\frac{s}{\omega_{\rm LPF}}\right)} V_{\rm dc}(s) \tag{34}$$

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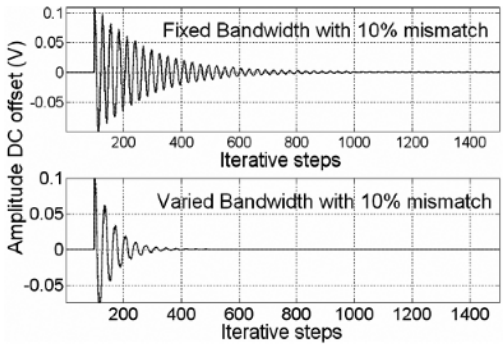
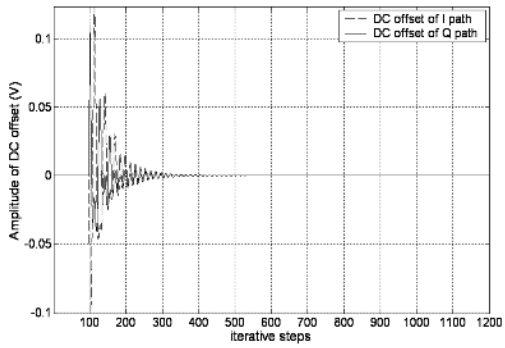
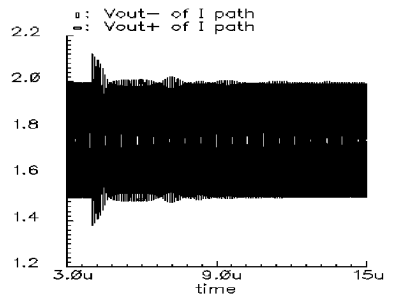


(a)

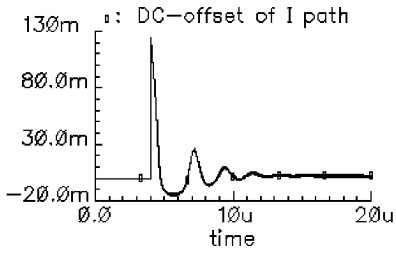


(b)

Fig. 10. Settling behavior of the dc-offset tuning loop (MATLAB simulation): (a) dc offset of I and Q path with the same polarity and (b) dc offset of I and Q path with different polarity.



(a)



(b)

Fig. 11. Circuit-level simulation of the tuning loop: (a) signal at I path and (b) dc-offset tuning process.

housed in a 24-pin QFP package. Fig. 12 shows the microphotograph of the fabricated chip. The core area is 1.7 mm $\times$ 1.5 mm. All components are integrated in the chip. The total current consumption is 9.1 mA, where the three-stage VGAs with buffers consume 4.2 mA, the three-stage tuning loop consume 3.6 mA, and the exponential circuits consumes 1.3 mA.

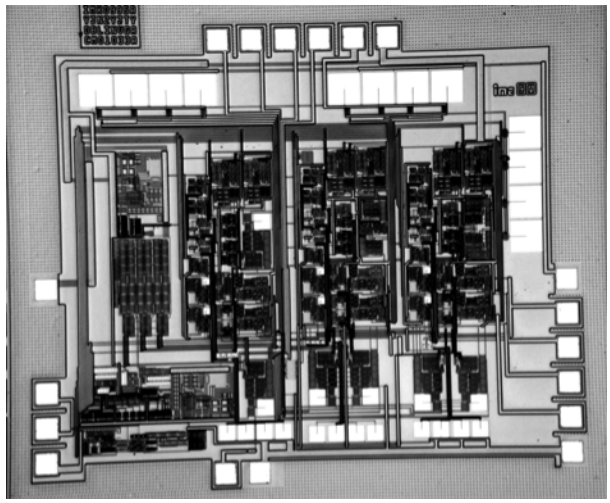


Fig. 12. Chip photograph of the dB-linear VGA with tuning loop.

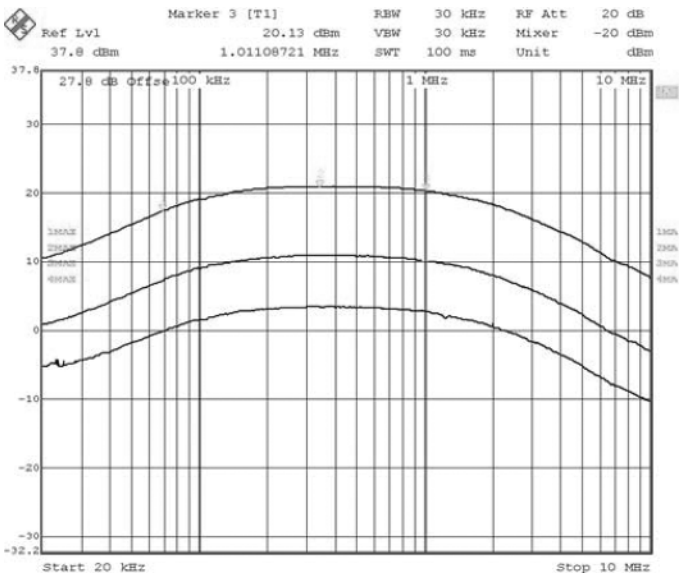


Fig. 13. AC response of the VGA.

AC response of one VGA stage is measured and shown in Fig. 13 and the bandpass characteristic is evident. The high-pass cutoff frequency is 67 kHz and the -3 dB bandwidth is 2.78 MHz. Due to the limitation of the test instrument, the frequency response at dc cannot be displayed directly. Based on the slope of -10 dB/Decade for the low frequency roll-off, we can extrapolate the curve for five decades from 67 kHz to 0.67 Hz. The resulting dc gain is about -30 dB at 0.67 Hz, which implies a dc-offset rejection of > 50 dB.

Measurement results of dB-linearity of the VGA are shown in Fig. 14. The gain of the VGA can be adjusted continuously from 0 to 20 dB. Reasonably good linearity is achieved with the pre-distortion techniques when the input voltage is less than 1 V, and the VGA gain varies from 0 to 12 dB. When the input voltage increases larger than 1.2 V, the gain curve exhibits some saturation. This can be explained as follows. To make approximation (8) accurate, the condition $-0.575 < 2g_b V_{\text{in}}^c/4I_0 < 0.815$ should be satisfied. Furthermore, to omit the third term in (15), the condition $g_m \gg K\left[4I_0 \exp\left(g_b V_{\text{in}}^c/2I_0\right)\right]$ should be

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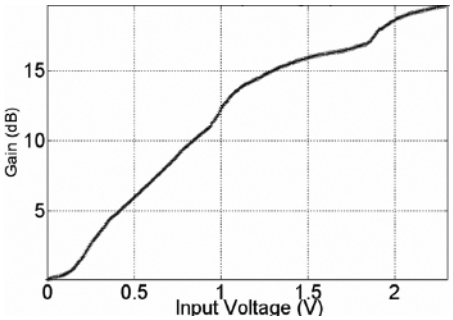

Fig. 14. Measurement results of dB linearity.

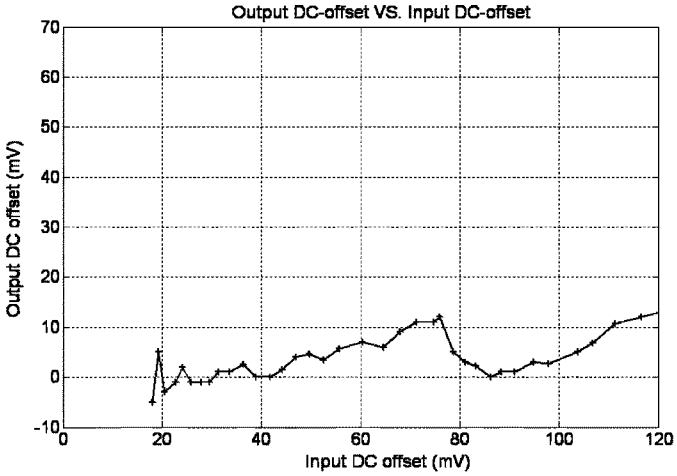

Fig. 15. Measurement result of dc-offset rejection performance.

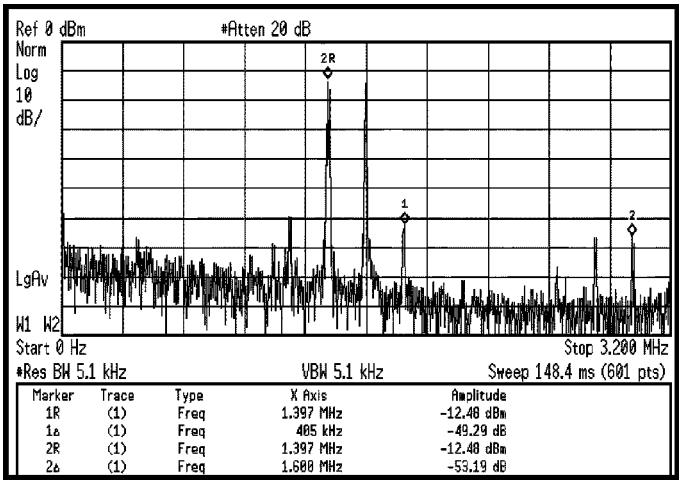

Fig. 16. Two-tone test.

satisfied. However, when the input control voltage $V_{\rm in}^{c}$ becomes larger, these two conditions are not met, and thus the dB linearity becomes poor.

The measured result of dc-offset cancellation is shown in Fig. 15. A dc offset is intentionally added at the input of VGA, and the dc voltage is measured at the output. VGA is set to the highest gain of 20 dB. The final output dc offset versus the input dc offset is shown in Fig. 15. The output dc offset can be suppressed effectively when the input dc offset is up to 120 mV. The highest output dc offset is 14 mV. Because

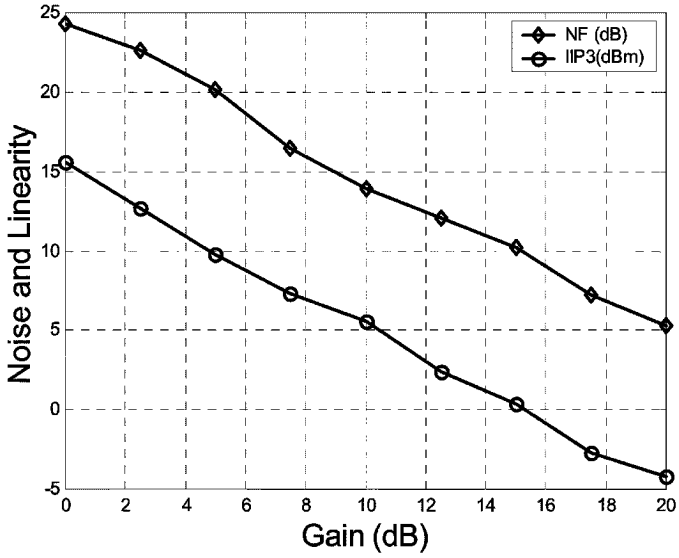

Fig. 17. Measured noise figure and IIP3 versus gain.

in practical applications the dc offset coming from the mixer will not exceed 100 mV, the dc-cancellation ability of the tuning loop has met the requirement of DCR. For testing of three stages of VGA, the bandwidth is slightly reduced due to cascaded stages. The other results are similar to those of single stage. The measured settling time of dc-offset cancellation are 19.5–21.3 μs and 7.7–8.5 μs (at different gain settings) by using fixed and variable bandwidth scheme respectively. Compared with conventional dc-offset cancellation schemes which normally employ fixed high-pass bandwidth (e.g., [1], [13], [19]), the proposed adaptive variable bandwidth scheme can achieve 2.5 times faster settling than the conventional ones without losing the tuning accuracy.

Fig. 16 shows the measured receiver two-tone test output spectrum. The two-tone input signals are at 1.4 and 1.6 MHz with power levels of -12 dBm. The second-order inter-modulation product, which is located at 3 MHz (marker 2$\diamond$, offset 1.600 MHz), is 53.2 dB below the desired signal. This translates to an input-referred second-order intercept point (IIP2) of 41.2 dBm. Similarly, the third-order inter-modulation product, which is located at 1.8 MHz (marker 1$\diamond$, offset 405 kHz), is 49.29 dB below the desired signal. Therefore, the input-referred third order intercept point (IIP3) of the VGA is $+12.65$ dBm. The measured Noise figure and IIP3 at different gains are shown in Fig. 17. Finally, the measurement results and the comparison with other VGA designs are summarized in Table III. From comparison, we can see the proposed VGA design achieves large dynamic range, good noise figure and IIIP3 with comparable power consumption. Moreover, it can remove dc offset and suppress I/Q mismatch simultaneously with accelerated setting time.

VII. Conclusion

A CMOS dB-linear VGA for DCR with dc-offset suppression is presented. The VGA has achieved gain control range over 60 dB. A good dB linearity is achieved with the proposed exponential function generation circuit and pre-distortion technique.

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TABLE III
COMPARISONS OF VGA PERFORMANCE

	Gain (dB)	BW (MHz)	Current (mA)	dB linearity	Noise Figure (dB)	IIP3 (dBm)	DC offset rejection	Process
[19]	0-134	2.5	--	Gain Step: Coarse: 2 dB Fine:0.5 dB	--	--	300mV DC offset input tolerance	0.35-μm
[20]	-35-55	30-210	11	Continuous	8 @Gmin	8@Gmin	--	0.25-μm
[21]	-9-15	1.6	1.67	Gain step: 5 dB	--	IM3: -40dBc	--	0.5-μm
[22]	-42-42	20-350	3.0	Continuous	7@Gmax	-22@Gmax +20@Gmin	--	0.25-μm
[23]	-6-24	4	0.9	Gain step: 0.55 dB	16.5 $nV/\sqrt{Hz}$	30(OIP3)	--	1.2-μm
[24]	-10-20	0.5-30	1.35	Gain step: 1 dB	11.2 $nV/\sqrt{Hz}$	29.2(OIP3)	--	0.18-μm
[25]	0-16	3.84	1	--	4	3	Highpass cutoff 4kHz	0.18-μm
This work	0-60	2.87	9.1 (I/Q)	Continuous	5.2@Gmax 24.1@Gmin	-4@Gmax 16.2@Gmin (IIP2: 41.2)	On-chip >50 dB rejection (DC offset I/Q mismatch)	0.35-μm

A novel dc-offset suppressing technique has been demonstrated. The measured result has shown that the dc-offset tuning loop is able to reduce the dc offset to less than 14 mV for the input dc offset up to 120 mV. Both dc offset and I/Q mismatch can be suppressed by the tuning loop simultaneously.

APPENDIX
LARGE-SIGNAL DYNAMICAL BEHAVIOR

Differential equations are employed to evaluate the large-signal transient response of the tuning loop in Fig. 5. Assuming $V_{\rm inI}(V_{\rm inQ})$ and $V_I(V_Q)$ denote the input and output signal of the $I(Q)$ path. R_I and R_Q denote the output resistor of the buffer in the I and Q paths, respectively. $C_{1,I}(C_{1,Q})$, $Y_{1,I}(Y_{1,Q})$, and $R_{1,I}(R_{1,Q})$ denote the capacitance, the transconductance, and the output resistance of the LPF_P in the $I(Q)$ path. For $C_{\rm int,I}(C_{\rm int,Q})$, $Y_{VI,I}(Y_{VI,Q})$ and $Y_{\rm int,I}(Y_{\rm int,Q})$, the first subscript denotes the function block and the second one denotes the $I(Q)$ path. Other coefficients are as defined earlier. Assuming that a first-order LPF is used, the behavior of the tuning loop can be described as

$$V_I(t) = V_{\rm inI}(t) + V_{\rm dcI}(t) - R_I Y_{VI,I}\frac{Y_{{\rm int},I}}{C_{{\rm int},I}} \times \int \left[k_{1I,I}V_{1I}(t) + k_{1Q,I}V_{1Q}(t) + k_{2,I}k_l \mathrm{sign}\left(V_Q(t)\right)V_{\rm LPF}(t)\right]dt \quad (36)$$

$$V_Q(t) = V_{\rm inQ}(t) + V_{\rm dcQ}(t) - R_Q Y_{VI,Q}\frac{Y_{{\rm int},Q}}{C_{{\rm int},Q}} \times \int \left[k_{1I,Q}V_{1I}(t) + k_{1Q,Q}V_{1Q}(t) + k_{2,Q}k_l \mathrm{sign}\left(V_I(t)\right)V_{\rm LPF}(t)\right]dt \quad (37)$$

and

$$\frac{V_{1I}(t)}{R_{1,I}} + C_{1,I}\frac{dV_{1I}(t)}{dt} = Y_{1,I}V_I(t) \quad (38)$$

$$\frac{V_{1Q}(t)}{R_{1,Q}} + C_{1,Q}\frac{dV_{1Q}(t)}{dt} = Y_{1Q}V_Q(t) \quad (39)$$

$$k_m Y_{\rm LPF}V_I(t)V_Q(t) = \frac{V_1(t)}{R_{\rm LPF}} + C_{\rm LPF}\frac{dV_1(t)}{dt}. \quad (40)$$

It is difficult to solve (36)–(40) analytically. Therefore, a trapezoidal operator is used to calculate the numerical solution. The trapezoidal operator is a third-order operator and can ensure that the approximation has sufficient precision [18].

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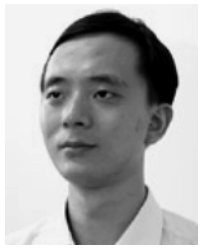

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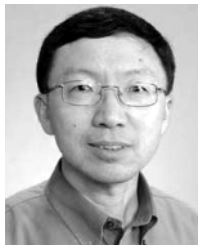

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