A Compact Adder and Reprogrammable Logic Gate Using Micro-Electromechanical Resonators With Partial Electrodes

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***Abstract*—In this brief, the design principles and experimental demonstration of a compact full adder along with a reprogrammable 4-input logic gate are presented. The proposed solution for implementation of digital circuits is based on a clamped–clamped micro-beam resonator with multiple split electrodes, in which the logic inputs tune the resonance frequency of the beam. This technique enables re-programmability during operation, and reduces the complexity of the digital logic design significantly; as an example, for a 64-bit adder, only 128 micro-resonators are required, compared to more than 1500 transistors for standard complementary metal–oxide–semiconductor (CMOS) architectures. We also show that an optimized simulated micro-resonator-based full adder is 45 times smaller than a CMOS mirror adder in 65-nm technology. While the energy consumption of this early generation of micro-resonator logic gates is higher than the CMOS solutions, we show that by careful device optimization and shrinking of the dimensions, femtojoules energy consumption and MHz operation, required by Internet of Things applications, are attainable.**

***Index Terms*—Micro-beam resonator, electromechanical computation, electrostatic softening effect, low power logic design, adder.**

I. Introduction

THE CONTINUOUS miniaturization of the complementary-metal-oxide-semiconductor (CMOS) technology has led to higher operational speeds, while the leakage energy and power density have increased. However, IoT devices and sensors do not require high performance and only require moderate data transmission and computation speeds, in the range of sub-kHz to 100 MHz [1], [2]. The most critical aspect in such applications is the energy-efficiency of battery-operated, often stand-alone sensors and gadgets. Therefore, alternative low-power computing techniques have been recently sought after. In particular, the interest in mechanical computations has renewed due to the advancements in lithography and fabrication techniques. Micro/nano-electromechanical (NEMS/MEMS) relays offer a low power alternative for integrated circuit applications due to their zero off-state current [3]. MEMS/NEMS structures were used to implement different logic gates [4], [5]. Despite their cascadability and low power consumption, relays suffer from major shortcomings, such as low contact reliability, high contact resistance, and wearing, which limit their practical applications [6]. Micro-electromechanical resonators provide a more reliable option as their operation depends on the amplitude of the vibrating resonator rather than physical contacts. The output logic high (low) is defined as the on-resonance (off-resonance) signal. In order to implement a micro-resonator based arithmetic and logic operation unit (ALU) of a microprocessor, basic logic gates and computing blocks such as adders are required. The first resonator-based logic device was a NEMS piezoelectric XOR gate [7]. Later, reprogrammable micro and nano-electromechanical logic gates were demonstrated using different techniques, such as frequency mixing [8], electro-thermal [9]–[11], and electrostatic [12] frequency tuning, and parametric resonances excitation [13]. A reversible logic gate has been demonstrated via electrically coupled resonators [14].

In this brief, a general 4-input reprogrammable logic gate and the first micro-resonator based full adder are presented. Although the proposed device and our previous device presented in [12] use the same physical phenomena, namely resonance frequency tuning by electrostatic softening effect, there are several differences between the two works. The major differences are the number of partial electrodes and digital inputs, the number of applied drive frequencies, the impact of the location of drive, sense and digital input electrodes, the overall design methodology and the circuit applications. We show that the application of two drive frequencies, instead of a single frequency as in [12], along with increased number of input electrodes, can result in a significantly more compact and energy efficient design for critical digital circuit blocks, such as adders. This is different from [11], where multiple 2-input

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devices from [9] were used to implement a 4-input XOR gate using conventional CMOS design techniques.

The rest of this brief is organized as follows. In Section II, the device structure, operation, and simulation results are presented. Section III shows the experimental results. A thorough discussion on energy and speed trade-offs and prospect for miniaturized resonators is presented in Section IV, followed by concluding remarks in Section V.

II. Device Structure and Operation Principles

The device consists of an in-plane clamped-clamped microbeam with six split electrodes. The device is fabricated using a silicon on insulator (SOI) wafer with a highly doped device layer. First, a metal bi-layer consisting of Cr/Au is lifted off to define the contact area, followed by deep reactive ion etching (DRIE) of the silicon device layer to define the beam and the side electrodes. Finally, the beams are released using vapor HF.

For the operation of the device, the logic inputs, which are DC signals, are applied at the four corner electrodes, as shown in Fig. 1(a) and (b). One of the middle electrodes is used for electrostatically driving the beam while the opposite electrode is used for sensing the output motional signal. When the frequency of the applied AC signal matches the resonance frequency of the beam, it resonates and a relatively high output signal is detected. This defines the output logic 1. On the other hand, the output signal is very low in the off-resonance state; thus defining the output logic 0. The operation of the device depends on modulating the resonance frequency of the beam by the applied logic inputs through the electrostatic softening effect. The four corner electrodes were selected for applying the logic inputs as they have the same loading effect on the beam. Theoretically, the input combinations that have the same number of logic 1's should result in reasonably close resonance frequencies for the beam. So, for four inputs, we expect to have five different resonance frequencies (f_0-f_4), where f_n corresponds to n logic 1 inputs. To verify the concept, a finite element simulation using COMSOL software (Electro-Mechanics Physics, Structural Mechanics module and pre-stressed Eigen-frequency study), was performed to find the resonance frequencies of the beam for all different combinations. Four DC voltage signals were applied at the four corner electrodes while the drive and sense electrodes were grounded. Logic 1 for the inputs is 25V, while logic 0 is 0V. The beam is biased with 60V. Parametric sweep was performed on the four inputs and the resonance frequency of the beam was calculated for the sixteen different combinations from 0000 to 1111. Fig. 1 (c) indicates that both simulation results (squares) and experimental data (circles) have the same trend in frequency shift in the different states. However, a small deviation is noted due to residual stresses and imperfections in the fabricated device, which are not accounted for in the model. These stresses can be minimized by optimizing the fabrication process to control the stress in the beam.

We should mention here that for proper operation of the device, it is very important to make sure that the resonance frequency shift Δf between two adjacent cases, for example: the cases of all zeros and single ones, is greater than the full-

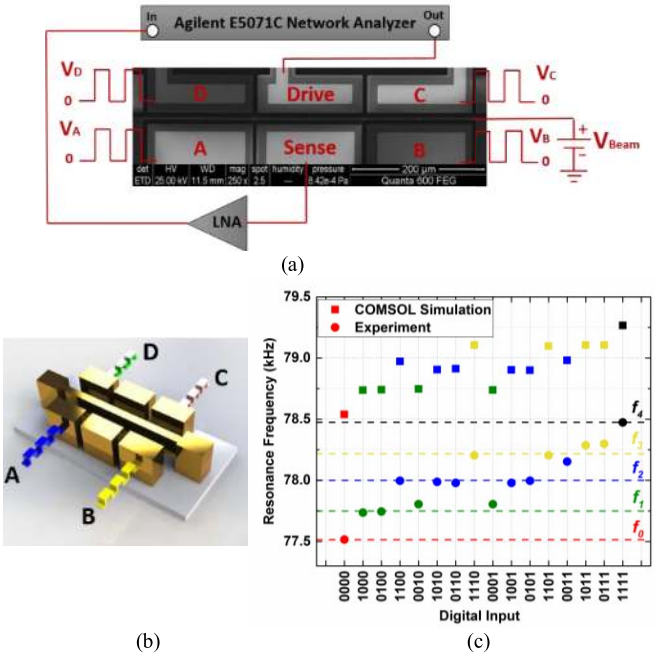

Fig. 1. (a) SEM image of the device showing the experimental setup. (b) 3D Schematic of the micro-resonator with six partial electrodes. The beam is 500μm long, 2.3μm wide and 30μm thick. The air gap between each electrode and the beam is 8μm. (c) COMSOL simulation results (squares) and experimental data (circles).

width at half maximum power, which is defined as

$$\Delta f = 2f_0/Q, \tag{1}$$

where f_0 is the resonance frequency and Q is the quality factor [14]. Based on the proposed operating principle, two different applications will be discussed, multi-input logic gates and a full adder.

A. Reprogrammable Logic Gates

The proposed logic device is reprogrammable such that different gate operations can be achieved by selecting different operating frequencies. In order to realize a 4-input NOR gate, an AC signal with frequency f_0 is applied to the drive electrode. In this case, only the-all-zeros input state will match the resonance frequency of the beam with input frequency f_0, hence a high output signal (on-resonance) is obtained. The rest of the input combinations will shift the beam's resonance frequency to values different from f_0 and will result in a low output signal (off-resonance). Similarly, applying the frequency of all-ones case (f_4) to the drive electrode will program the device to work as a 4-input AND gate.

B. Full Adder Operation

The full adder device has three inputs (A, B, C_{in}) and two outputs (Sum, C_{out}), where A and B are the two digits that should be added, C_{in} is the carry in, and C_{out} is the carry out. The outputs of the full adder are described as follows:

$$Sum = A \oplus B \oplus C_{in}, \quad C_{out} = AB + AC_{in} + BC_{in}$$

The sum is basically a three-input XOR gate while the carry is a majority function which means that the output is high

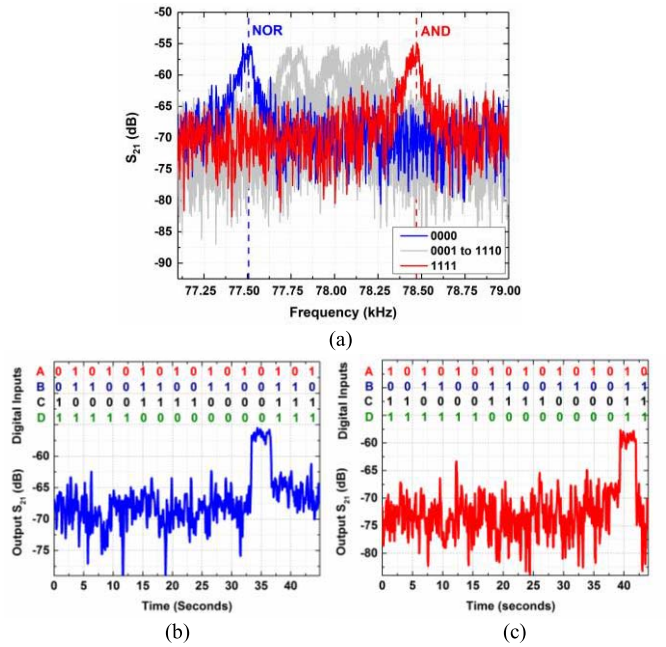

Fig. 2. (a) Frequency response for all input combinations. The 0000 and 1111 cases are highlighted as they are used for NOR and AND gate operations, (b) Time response for a 4-input NOR operating at 77.5 kHz, (c) Time response for a 4-input AND operating at 78.47 kHz.

if the input contains at least two ones. Unlike the case of AND and NOR gates that require only a single frequency for operation (f_0 and f_4, respectively), each output of the full adder requires two frequencies to be applied simultaneously. For example, in order to implement the sum bit, the output must be high if the input vector contains single 1 or three 1's, so two different signals with frequencies f_1 and f_3 should be applied simultaneously. Similarly, the carry out output requires the application of two signals with the frequencies f_2 and f_3.

III. Results

Fig. 1(a) shows the experimental test setup and the SEM image of the device. First, a frequency sweep is performed for each logic combination. Next, the sixteen frequency responses from the sixteen input combinations are plotted together as shown in Fig. 2 (a), and the frequencies of operation of the five different cases (f_0, f_1, f_2, f_3, f_4) are determined. After that, the time response is obtained by fixing the frequency of the applied AC signal at the drive electrode to the frequency of interest and varying the logic inputs.

A. Logic Gates

As explained earlier, 4-input NOR gate and 4-input AND gate can be obtained by selecting the right operating frequency. Fig. 2 (a) shows the frequency response of the 16 combinations. The blue curve represents the frequency response of the micro-resonator under all zeros case ABCD=0000. The NOR gate is implemented by fixing the frequency of the AC signal at the drive electrode to 77.5 kHz. Fig. 2 (b) shows the output S_{21} parameter for the NOR gate for different inputs (V_A, V_B, V_C, and V_D). Only all zeros case results in a high output signal while the other fifteen cases result in a low output signal at the given operating frequency. The red curve in Fig. 2 (a) represents the frequency response for 1111 case. Similarly, by fixing the frequency of the drive signal at 78.47 kHz, the AND logic gate can be realized as shown in Fig. 2 (c).

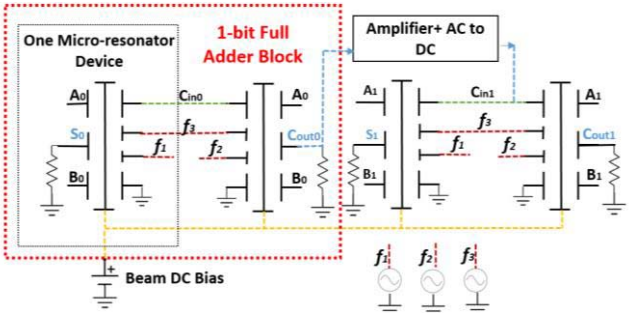

Fig. 3. Block diagram of a 2-bit micro-resonator based full adder.

B. Full Adder

For the full adder, shown in Fig. 3, three corner electrodes are used as inputs and the fourth electrode is grounded. Fig. 4 (a) shows the frequency response of the eight different input combinations of a full adder. The black curve represents the beam's frequency response under all zeros condition 000 with resonance occurring at 77.5 kHz (f_0). The pink, dark green and blue curves represent the frequency response of the beam when only one input is high. Although theoretically speaking all those cases should result in the same resonance frequency for the beam, the case of "001" is slightly shifted to the right due to fabrication imperfections. However, the shift is tolerable and the resonance peaks of the three cases intersect at 77.75 kHz (f_1), which is chosen as the operating frequency for the single one case. For the case of two 1's the resonance occurs at 78 kHz (f_2). Finally, the all-ones case shifts the resonance frequency of the beam to 78.2 kHz (f_3).

After identifying the resonance frequencies, the drive electrode is fixed at the frequency of interest and the time response is measured. To obtain the sum output, two frequencies (f_1 and f_3) should be applied simultaneously to the device. This can be done in different ways, for instance by electronically mixing the two frequencies and applying them to the same electrode, by applying the two signals to separate electrodes or by applying one frequency to the drive electrode, and combining the other frequency with the beam DC bias using a bias tee. However, due to some limitations in our current experimental setup, only one frequency could be applied and detected at the same time. As shown in Fig. 4 (b), the sum was obtained in two steps, first by applying the frequency of single one (f_1), the blue curve, followed by applying the frequency corresponding to the three-ones case (f_3), the green curve. Similarly, the carry is obtained by applying (f_2), the orange curve, followed by (f_3), the green curve.

IV. Discussion

It is of paramount importance to highlight the potential advantages and possible obstacles in using micro/nano-resonator technology in building logic blocks. Some of the important aspects that are discussed in this

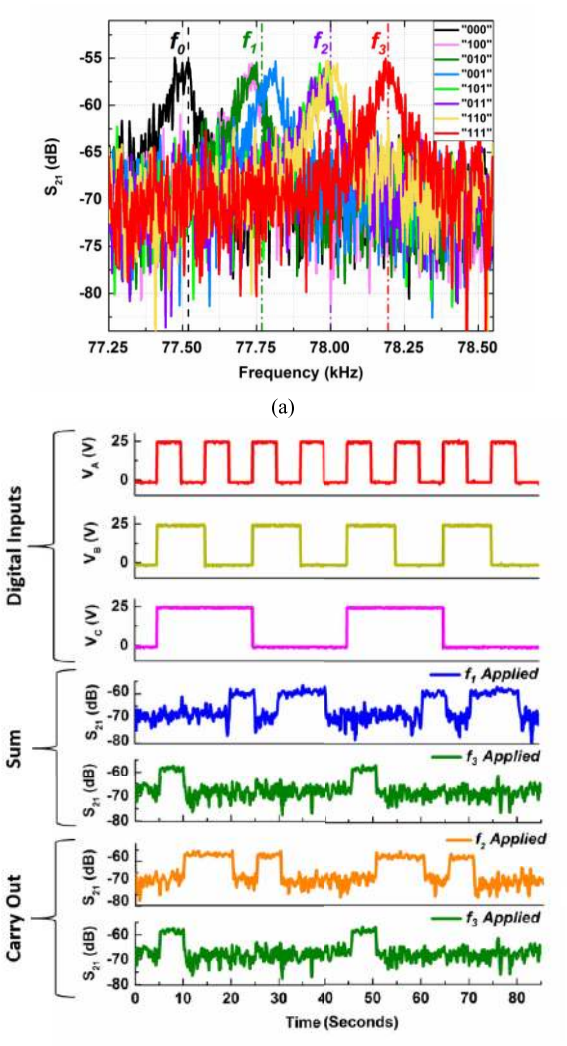

Fig. 4. (a) Frequency response of the resonator for the 8 different combinations, with the 4th bit fixed to 0, (b) Time response showing the full adder outputs.

section include speed, energy consumption, area requirement, complexity and cascading plan. Other aspects like frequency stability and temperature stability have been discussed in [12]. The speed of the device is determined by the mechanical transition time t_s, which is determined by (Q/f), where Q is $\approx$ 1000 operating at 700 mTorr and f is the resonance frequency. The mechanical transition time for this device is estimated to be 12.98 ms, which limits the speed of the resonator to $\approx$ 77 Hz. However, the speed can be increased by two means: either by reducing the quality factor of the resonator, which adversely affects the signal to noise ratio or by designing the resonator to operate at higher frequencies (megahertz or gigahertz) as shown in Table I. By doing that, an operating speed in megahertz is potentially achievable. Another important evaluation metric is the consumed energy per logic operation. The total energy per logic operation for the current device has two components: switching energy (E_{Switch}) and ac activation energy ($E_{Activation}$)

$$E_{Total} = E_{Switch} + E_{Activation} \tag{2}$$

$$E_{Switch} = \frac{1}{2}C\begin{bmatrix} (V_{Beam}^2 - (V_{Beam} - V_A)^2) + \\ (V_{Beam}^2 - (V_{Beam} - V_B)^2) + \\ (V_{Beam}^2 - (V_{Beam} - V_C)^2) + \\ (V_{Beam}^2 - (V_{Beam} - V_D)^2) \end{bmatrix}, \tag{3}$$

where C is the capacitance between one split electrode and the beam, which is around 5.17 fF, V_{Beam} is the beam DC bias. In order to calculate the switching energy per logic operation, we need to calculate the average of the energies for the different combinations. For the four input NOR and AND gate, the switching energy per operation is 13.1 pJ. For the full adder, which is comprised of two micro-resonators with three inputs, the switching energy per operation is 18.7 pJ. Note that the switching energy can be significantly reduced by decreasing the capacitance and the operating voltages, which can be done by careful shrinking and optimization of the device dimensions and its stiffness as shown in Table I. The activation energy can be calculated using (4)

$$E_{Activation} = t_s \times V^2/Z \tag{4}$$

$$Z = 50 \times 10^{\frac{S_{21}}{20}}, \tag{5}$$

where V is the RMS value of the applied AC signal and Z is the impedance of the micro-resonator which can be calculated using (5) [12]. With measured insertion loss of 80 dB, the impedance of the micro-resonator was found to be around 500 kΩ. With V=5 mV (RMS), the activation energy is $\approx$ 0.6 pJ. The total energy per operation for a logic gate is 19.3 pJ, while the full adder's total energy per operation is 18.7 pJ. Note that the total energy is dominated by the switching energy, which can be reduced by optimizing the device dimensions.

Table I summarizes the energy, speed, and area of simulated micro-resonator design with different dimensions and resonance frequencies. Reducing device dimensions in design 2, 3 and 4 enables the use of lower voltages for the logic 1 and the beam bias compared to the tested device (design 1). This reduces the energy per operation by more than three orders of magnitude. In addition, the higher resonance frequencies of designs 2-5 result in faster operation. Note that in Table I, design 3, 4, and 5 show that for the same resonator dimensions, by lowering the quality factor, which can be partially controlled by the vacuum level during testing, the speed increases. However, the minimum required separation between the different resonance peaks increases according to (1) and higher voltages will be required to ensure that, which results in higher energy per operation.

Looking into the complexity aspect, a standard CMOS 4-input NOR/AND gate requires 8/10 transistors, while the same operations can be performed using only one reprogrammable micro-resonator device. Similarly, a mirror adder in CMOS technology requires 28 transistors, while it can be implemented with only two of the proposed micro-resonator-based devices. Note that if the same function is implemented with the micro-resonator proposed in [12], 8 devices will be required. A comparison between a micro-resonator adder and CMOS mirror adder [15] is shown in Table II. The miniaturized resonator based adders are approximately 45 times smaller than the standard mirror adder in 65nm CMOS technology. The energy per operation for micro-resonator adders is

TABLE I
SPEED, AREA AND POWER CONSUMPTION OF THE PROPOSED MICRO-RESONATOR DESIGN WITH DIFFERENT DIMENSIONS. THE QUALITY FACTOR (Q) CAN BE PARTIALLY CONTROLLED BY VACUUM LEVEL. L, W, G AND T ARE THE BEAM LENGTH, WIDTH, BEAM/ELECTRODE AIR GAP AND BEAM THICKNESS

Design	Beam Dimensions (μm)				Area (μm^2)	Resonance Frequency *(f)*	Q_{min}	Speed *(f/Q)*	Beam Bias	Inputs (V)		Switching Energy/Op	Total Power Switching + Activation
	L	W	G	T						'0'	'1'		
1 (measured)	500	2.3	8	30	10150	77 kHz	1000	77 Hz	60 V	0	25	9.23 pJ	0.71 nW
2	20	0.35	0.45	0.35	37	6 MHz	1600	6 kHz	15 V	0	5	4.3 fJ	17.82 pW
3	0. 66	0.05	0.05	0.05	0.28	0.96 GHz	10^4	90 kHz	15 V	0	5	0.166 fJ	19.88 pW
4							1280	0.75 MHz	30 V	0	10	0.664 fJ	0.5 nW
5							640	1.5 MHz	30 V	0	30	1.195 fJ	1.79 nW

TABLE II
COMPARISON BETWEEN THE PROPOSED FULL ADDER DESIGN AND CMOS MIRROR ADDER IN 65NM TECHNOLOGY

Speed	Micro-resonator Full Adder			Mirror Adder in CMOS 65nm Technology		
	Energy/Op	Power	Area (μm^2)	Energy/Op	Power	Area (μm^2)
77 Hz (Design 1)	18.7 pJ	1.4 nW	20300	220 pJ	16.94 nW	32
6 kHz (Design 2)	8.8 fJ	35.6 pW	74	1.412 pJ	16.94 nW	
90 kHz (Design 3)	0.443 fJ	39.8 pW	0.7	94.41 fJ	16.97 nW	
0.75 MHz (Design 4)	1.34 fJ	1 nW		11.87 fJ	17.59 nW	
1.5 MHz (Design 5)	2.39 fJ	3.59 nW		6.32 fJ	18.9 nW	
Number of Devices	2			28 transistors		

one to two orders of magnitude lower than the CMOS counterparts, up to the operation frequency of a few MHz. It's worth mentioning that the speed can be increased to GHz by choosing the right material and design of a resonator with THz resonance frequency [16]. The proposed design methodology could also be applied to optical resonators reporting 10 Gbps speed [17]. Another observation here is that the inputs and the outputs of the micro-resonator device are not compatible (DC inputs and AC output). Therefore, a signal conditioning circuit is required between different stages (Fig. 3). We are currently investigating design strategies, such as resistive termination between logic stages [18], to minimize the need for extra signal conditioning blocks.

V. CONCLUSION

We have demonstrated the design and operation of a 4-input reprogrammable logic gate and a full adder using microresonators. The operation of the device is based on the resonance frequency tuning of the beam by the logic inputs. The applied frequencies determine the function of the device. The energy per operation for the current device is in 10s of pico-joules and can be further reduced to femtojoule level by optimizing the structure to have high resonance frequency, low stiffness and moderate quality factor.

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REFERENCES

[1] D. Blaauw *et al.*, "IoT design space challenges: Circuits and systems," in *Symp. VLSI Technol. (VLSI Technol.) Dig. Tech. Papers*, 2014, pp. 1–2.
[2] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 3–29, Jan. 2012.
[3] S. Houri, G. Billiot, M. Belleville, A. Valentian, and H. Fanet, "Limits of CMOS technology and interest of NEMS relays for adiabatic logic applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1546–1554, Jun. 2015.
[4] H. Fariborzi *et al.*, "Design and demonstration of micro-electromechanical relay multipliers," in *Proc. IEEE Asian Solid-State Circuits Conf.*, 2011, pp. 117–120.
[5] M. Spencer *et al.*, "Demonstration of integrated micro-electromechanical switch circuits for VLSI applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 308–320, Jan. 2011.
[6] D. A. Czaplewski *et al.*, "Lifetime limitations of ohmic, contacting RF MEMS switches with Au, Pt and Ir contact materials due to accumulation of 'friction polymer' on the contacts," *J. Micromech. Microeng.*, vol. 22, no. 10, 2012, Art. no. 105005.
[7] S. C. Masmanidis *et al.*, "Multifunctional nanomechanical systems via tunably coupled piezoelectric actuation," *Science*, vol. 317, no. 5839, pp. 780–783, 2007.
[8] S. Ilyas, S. N. Jaber, and M. I. Younis, "MEMS logic using mixed-frequency excitation," *J. Microelectromech. Syst.*, vol. 26, no. 5, pp. 1140–1146, Oct. 2017.
[9] M. A. A. Hafiz, L. Kosuru, and M. I. Younis, "Microelectromechanical reprogrammable logic device," *Nat. Commun.*, vol. 7, Mar. 2016, Art. no. 11137.
[10] M. A. A. Hafiz, L. Kosuru, M. I. Younis, and H. Fariborzi, "Microelectromechanical resonator based digital logic elements," in *Proc. ESSDERC/ESSCIRC*, Lausanne, Switzerland, 2016, pp. 448–451.
[11] M. A. A. Hafiz, R. Li, M. I. Younis, and H. Fariborzi, "A parity checker circuit based on microelectromechanical resonator logic elements," *Phys. Lett. A.*, vol. 381, no. 9, pp. 843–848, 2017.
[12] M. A. A. Hafiz, S. Ilyas, S. Ahmed, M. I. Younis, and H. Fariborzi, "A microbeam resonator with partial electrodes for logic and memory elements," *IEEE J. Explor. Solid-State Computat. Devices Circuits*, vol. 3, pp. 83–92, 2017.
[13] I. Mahboob, M. Mounaix, K. Nishiguchi, A. Fujiwara, and H. Yamaguchi, "A multimode electromechanical parametric resonator array," *Sci. Rep.*, vol. 4, Mar. 2014, Art. no. 4448.
[14] J. S. Wenzler, T. Dunn, T. Toffoli, and P. Mohanty, "A nanomechanical Friedkin gate," *Nano Lett.*, vol. 14, no. 1, pp. 89–93, Jan. 2014.
[15] *Cadence Generic Process Design Kits (GPDK)*. Accessed: Feb. 2018. [Online]. Available: https://support.cadence.com/gpdk
[16] D. Svintsov, V. G. Leiman, V. Ryzhii, T. Otsuji, and M. S. Shur, "Graphene nanoelectromechanical resonators for the detection of modulated terahertz radiation," *J. Phys. D. Appl. Phys.*, vol. 47, no. 50, Dec. 2014, Art. no. 505105.
[17] F. K. Law, M. R. Uddin, H. Hashim, and Z. Hamid, "Simulation and demonstration of electro-optic digital logic gates based on a single microring resonator," *Opt. Quant. Electron.*, vol. 49, no. 12, p. 413, Dec. 2017.
[18] S. Ilyas, S. Ahmed, M. A. A. Hafiz, H. Fariborzi, and M. I. Younis, "Cascadable microelectromechanical resonator logic gate," *J. Micromechan. Microeng.*, vol. 29, no. 1, 2018, Art. no. 015007.