A Compact Low-Power Supply-Insensitive CMOS Current Reference

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***Abstract*—A simple low-power current reference using dual-threshold MOS transistors is introduced. The area required for this reference is small and the sensitivity of the output current to the supply voltage is low. Simulation results show that an implementation of this current reference in a TSMC 0.18um CMOS process with a 1.8V power supply is constant to within ±1.25% over the temperature range of -10˚C to 100˚C. In this implementation, the active area is 86 μm^2, the power dissipation is 72μW, and the worst process corner nonlinearity due to temperature variations is bounded by ±4.16%.**

I. INTRODUCTION

Current references are key building blocks in many mixed signal system. The performance of many analog and mixed-signal circuits depends on the proper biasing, linearity, and accuracy of current reference. As VLSI circuits become more complex there is an increasing emphasis on efficient, simple, and easy-to-design components. Traditionally, the bandgap voltage reference combined with a resistor is used to generate a reference current. However, the on-chip resistor is not attractive in basic CMOS processes because of the large area requirements, the process dependence, and the variation in the sheet resistance with temperature. Usually an additional amplifier is also required in this type of current reference thus increasing both power and area requirements [1].

Some works have incorporated a zero temperature coefficient (ZTC) bias point of the MOSFET to generate a temperature independent current reference [2]. The accuracy over temperature variations of current references designed using the ZTC bias point approach is limited by statistical variations in the process technology, because only under the conditions of mutual compensation between mobility and threshold voltage temperature effects in MOS transistors will the ZTC property be achieved. In the ZTC bias point approach, the compensation requires that the transistor threshold voltage is a linear function of temperature T and that the mobility is proportional to T^{-2}. The ZTC biasing point approach typically requires a bandgap voltage reference for biasing the gate voltage at the ZTC point and this increases both area and power requirements as well.

In this paper a simple, self-biased low-power CMOS current reference is introduced. It includes two like-type transistors with different threshold voltages and with different threshold temperature coefficients. The output current level can be adjusted with a programmable current mirror. The proposed circuit is comprised entirely of MOS transistors and is void of both resistors and operational amplifiers. The resultant circuit is compact, has a low sensitivity to both supply voltage and temperature variations, and has very low power requirements.

II. CURRENT REFERENCE ARCHITECTURE

Figure 1 illustrates the operating principle of the sensor. Two LNTC (Linear Negative Temperature Coefficient) current sources I_1 and I_2 are combined to generate a difference current $I_1 - I_2 \times N$ where N is the weighting factor of current source I_2. A current mirror scales this difference by a factor A and presents it as a sinking current at the output.

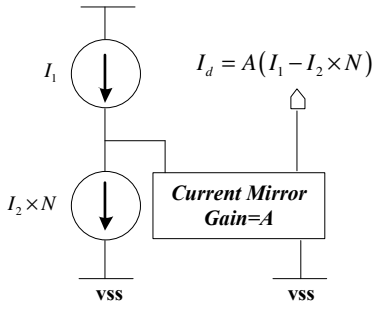

Figure 1. Proposed Current Reference Architecture

The temperature dependence of the output of the first LNTC current source can be expressed as

$$I_1 = k_1 \times T + I_{01} \quad (1)$$

where T is absolute temperature, I_{01} is the current level at 0K, and where k_1 is used to model the first order temperature coefficient of I_1. Since this is an LNTC source, k_1 is negative. The second LNTC current source can be modeled by the equation

$$I_2 = k_2 \times T + I_{02} \quad (2)$$

where k_2 and I_{02} are the corresponding characterization parameters. From equations (1) and (2), it can be easily shown that the difference current I_d between two scaled LNTC currents will be constant with absolute temperature under the condition that the scaling factor N satisfies the equation

$$N = k_1 / k_2 \quad (3)$$

When (3) is satisfied, the current Id can be expressed as

$$I_d = A \times (I_1 - N \times I_2) = A \times (k_{01} - N \times k_{02}) \quad (4)$$

The currents I_1, I_2, and I_d obtained when N satisfies (3) are depicted in Figure 2.

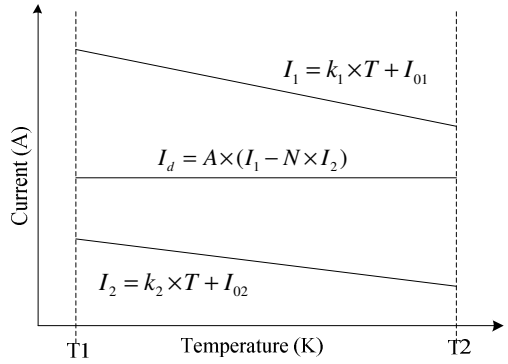

Figure 2. Temperature dependency of the key current in the current reference

To be practical, it is necessary that the current I_d not vanish nor change significantly in the presence of process variations. LNTC current sources can be designed in processes with dual threshold devices. As an alternative to subtracting the two LNTC currents, one could consider adding a LNTC current to a current with a linear positive temperature coefficient (LPTC). Unfortunately, in processes with a single-threshold n-channel device and a single-threshold p-channel device, the magnitude of the temperature coefficients and the magnitudes of 0K currents are often about the same so when combining to obtain a zero temperature coefficient, the difference current either vanishes or becomes highly sensitive to process variations.

III. Description of Proposed Circuit

Two CMOS LNTC current source circuits are described in this paragraph. One is a 4 MOSFET structure and the other is a 5 MOSFETs structure. Recent works [3] and [4] have discussed the operation of these circuits as two independent temperature sensors. In these earlier works, they were both designed to provide an output voltage that varies linearly with temperature (LNTC).

A. 4 MOSFET LNTC Current Source

The circuit structure of a 4 MOSFET LNTC current source is shown in the Figure 3. M1, M3 and M4 are normal transistors and M2 are high threshold voltage transistor. All the transistors are biased to operate in the saturation region. In this circuit, if channel length modulation and output conductance effects are neglected, it follows from the basic square-law model that the equations (5) and (6) describe the current in the two branches of the circuit.

$$I_{d1} = 1/2 \cdot \mu_n C_{ox} (W/L)_1 (V_1 - V_{tn1})^2 \quad (5)$$

$$I_{d2} = 1/2 \cdot \mu_n C_{ox} (W/L)_2 (V_1 - V_{tn2})^2 \quad (6)$$

If the current mirror gain is 1, I_{d1}=I_{d2}, and it follows upon eliminating V_1 that the current I_{d1} is

$$I_1 = I_{d1} = \frac{(V_{t2} - V_{t1})^2 \frac{1}{2} \mu_n C_{ox}}{\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} \right)^2} \quad (7)$$

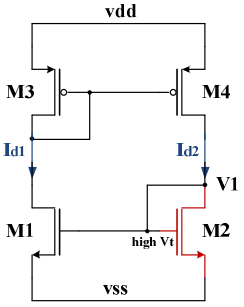

Figure 3. Circuit of 4 MOSFETs LNTC current source

The current flowing in the 4 MOSFET structure depends on threshold voltage, mobility, Cox and also the transistor sizes. Only mobility and threshold voltage are significantly temperature dependent. Both of these two parameters will affect the current temperature characteristics of I_1.

The threshold voltage is function of temperature and is often modeled by the linear equation,

$$V_{tn} = V_{t0} + KT1 \times T \quad (8)$$

where KT1 is the first order temperature coefficient of threshold voltage and is negative. The temperature dependence of the mobility function is typically modeled by the equation

$$\mu_n = \mu_0 \left(\frac{T}{T_0} \right)^{\beta} \quad (9)$$

Where T_0=300K, μ_0 is the mobility at T=300K, and β is the mobility potential factor. Typically -2<β<-1. Substituting the threshold voltage and mobility temperature dependencies into (7), it follows that

$$I_1 = I_{d1} = \frac{(\Delta V_{t0} + \Delta KT1 \times T)^2 \frac{1}{2} \mu_0 \left(\frac{T}{T_0} \right)^{\beta} C_{ox}}{\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} \right)^2} \quad (10)$$

$$= \left(\Delta V_{t0}{}^2 T^{\beta} + 2 \times \Delta V_{t0} \times \Delta KT1 \times T^{\beta+1} + \Delta KT1^2 \times T^{\beta+2} \right) \times C$$

where C, ΔV_{t0}, and $\Delta KT1$ are defined as

$$C = \frac{\frac{1}{2}\mu_0 \left(\frac{1}{T_0}\right)^{\beta} C_{ox}}{\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}}\right)^2} \tag{11}$$

$$\Delta V_{t0} = (V_{t0})_1 - (V_{t0})_2 \tag{12}$$

$$\Delta KT1 = (KT1)_1 - (KT1)_2 \tag{13}$$

The subscripts "1" and "2" correspond to M_1 and M_2 respectively.

The expression (10) is not perfectly linear with temperature but it can be shown that in a typical dual-threshold CMOS process, the temperature coefficient of I_1 is negative with dominantly linear temperature dependence.

B. 5 MOSFETs LNTC Current

A 5 MOSFET LNTC current source is presented in this paragraph. The operation is similar to that of the 4 MOSFET structure, but it has different temperature characteristics. The circuit structure of the 5 MOSFET current source is shown in Figure 4. All transistors in this circuit have normal threshold voltages. Using the same functional form of the device models as was used in the previous section, it follows that,

$$I_{d1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_5 (V_1 - V_{t1})^2 \tag{14}$$

$$I_{d2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 (V_1 - V_2 - V_{t1})^2 \tag{15}$$

$$I_{d2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_7 (V_2 - V_{t1})^2 \tag{16}$$

Assuming the gain of the M8:M9 current mirror is 1, it follows that

$$I_{d1} = \frac{(V_{t1})^2 \frac{1}{2}\mu_n C_{ox}}{\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_3}}\right)^2} \tag{17}$$

Introducing the temperature dependence of the mobility and threshold voltage from (9) and (10) into (17), it follows that the current in the 5 MOSFET structure is

$$I_2 = I_{d1} = \left((V_{t0})_1^2 \times T^{\beta} + 2\times(V_{t0})_1 \times KT1 \times T^{\beta+1} + KT1 \times T^{\beta+2}\right) \times C_2 \tag{18}$$

where

$$C_2 = \frac{\frac{1}{2}\mu_0 \left(\frac{1}{T_0}\right)^{\beta} C_{ox}}{\left(\frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_3}}\right)^2} \tag{19}$$

It can also be shown that this current has a dominantly linear dependence on temperature with a negative temperature coefficient.

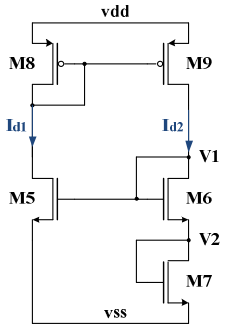

Figure 4. Circuit of 5 MOSFETs CTAT current source

C. Differential Current

In order to compare two current temperature characteristics, two LNTC current functions, (10) and (17) are rewrite as follows,

$$I_1 = p_1 \times T^{\beta} + p_2 \times T^{\beta+1} + p_3 \times T^{\beta+2} \tag{20}$$

$$I_2 = q_1 \times T^{\beta} + q_2 \times T^{\beta+1} + q_3 \times T^{\beta+2} \tag{21}$$

$$\begin{cases} p_1 = \Delta V_{t0}{}^2 \times C_1 \\ p_2 = 2\times \Delta V_{t0} \times \Delta KT1 \times C_1 \\ p_3 = \Delta KT1^2 \times C_1 \end{cases} \tag{22}$$

$$\begin{cases} q_1 = (V_{t0})_1^2 \times C_2 \\ q_2 = 2\times (V_{t0})_1 \times \Delta KT1 \times C_2 \\ q_3 = \Delta KT1^2 \times C_2 \end{cases} \tag{23}$$

From both current expressions of two structures (22) and (23), the fact can be observed that the ratios between the coefficients of T's exponent are design parameter independent. For example p_1/p_2 has no relationship with any transistor size in 4 MOSFETs structure. Hence two LNTC currents, I_1 and I_2 generated by the same structure have the relation that I_1/I_2 equals a constant. This gives the reason why two different types LNTC current generators are required. Only one type LNTC current source structure can't get an appropriate current level if they cancel each other's first order temperature dependency. From function (22) and (23), p_1/p_2 is independent with q_1/q_2 and p_1/p_3 is also independent with q_1/q_3. 4MOSFETs and 5MOSFETs structure are combined to get a useful constant current level with significant temperature dependency canceled.

In this work, the process used for current reference design has $\beta = -1.08$ which is closed to -1. Assume $p_1 >> p_3$ and $q_1 >> q_3$,

$$I_1 = p_1 \times T^{-1} + p_2 \tag{24}$$

$$I_2 = q_1 \times T^{-1} + q_2 \tag{25}$$

$$N = p_1 / q_1 \tag{26}$$

$$I_d = A\times(I_1 - I_2 \times N) = A\times(p_2 - \frac{p_1}{q_1}\times q_2) \tag{27}$$

In other process, β does not equal -1, Taylor expansion need be used to calculate the most significant temperature dependent coefficients. Further, scaling the two LNTC

currents and cancel most temperature dependency of two LNTC currents to get the differential current.

D. Proposed circuit

. The whole circuit is shown in the Figure 5. M1-M4 are 4MOSFETs LNTC current source and M5-M9 are 5 MOSFETs LNTC current source. The start-up current for 5 MOSFETs structure isn't shown but needed. From reference [3], it can be known that 4 MOSFETs structure doesn't need any start-up circuit to keep circuit always working normally. The ratios M10/M8 and M11/M2 can be sized to scale two LNTC currents. M10-M11 also compose a subtracter, which generates the difference current between M10 and M11 drain current. M13 is part of current mirror and shift the output current according to the working requirements from other circuits.

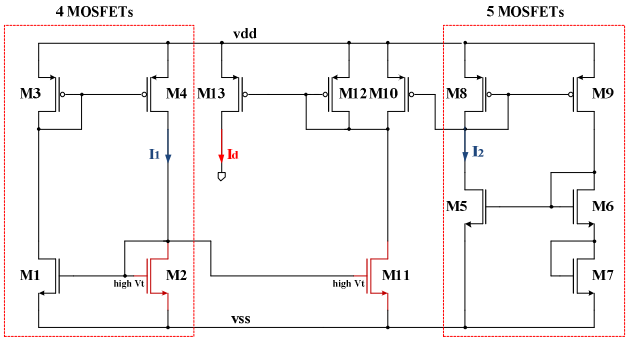

Figure 5. Proposed Circuit of Current Reference

IV. SIMULATION RESULTS

The proposed circuit is designed in a TSMC 0.18um process. Simulation is run in temperature range [-10℃ ~100℃]. The nominal supply voltage is 1.8V. The ratio N between the first order temperature coefficients of I_1 and I_2 is 1.1. The output current mirror gain A is 1. At the typical state, the simulation results is shwon in Figure 6. I_1 and I_2 are LNTC current and the differential current is 4.82μA and almost flat. The accuray is ±1.24% within 110℃ range.

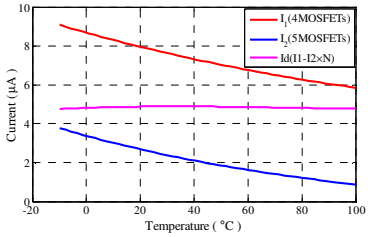

Figure 6. Two CTAT current and reference current at typical state

To varify the proposed circuit with process variation, at both corners, NMOS slow_PMOS slow and NMOS fast_PMOS fast, this circuit is also simulated and the results are shown in the Figure 7. In the same temperature range [-10℃ ~100℃], the output current in NMOS slow_PMOS slow corner is 4.02μA has ±4.16% variation. Current error in NMOS fast_PMOS fast is within ±3.42% and the current level is 5.57 μA.

To compare the proposed circuit with other works, the table1 shows the performance and circuit features. The current reference in this work doesn't include any resistor and Op Amp and gets a smaller current variation due to temperature change.

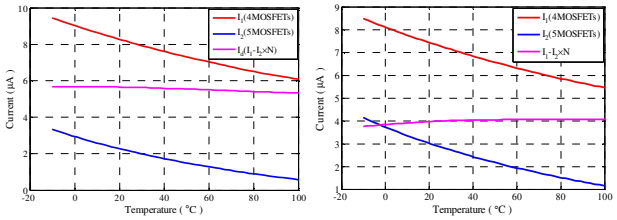

Figure 7. Proposed Circuit of Current Reference

TABLE I. COMPARISON WITH OTHER WORKS

Ref	Temperature Range	V_{dd}	Process	Feature	Current Level	Current Variation
[1]	-10℃ ~70℃	3V	0.35μm	b & c	1 μA	±7% (Sim)
[2]	-20℃ ~100℃	1V	0.18 μm	b&c	144 μA	±7%(Meas)
[5]	40℃ -150℃	1.5V	0.25 μm	b&c	5 μA	7%(Meas)
[6]	-20℃ -70℃	1.2V	1.5 μm	a	410pA	±10%(Meas)
This work	-10℃ -100℃	1.8V	0.18 μm	a	4.2 μA	±1.5% (Sim_typical) ±4.16% (Sim_worst corner)

a. All CMOS b. Resistor included c.Op amp included
Sim. Simulation Results Meas. Measurement Results

I. CONLCUSION

This paper presents a CMOS current reference without any on-chip resistor in TSMC 0.18μm with 1.8V power supply. The maximum power consumption cost by itself is only 72μW. Also this circuit is very compact with active area 85.42 μm^2. The output current variation due to temperature is ±1.24% at typical sate and less than ±4.16% over all process corners.

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