A Compact Model of MOSFET Mismatch for Circuit Design

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***Abstract*—This paper presents a compact model for MOS transistor mismatch. The mismatch model uses the carrier number fluctuation theory to account for the effects of local doping fluctuations along with an accurate and compact dc MOSFET model. The resulting matching model is valid for any operation condition, from weak to strong inversion, from the linear to the saturation region, and allows the assessment of mismatch from process and geometric parameters. Experimental results from a set of transistors integrated on a 0.35 μm technology confirm the accuracy of our mismatch model under various bias conditions.**

***Index Terms*—MOSFET, analog design, matching, mismatch, compact models.**

I. Introduction

IT IS widely recognized that the performance of most analog or even digital circuits is limited by MOS transistor mismatch [1]–[4]. In analog circuits, the spread in the dc characteristics due to doping statistics in the MOSFET channel results in inaccurate or even anomalous circuit behavior [5]. Also, for digital circuits, transistor mismatch leads to propagation delays whose spread can be of the order of several gate delays for deep-submicron technologies [5]. As predicted by Meindl [6], "variations will set the ultimate limits on scaling of MOSFETs." The shrinkage of the MOSFET dimensions and the reduction in the supply voltage make matching limitations even more important, to such an extent that several new studies have been published in recent years [7]–[10]. Existing mismatch models use either simple drain current models limited to a specific operating region [1], [2], [4], [9]–[11] or use complex expressions [8] like those of BSIM.

In general, however, the applicability of dc models to characterize mismatch is not questioned. It is widely accepted that matching can be modeled by the random variations in geometric, process, and/or device parameters, and the effect of these random parameters on the drain current is quantified using the transistor dc model. As pointed out in [9] and [10] and more recently in [12], there is a fundamental flaw in the current use of dc models for mismatch that results in inconsistent formulas. In effect, mismatch models implicitly assume that the actual values of the lumped model parameters can be obtained by integration of the position-dependent parameters distributed over the channel region of the device, e.g., for the threshold voltage V_T

$$V_T = \frac{1}{WL} \iint_{\text{channel-area}} V_T(x,y)\,dx\,dy \tag{1}$$

where W and L are the width and length of the transistor, respectively.

As analyzed in [9], [10], and [12], the application of (1) to series or parallel association of transistors leads to an inconsistent model of matching owing to the nonlinear nature of MOSFETs. Consequently, the simple consideration of random fluctuations in the lumped parameters of the dc current model is not appropriate for developing matching models, and new formulas need to be derived from the device physics.

The impact of local impurity fluctuation on MOSFET threshold voltage, which was first recognized in 1975 [13], is one of the main sources of mismatch in current MOS devices [12]–[16]. As MOSFETs are scaled down to the deep-submicron regime, the number of dopants in the depletion layer decreases, being on the order of only hundreds for minimum-size devices [17]. As an example, a minimum transistor in a 0.25-μm process contains about 1100 dopant atoms in the depletion layer while in a 0.1-μm process this number is only around 200 [5]. The relative spread in the number of dopant atoms in the depletion layer causes a spread in the threshold voltage, which increases with each new process generation [17]. Even though lightly doped double-gate MOSFETs [17], [18] avoid dopants and, consequently, the number fluctuation effects, single-gate doped MOSFETs are still the prevailing devices and will be for the coming years. Therefore, predicting the effects of random dopant number on MOSFET mismatch is of prime importance.

This paper deals mainly with the effects of random number of carriers due to impurity fluctuations. The conventional approach takes into account the dopant fluctuations over the entire channel, but here we consider explicitly the effects of local fluctuations. We integrate the contribution of the local fluctuations along the channel considering the main MOSFET nonlinearities. Fortunately, the formalism needed to include local fluctuations is already available in flicker or $1/f$ noise modeling, namely, carrier number fluctuation theory [19].

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Device mismatch and internal noise are accuracy-limiting factors for electronic circuits. Parallelism between their effects in electronic circuits has been previously reported [20] through a comparison between the limits on minimum power consumption, for a given speed and accuracy, imposed by mismatch and noise.

Mismatch (spatial fluctuation) and noise (temporal fluctuation) are similar phenomena, both depending on process, device dimensions, and bias. Put simply, mismatch can be seen as a "dc noise."

In this paper, we will show that the carrier number fluctuation theory, employed to derive $1/f$ transistor noise, can also be applied to model current matching in MOSFETs. In this way, we show the parallelism between noise and mismatch effects at the circuit level.

To obtain general results for all bias regions of the transistor, we have used the advanced compact MOSFET (ACM) model, a physics-based one-equation all-region model [21], [22]. The model presented here does not include the effects of mobility degradation, velocity saturation, and series resistances. The inclusion of such effects is certainly essential for a computer-implemented version of the model, but it leads to complicated expressions that are not suitable for discussion in this paper.

Section II reviews briefly the ACM MOSFET model. In Section III, we calculate the contribution of local fluctuation current to the total current mismatch. The effect of local fluctuations in impurities on the drain current mismatch is determined in Section IV. In Section V, we derive a compact expression that allows one to calculate current mismatch in terms of inversion level. In particular, very simple formulas are provided for analog designers to predict mismatch for any bias condition. In Section VI, we show experimental results that corroborate the compact mismatch model presented in previous sections. Finally, the conclusion is given in Section VII.

II. ACM Model

The fundamental approximation of the ACM model [21], [22] is the linear dependence of the inversion charge density Q'_I on the surface potential ϕ_S, which encompasses the weak, moderate, and strong inversion regions

$$dQ'_I = (C'_b + C'_{\rm ox})d\phi_S = nC'_{\rm ox}d\phi_S. \tag{2}$$

Here, n is the slope factor, slightly dependent on the gate voltage, and $C'_b, C'_{\rm ox}$ are the depletion and oxide capacitances per unit area. The drain current in a long-channel transistor is calculated with the aid of (2) and the charge-sheet approximation [23] and is given by

$$I_D = \frac{\mu W}{nC'_{\rm ox}}\left(-Q'_I + nC'_{\rm ox}\phi_t\right)\frac{dQ'_I}{dx} \tag{3}$$

where μ is the effective mobility, W is the channel width, ϕ_t is the thermal voltage, and x is the position along the channel length.

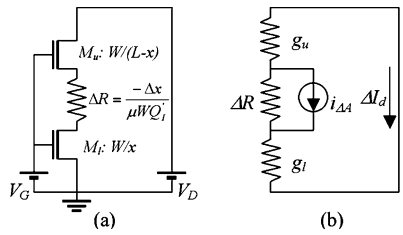

Fig. 1. Splitting of a transistor into three series elements: (a) transistor equivalent circuit and (b) small-signal equivalent circuit.

The other specificity of the ACM model is the use of the unified charge control model (UCCM) [24], which links the carrier charge density to the applied voltages according to

$$V_P - V_x = \phi_t\left[\frac{Q'_I}{Q'_{IP}} - 1 + \ln\left(\frac{Q'_I}{Q'_{IP}}\right)\right] \tag{4}$$

where $Q'_{IP} = -nC'_{\rm ox}\phi_t$, $V_P = (V_{\rm GB} - V_T)/n$ is the pinch-off voltage, and V_x is the channel potential at position x. As shown in [25], the use of (3) in conjunction with (4) gives

$$I_D = -\mu\frac{W}{dx}Q'_I(x)dV_x. \tag{5}$$

Consequently, the ACM model is fully consistent with the quasi-Fermi potential formulation for the drain current [23]. As will be shown next, (5) is essential for finding the relationship between current fluctuation and carrier fluctuation.

III. Consistent Model for Drain Current Fluctuation

The fluctuations of the drain current around its nominal value result from the sum of all the contributions from local fluctuations along the channel, whatever their origin. To calculate the effect of these fluctuations, we split the transistor into three series elements as shown in Fig. 1(a): an upper transistor, a lower transistor, and a small channel element of length Δx and area $\Delta A = W\Delta x$. In Fig. 1(a), x is the distance from the channel element to the source.

The local current fluctuation $(i_{\Delta A})$ is assumed to be a zero-mean stationary random process on the variable x. Small-signal analysis allows one to calculate the effect of $i_{\Delta A}$ on the drain current deviation (ΔI_d), as shown in Fig. 1(b). Noting that [21] $g_u = -\mu[W/(L-x)]Q'_{\rm Ix}$ and $g_l = -\mu(W/x)Q'_{\rm Ix}$, the current division between the channel element and the equivalent small-signal resistance of the rest of the channel gives $\Delta I_d = (\Delta x/L)i_{\Delta A}$. This very simple result for the current division, proportional to a geometric ratio, is a consequence of the quasi-Fermi potential formulation for the drain current, i.e., the conductance of the channel element and the transconductances of the upper and lower transistors are proportional to the local charge density [21]–[23]. Thus, the mean square of the total drain current fluctuation is

$$\overline{\Delta I_D^2} = \sum_{\text{channel-length}} \overline{(\Delta I_d)^2} = \lim_{\Delta x\to 0}\sum \overline{\left(\frac{\Delta x}{L}i_{\Delta A}\right)^2} = \frac{1}{L^2}\int_0^L \Delta x\overline{(i_{\Delta A})^2}dx \tag{6}$$

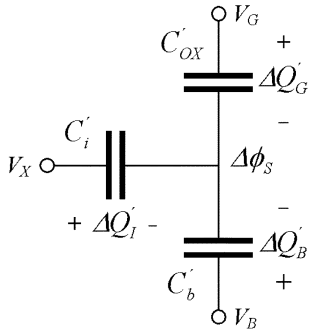

Fig. 2. Capacitive model of the MOSFET channel for matching analysis. Terminal voltages are constant.

since local current fluctuations along the channel are uncorrelated. Local current fluctuations arise from three independent physical origins, namely, fluctuations of channel doping, surface state density, and gate oxide thickness [14]. Note that, since $i_{\Delta A}$ is related to local fluctuation in the area $W\Delta x$, its variance must be proportional to $1/W\Delta x$. As in [14], we have assumed that fluctuation of channel doping is the main factor that determines local current fluctuations.

IV. Number Fluctuation Mismatch Model

The local current fluctuation that results from local fluctuations in the inversion charge density is calculated from (5) as in [28], [46], and [48], yielding

$$i_{\Delta A} = I_D \frac{\Delta Q'_I}{Q'_I} \tag{7}$$

where $\Delta Q'_I$ is the fluctuation of the inversion charge density in a channel element of area ΔA. For the sake of simplicity, we will consider only the fluctuations in the number of carriers, but the analysis can also be extended to include mobility fluctuation, as done in [28] for $1/f$ noise.

As in [14], we assume that fluctuations in the number of impurities is solely responsible for fluctuations in the number of carriers. To derive the fluctuation of the inversion charge density, we have used the capacitive MOS model of Fig. 2. Charge conservation in the structure of Fig. 2 requires that

$$\Delta Q'_B(x) + \Delta Q'_G(x) + \Delta Q'_I(x) = 0 \tag{8a}$$

where $\Delta Q'_G = -C'_{\rm ox}\Delta\phi_S$ and $\Delta Q'_I = -C'_i\Delta\phi_S$. The variation in the depletion charge is the sum of two components, the first equal to $-C'_b\Delta\phi_S$, associated with the fluctuation in the surface potential, and the second, designated by $\Delta Q'_{\rm IMP}$, and associated with the fluctuation in the number of ionized impurities. Therefore, the variation in the depletion charge is $\Delta Q'_B = -C'_b\Delta\phi_S + \Delta Q'_{\rm IMP}$.

The definitions of capacitances along with (8a) result in

$$\Delta Q'_I = -\frac{C'_i}{C'_i + C'_b + C'_{\rm ox}}\Delta Q'_{\rm IMP}. \tag{8b}$$

Recalling [21], [26] that $C'_i \cong -Q'_I/\phi_t$ and $C'_b = (n-1)C'_{\rm ox}$ under any bias condition, (8b) can be rewritten as

$$\Delta Q'_I = -\frac{Q'_I}{Q'_I - nC'_{\rm ox}\phi_t}\Delta Q'_{\rm IMP}. \tag{8c}$$

The local fluctuation in the number of impurities in an elementary slab of the depletion layer is calculated assuming it to be a random variable with Poisson distribution [11], [14]. The average number $(\overline{n_a})$ of dopants in the elementary volume of a depletion layer of length Δx [14] and depth Δy is

$$\overline{n_a} = N_a \Delta y W \Delta x \tag{9a}$$

where N_a is the net concentration of dopants (acceptors and donors) in the elementary volume of the depletion layer.

The square of the standard deviation of a random variable with Poisson distribution is equal to its average value, thus,

$$\sigma^2(n_a) = N_a \Delta y W \Delta x. \tag{9b}$$

Now, to calculate the standard deviation of $\Delta Q'_{\rm IMP}$, we proceed as in [16] and [47], which assume the individual contributions of the local deviations in the number of impurities to $\Delta Q'_{\rm IMP}$ to be uncorrelated, thus yielding

$$\sigma^2(\Delta Q'_{\rm IMP}) = \frac{q^2}{W\Delta x}\int_0^{y_d} N_a\left(1 - \frac{y}{y_d}\right)^2 dy \tag{9c}$$

where q is the electron charge, y is the distance to the semiconductor–oxide interface, and y_d is the depletion depth.

Using (7), (8c), and (9c), $(i_{\Delta A})^2$ can be calculated and, inserting the resulting value into (6), we obtain the expression for $\overline{\Delta I_D^2}$. With the aid of (3), the integration over the channel length in (6) is changed to the integration over the channel charge density given by

$$\sigma^2_{I_D} = \overline{\Delta I_D^2} = \frac{q^2\mu I_D}{nC'_{\rm ox}L^2}\int_{Q'_{IS}}^{Q'_{ID}} \frac{\int_0^{y_d} N_a\left(1 - \frac{y}{y_d}\right)^2 dy}{nC'_{\rm OX}\phi_t - Q'_I} dQ'_I \tag{10}$$

where Q'_{IS} and Q'_{ID} are the channel charge densities at the source and drain ends of the channel, respectively. Equation (10) allows computing current mismatch in terms of both the doping concentration along the depletion region and bias, which in this case is represented by the inversion charge densities at source and drain. The main difficulty in calculating the integral in (10) arises from the nonuniform doping profile and from the variation in the depletion depth along the channel. For a constant doping profile, we have verified that the introduction of a variable depletion depth along the channel is generally not relevant, except for very high inversion levels (under saturation, the impact of a variable depletion depth is less than 6% for an inversion level of 1000 in TSMC 0.35-μm technology).

In order to simplify the notation and derive simple expressions for mismatch, let us assume the integral in (9c) to be constant. From now on, we will use the notation

$$N_{oi} = \int_0^{y_d} N_a \left(1 - \frac{y}{y_d}\right)^2 dy. \tag{11}$$

where N_{oi} takes into account the influence of the vertical impurity profile on fluctuations in the depletion charge. We quote here the remarkable conclusion concerning (11) given by the authors of [47]. "Since the weight function $(1 - y/y_d)^2$ in (11) takes a steep maximum at $y = 0$, the removal of impurity near the surface should be effective for reducing the deviation." Thus, by adjusting the impurity distribution, mismatch reduction should be possible while keeping the target threshold voltage.

Finally, using (11) and integrating (10) from source to drain results in

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{q^2 N_{oi}\mu}{L^2 n C'_{\rm ox} I_D} \ln\left(\frac{nC'_{\rm ox}\phi_t - Q'_{IS}}{nC'_{\rm ox}\phi_t - Q'_{ID}}\right). \tag{12}$$

The result in (12) is essentially the same as that derived for flicker noise in MOS transistors in [25]. This is because mismatch behaves as a "dc noise" and the physical origin of both matching and noise is related to fluctuations in either fixed charges or localized states along the channel.

V. Mismatch Model in Terms of Inversion Level

An alternative expression for (12) which may be of great use to circuit designers is obtained if the charge density, at source and drain, is written in terms of the forward and reverse currents [21], [22], [27]. In the ACM model [21], [22], the drain current is expressed as the difference between the forward (I_F) and reverse (I_R) components

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D) = I_S(i_f - i_r) \tag{13}$$

where $I_S = (1/2)\mu C'_{\rm ox} n \phi_t^2 (W/L)$ is the specific current, which is proportional to the aspect ratio W/L of the transistor. V_G, V_S, and V_D are the gate, source, and drain voltages, with reference to the substrate. Parameters i_f and i_r are the normalized forward and reverse currents, or inversion levels at source and drain, respectively. Note that, in the saturation region, the drain current is almost independent of V_D; therefore, $i_f \gg i_r$ and $I_D \cong I_F$. On the other hand, if $V_{\rm DS}$ is low (linear region), then $i_f \cong i_r$. Using the relationship between inversion charge density and current [21], [22], $-Q'_{IS(D)}/nC'_{\rm ox}\phi_t = \sqrt{1 + i_{f(r)}} - 1$, and (13), (12) can be rewritten as

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{{\rm WLN}^{*2}} \frac{1}{i_f - i_r} \ln\left(\frac{1 + i_f}{1 + i_r}\right) \tag{14}$$

where we define N^* as in [25], [28]

$$N^* = \frac{-Q'_{IP}}{q} = \frac{nC'_{\rm ox}\phi_t}{q} \tag{15}$$

where Q'_{IP} is the channel charge density at pinch-off.

As is well known, (14) indicates that the ratio of mismatch power to dc power is inversely proportional to the gate area. In strong inversion, considering $n = 1$, (14) reduces to [12, eq. (12)]. Moreover, the ratio of mismatch power to dc power is proportional to $t^2_{\rm ox}$ and to $N_a^{1/2}$. Finally, the substrate voltage also affects the factor N_{oi} through modulation of the depletion depth. For fixed i_f and i_r, reverse substrate-to-source voltages increase the depletion depth and, consequently, N_{oi}. As a result, matching worsens for a reverse biased bulk-to-source junction.

Equation (14) can be simplified under specific conditions. From weak to strong inversion in the linear region, $i_f \cong i_r$ and (14) reduces to

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{{\rm WLN}^{*2}} \frac{1}{1 + i_f}. \tag{16a}$$

Equation (16a) can also be written as

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{{\rm WLN}^{*2}} \left(n\phi_t \frac{g_m}{I_D}\right)^2. \tag{16b}$$

In weak inversion, $i_f \ll 1$; thus, the first-order series expansion of (14) leads to

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{{\rm WLN}^{*2}} \tag{17}$$

for either saturation or nonsaturation.

In saturation, $i_r \to 0$; thus, expression (14) can be written as

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{{\rm WLN}^{*2}} \frac{\ln(1 + i_f)}{i_f}. \tag{18a}$$

Equation (18a) can also be written as

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{{\rm WLN}^{*2}} \frac{\ln(1 + I_D/I_S)}{I_D/I_S}. \tag{18b}$$

For the sake of completeness, one can include the random errors due to the specific sheet current $I_{\rm SQ} = (1/2)\,\mu C'_{\rm ox} n \phi_t^2$ as in [1], which results in a modification of (14), yielding

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{1}{WL}\left[\frac{N_{oi}}{N^{*2}} \frac{1}{i_f - i_r} \ln\left(\frac{1 + i_f}{1 + i_r}\right) + B^2_{I_{\rm SQ}}\right]. \tag{19}$$

In (19), $B_{I_{SQ}}$ is a mismatch factor that, to a first order, is a constant factor that accounts for variations in mobility, gate oxide thickness, and slope factor. A more elaborate model would consider $B_{I_{SQ}}$ as a bias-dependent term.

VI. Measurements

Intradie current mismatch of a set of NMOS and PMOS transistors was measured on a test circuit fabricated with the TSMC 0.35-μm 3.3-V CMOS n-well process. This process presents a gate oxide thickness of 78 Å. In the test circuit, transistors are arranged in arrays of 20 identical functional devices terminated by dummy ones to ensure uniform boundary conditions for all the transistors. Matched transistors have the same orientation. Transistor dimensions $(W \times L)$ of each array are 12 μm $\times$ 8 μm (*large*),

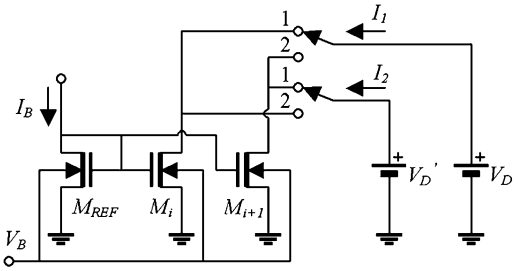

Fig. 3. Test circuit: $M_{\rm REF}$ is the reference transistor while M_i and M_{i+1} are the transistors under test. $I_B(V_B, V_D' = V_D)$ is a current (voltage) source.

3 μm $\times$ 2 μm (*medium*), 0.75 μm $\times$ 8 μm (*narrow*—minimum width), 12 μm $\times$ 0.5 μm (*short*—minimum length), and 0.75 μm $\times$ 0.5 μm (*small*—minimum size). Wide metal connections and multiple contact windows were employed in the layout to lower ohmic drops [29]. All of the ten packaged dies out of forty that were characterized showed similar mismatch behavior.

The circuit shown in Fig. 3 was used for measuring current mismatch. $V_D, V_D'(= V_D)$, and V_B are voltage sources and I_B is the bias current for the reference transistor $M_{\rm REF}$. Source/monitor units (SMUs) of the semiconductor parameter analyzer HP4145B were employed in the test setup. The same $M_{\rm REF}$ was used for all measurements while the remaining 19 transistors were measured in pairs of adjacent devices, M_i and M_{i+1} $(i = 1, \ldots, 18)$, for data acquisition. The differential technique was applied [30] to each pair of adjacent devices, as this test condition is used to highlight local, rather than global, mismatch effects.

Transistor pairs M_i and $M_{i+1}, i = 1, \ldots, 18$, were sequentially characterized, with the currents of both transistors (I_1 and I_2) being measured simultaneously for each bias condition with the switches in either position 1 or 2. The dc current flowing in each device, $I_{D(i)}$ or $I_{D(i+1)}$, was taken as the average value of the two currents measured for each transistor. This procedure minimizes any error that may result from mismatch between the two SMUs.

Normalized mismatch for each array is then calculated using the following expression:

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{1}{2(N-1)\overline{I_D}^2} \sum_{i=1}^{N} \left(I_{D(i)} - I_{D(i+1)}\right)^2 \tag{20}$$

where N is the total number of pairs in each group of identical transistors ($N = 18$ for our test structures). The factor 2 in the denominator of (20) was necessary to convert the variance of a differentially measured parameter into the variance of a single parameter [30], [31].

Figs. 4–7 present the mismatch power normalized to the dc power for drain-to-source voltage ranging from $+(-)10$ mV (linear region) to $+(-)2$ V (saturation) for the NMOS (PMOS) devices. Mismatch was measured for six different inversion levels (0.01, 0.1, 1, 10, 100, and 1000), for the *large* and *medium* device arrays. The bulk-source voltage was kept at zero volts. Simulated (model) curves were determined from

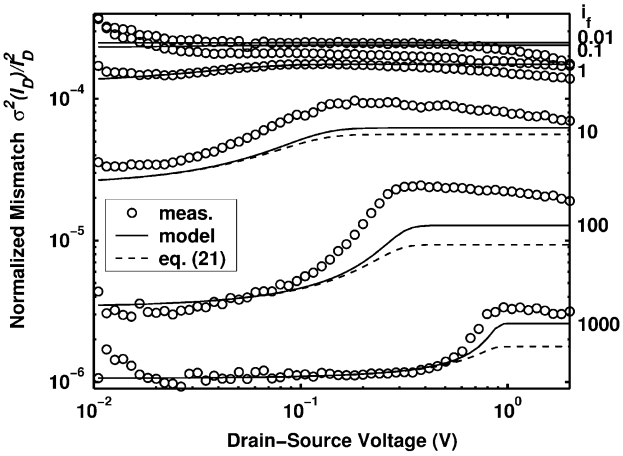

Fig. 4. Normalized current mismatch power for the *large* NMOS transistor array. Bulk-source voltage was kept at 0 V.

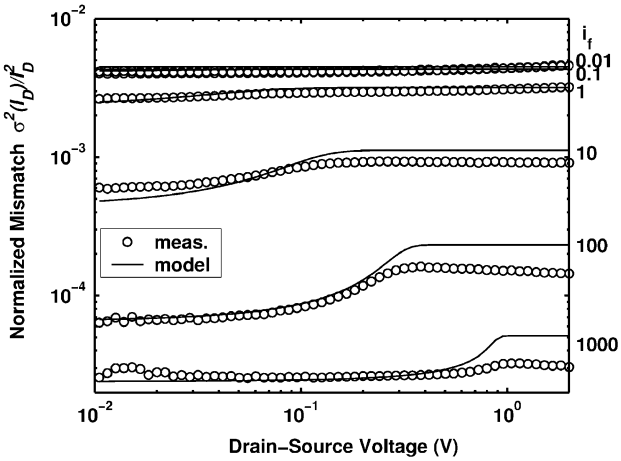

Fig. 5. Normalized current mismatch power for the *medium* NMOS transistor array. Bulk-source voltage was kept at 0 V.

(19), with i_r calculated through the long-channel ACM model [21], [22].

In weak inversion ($i_f = 0.01$ and 0.1), mismatch is almost constant from the linear to saturation regions and independent of the inversion level, as predicted by (17). Measured and simulated curves for weak inversion are almost coincident, being hardly distinguishable.

From moderate ($i_f = 1$ and 10) to strong ($i_f = 100$) inversion, both the simulated and measured curves present similar behavior, increasing from the linear region to saturation, where a plateau is reached. Differences between measured and simulated curves at saturation, which are more intense in the *medium* than in the *large* devices, may be associated with statistical spatial-nonuniformity concentration of dopant atoms [32].

Parameter N_{oi} was estimated from measurements in weak inversion, using (17). Effective transistor width and length ($W_{\rm eff}$ and $L_{\rm eff}$) were calculated [33] with the help of BSIM parameters *WINT* and *LINT* (0.065 μm and 0.075 μm, respectively) [34]. N^* was calculated based on parameters provided by MOSIS. The same value of $N_{oi}, 1.8\times10^{12}$ cm^{-2}, for the NMOS devices, and 7×10^{12} cm^{-2} for the PMOS devices was obtained for both the *large* and *medium* transistors.

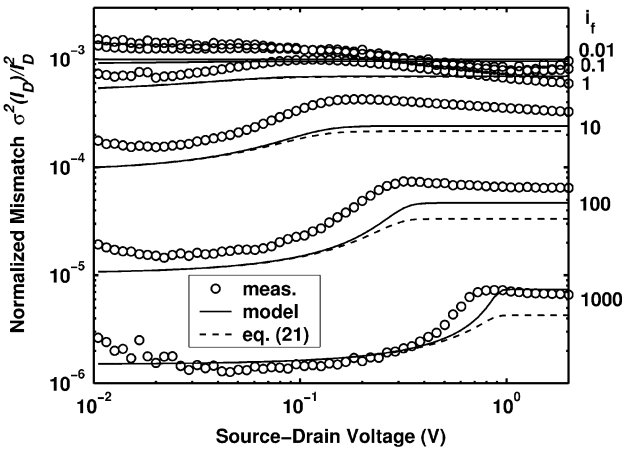

Fig. 6. Normalized current mismatch power for the *large* PMOS transistor array. Bulk-source voltage was kept at 0 V.

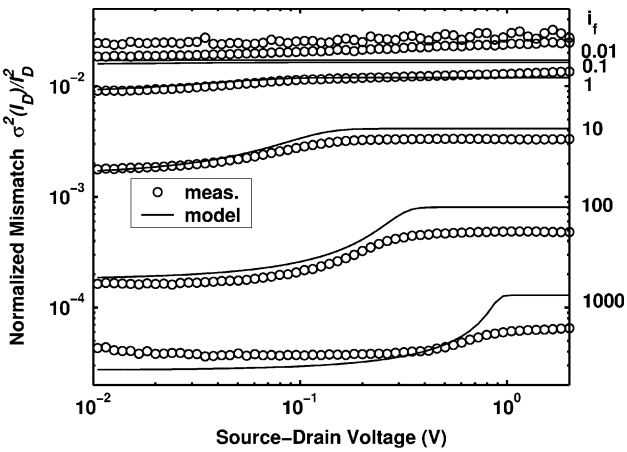

Fig. 7. Normalized current mismatch power for the *medium* PMOS transistor array. Bulk-source voltage was kept at 0 V.

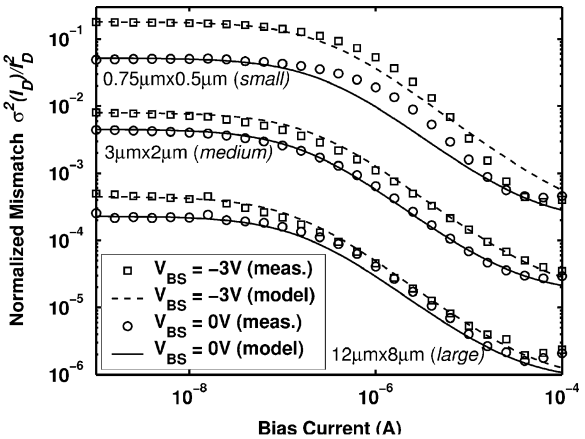

Fig. 8. Dependence of current matching on inversion level in the linear region for the *large*, *medium*, and *small* NMOS transistor arrays at two bulk bias voltages.

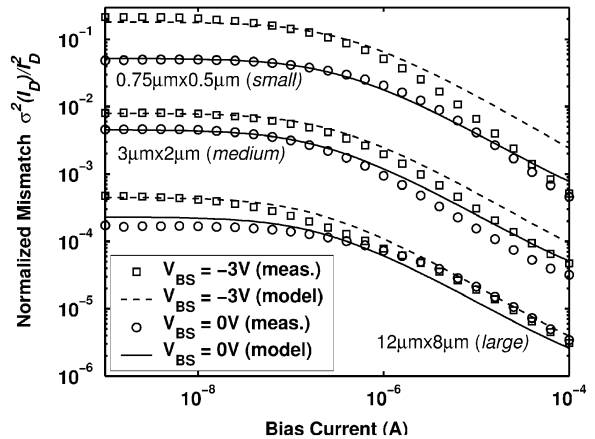

Fig. 9. Dependence of current matching on inversion level in saturation for the *large*, *medium*, and *small* NMOS transistor arrays at two bulk bias voltages.

It should be noted that N_{oi} includes both the acceptor and donor impurities [31]. As a consequence, N_{oi} is usually higher than the product of the net ion concentration and the depletion layer depth.

At a sufficiently high inversion level, the mismatch component of (19) associated with N_{oi} is of the same order of the contribution associated with $B_{I_{SQ}}$, a mismatch parameter that accounts for variations of mobility, gate oxide thickness, and slope factor. Therefore, for higher inversion levels, mismatch remains constant at a minimum determined by $B_{I_{SQ}}$, as can be noted, for example, in Fig. 8, which shows current mismatch for the linear region. As can be observed from the measurements, the ratio of the minimum mismatch at high inversion levels to the maximum mismatch measured in weak inversion, is the same for both the *medium* and *large* arrays.

Parameter $B_{I_{SQ}}$ was estimated from measurements in strong inversion and linear region, using (19). $B_{I_{SQ}}$ of the order of 0.89%-μm and 0.71%-μm resulted for NMOS and PMOS devices, respectively, for both the *large* and the *medium* devices. Simulated curves presented in Figs. 4–7 are based on the values extracted for both N_{oi} and $B_{I_{SQ}}$, for either NMOS or PMOS transistors.

Some authors [8] suggest that PMOS devices show better matching than NMOS devices or vice versa [3]. Our results, however, indicate that matching depends on process details, such as doping patterns (e.g., halo implant, twin-well, surface implant adjustment, and retrograde implant). As can be seen from the results, for NMOS and PMOS devices with the same geometry, inversion level, and drain voltage, PMOS (in compensated N-well) present higher mismatch than NMOS transistors. Other authors have found that PMOS show greater mismatch than NMOS devices [35], [36], while some have found the contrary [12]. We conclude that there is not a simple "rule of thumb" regarding which type of MOS transistor is better matched.

Figs. 8 and 9 show the measured and simulated dependence of current matching on inversion level for the linear and saturation regions, for three sizes of NMOS transistors, at two bulk bias voltages ($V_{\rm BS}$). From these figures, one can see that larger transistors follow the "area rule", as shown in our model. For a particular bulk bias, we used the same N_{oi} for modeling the matching of both the *large* and *medium* transistors, in the linear and saturation regions. We also used the same $B_{I_{SQ}}$ value for modeling the matching of both the *large* and *medium* devices under any bulk bias. The *small* transistors do not follow this rule,

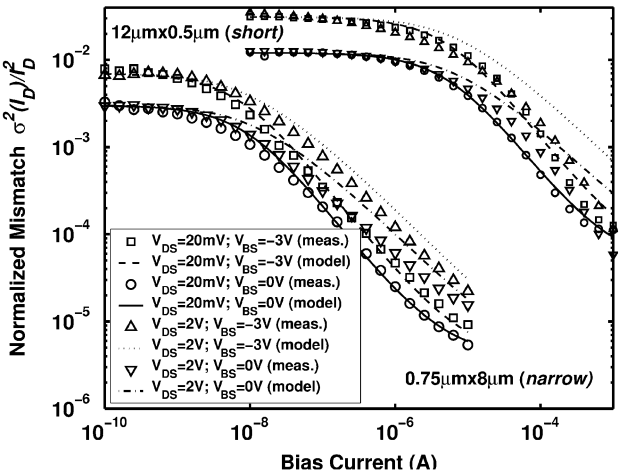

Fig. 10. Dependence of current matching on inversion level in the linear and saturation regions for the *short* and *narrow* NMOS transistor arrays at two bulk bias voltages.

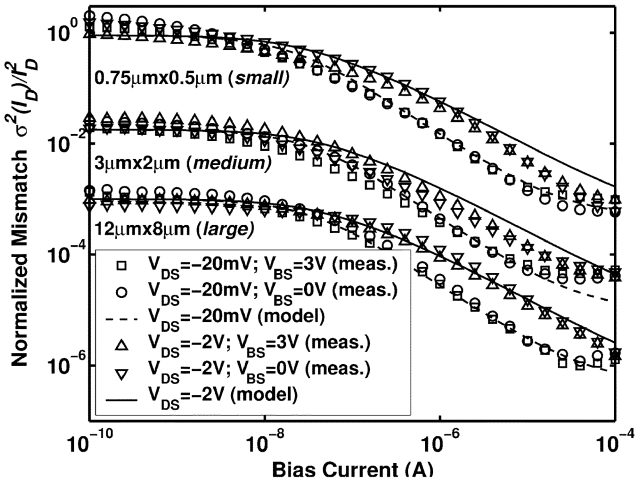

Fig. 11. Dependence of current matching on inversion level in the linear and saturation regions for the *large*, *medium*, and *small* PMOS transistor arrays at two bulk bias voltages.

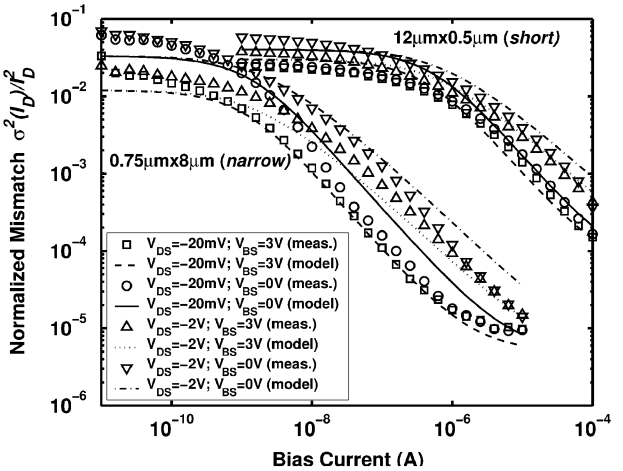

Fig. 12. Dependence of current matching on inversion level in the linear and saturation regions for the *short* and *narrow* PMOS transistor arrays at two bulk bias voltages.

presenting a mismatch 55% lower than the model estimates (at zero volt bulk bias) using the same N_{oi}. At $V_{\rm BS} = -3$ V, the mismatch measured for the *small* transistors is in good agreement with the value estimated by our model. However, values of N_{oi} for the *small* transistors different from those measured for the *large* transistors were chosen in order to obtain better fitting of the curves. For the dies we characterized, *small* transistors presented an unpredictable N_{oi}, as previously observed in [37] and [38]. Indeed, electrical characteristics of short-channel devices are very sensitive to fluctuations due to a greater dependence on edge effects. This high sensitivity of short-channel devices is one of the main reasons for the difficulties found in modeling mismatch, mainly in today's very complex submicron technologies. Also, for minimum length devices, drain and source doped regions are very close to each other, affecting strongly the shape of the depletion layer below the channel. For the *small* transistors $B_{I_{SQ}}$ was calculated in the same proportion that results from the N_{oi} used for this transistor to the N_{oi} of the *medium/large* sizes. As experimental data demonstrated, the model we developed for mismatch can also be used for short-channel transistors, even though fitting of both N_{oi} and $B_{I_{SQ}}$ is required. A good approach for modeling mismatch in short-channel transistors would be to define a range of "maximum–minimum" values for N_{oi} [39]. In a conservative design, the maximum value of N_{oi} would be chosen to predict the worst case mismatch.

From Figs. 8–12, one can also see that current mismatch increases for reverse bulk bias. The reason for this behavior is that, compared to the zero bulk bias, a reverse bulk voltage deepens the depletion layer, resulting in a higher N_{oi} [4], [40]–[42]. Owing to the difficulty in developing a model for the modulation of N_{oi} with bulk bias, we decided to choose values of N_{oi} that fit the measured data for each bulk bias condition.

Fig. 10 shows current mismatch for the *narrow* and for the *short* NMOS transistor arrays. We observed that our mismatch model is applicable to both minimum length and minimum width devices, showing good agreement with measured data.

Figs. 11 and 12 present a comparison of the results from the measurements and the model for PMOS devices. For these devices, bulk bias has a lesser impact on mismatch than for NMOS devices. The measured data show good agreement with the "area rule," except, again, for the *small* devices. The N_{oi} used for the fitting of the curve for *small* devices is 80% higher than the value estimated for larger PMOS devices. From the measurements taken on devices fabricated in the 0.35-μm technology, we can observe that, for equivalent size and bias, PMOS exhibit higher mismatch than NMOS devices.

Besides fluctuation of dopant atoms in the channel, gate dopant fluctuation and geometrical variations are also relevant mismatch factors [2], [15], [16], [42], [43]. Many authors have shown from experiments that the first factor is the dominant factor for threshold voltage (V_T) mismatch (resulting in current mismatch), the second being also very relevant for submicron processes, and the third being the least relevant in general. As can be seen, other sources of mismatch can be included in our model to improve its accuracy but, for the moment, we have tried to keep it as simple as possible.

Experimental results from another CMOS technology that were recently published [44], [45] also corroborate the mismatch model developed in this work.

VII. Summary and Conclusion

In this paper, we developed a mismatch model for the MOS transistor, continuous in all operating regions and consistent with the series-parallel association of devices. The approach we proposed for mismatch modeling is based on the integration of the random number of carriers along the channel. This approach along with the description of the ACM dc model resulted in a compact easy-to-use formula for mismatch that covers all operating regions. The results we obtained for mismatch are closely related to those derived in [25] for $1/f$ noise, since the physical mechanisms at the origin of both phenomena are similar. We conclude from our model that fluctuations in lumped parameters such as the threshold voltage are not appropriate for describing mismatch owing to the nonlinear distribution of carriers along the transistor channel. We have shown how to include the random fluctuations of both dopant atoms and sheet specific current in the mismatch model. A set of arrays of identical transistors was manufactured in a 0.35-μm CMOS technology from TSMC to assess the influence of bias and geometry on current mismatch. Experimental results confirmed the accuracy of our model under a wide range of geometries and bias conditions, including different bulk bias voltages. For the technology under analysis, we concluded that the dominant factor for mismatch is N_{oi}, the average number of dopants per unit area in the depletion layer below the channel. We expect this work to shed new light on mismatch modeling and help circuit designers predict transistor mismatch accurately from a pair of parameters (N_{oi} and $B_{I_{SQ}}$).

Appendix

Using Pelgrom's mismatch model [2] together with the ACM model [21], [22], the expression derived for the normalized mismatch power is

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{A^2_{\mathrm{VT}}}{WL}\left(\frac{g_m}{I_D}\right)^2 = \frac{N_{oi}}{WLN^{*2}}\left(\frac{2}{\sqrt{1+i_f}+\sqrt{1+i_r}}\right)^2 \tag{21}$$

where the dependence of the normalized mismatch power on i_f is the same as that of $(g_m/I_D)^2$ on i_f. Both expressions (14) and (21) tend to (17) in weak inversion ($i_f \ll 1$), both being almost insensitive to the current. But in strong inversion and saturation ($i_f \gg 1, i_r \to 0$) they diverge. For example, when $i_f = 1000$ and $i_r = 0$, (14) predicts a value 80% greater than (21). The explanation for this difference is the distributed nature of the MOSFET. While Pelgrom's model assumes a lumped V_T for the MOSFET, our model assumes a distributed V_T along the channel. As a consequence, for strong inversion and saturation, the part of the channel closer to the drain plays a less important role in the charge fluctuation along the channel than the part of the channel closer to the source. Figs. 4 and 6 present plots of (21) for comparison between Pelgrom's model and ours.

Even though Pelgrom's model used in conjunction with the ACM expression for g_m/I_D gives a good estimation of mismatch in saturation for not too high inversion levels, it is not consistent for modeling the series associations of transistors, as pointed out in [9], [10], and [12].

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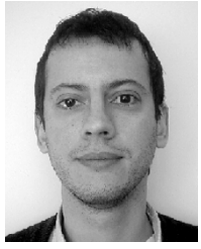

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