A Compact Power-Efficient 3 V CMOS Rail-to-Rail Input/Output Operational Amplifier for VLSI Cell Libraries

Ron Hogervorst, John P. Tero, Ruud G. H. Eschauzier, and Johan H. Huijsing

Abstract— **This paper presents a two-stage, compact, power-efficient 3 V CMOS operational amplifier with rail-to-rail input and output ranges. Because of its small die area of 0.04 mm^2, it is very suitable as a VLSI library cell. The floating class-AB control is shifted into the summing circuit, which results in a noise and offset of the amplifier which are comparable to that of a three stage amplifier. A floating current source biases the combined summing circuit and the class-AB control. This current source has the same structure as the class-AB control which provides a power-supply-independent quiescent current. Using the compact architecture, a 2.6 MHz amplifier with Miller compensation and a 6.4 MHz amplifier with cascoded-Miller compensation has been realized. The opamps have, respectively, a bandwidth-to-supply-power ratio of 4 MHz/mW and 11 MHz/mW for a capacitive load of 10 pF.**

I. Introduction

THE design of low-cost mixed/mode VLSI systems requires compact, power-efficient library cells. Digital library cells fully benefit from the continuing down-scaling of CMOS processes as well as from the ongoing reduction of the supply voltage. The down-scaling of processes results in smaller digital cells, because these cells can be designed using minimum-length components. The power consumption of digital cells is reduced by using a lower supply voltage [1]. In contrast to digital cells, analog library cells, such as the operational amplifier, cannot be designed using minimum-length components, for reasons of gain, offset etc. Furthermore, a lower supply voltage does not necessarily decrease the dissipation of the cell because it often leads to more complex designs, resulting in a larger quiescent current. To obtain compact, low-voltage, power-efficient analog cells, simple library cells with good performance need to be developed.

A two-stage opamp is very suitable to obtain a compact design. Published two-stage rail-to-rail opamps, however, contain complex class-AB output stages, which use large die area [2], [3]. Moreover, the class-AB control contributes significantly to the noise and offset of the amplifier. Very recently, an operational amplifier which overcomes the aforementioned problems has been described in [4]. This amplifier, however, uses a complex floating current source to bias the summing circuit and the class-AB control. The transconductance of the input stage varies strongly with the common-mode input voltage, which impedes an optimal frequency compensation. Moreover, the quiescent current in the output transistors depends on supply voltage variations.

In this paper a compact, two-stage, 3 V CMOS opamp with rail-to-rail input and output ranges will be presented. Because of its small die area, it is very suitable as a VLSI library cell. The opamp contains a constant-g_m rail-to-rail input stage and a simple class-AB output stage. To save die area, the class-AB driver circuit has been incorporated in the folded-cascoded summing circuit of the rail-to-rail input stage. The floating architecture of the class-AB driver prevents that it contributes to the noise and offset of the amplifier. This makes the input offset and noise of the amplifier comparable to those of a three-stage amplifier. The combined summing circuit and class-AB control is biased by a simple floating current source which has the same structure as the class-AB control, resulting in a quiescent current which is independent of the supply voltage.

Using the compact opamp, two designs with different types of frequency compensation have been realized. The first opamp is compensated using the well-known Miller splitting technique [5], resulting in a unity-gain frequency of 2.6 MHz. The second opamp is compensated by inserting the folded-cascode of the summing circuit in the Miller loop, which increases the unity-gain frequency up to 6.4 MHz. The compact design of the opamps provides a low-power consumption of 0.5 mW at a 3 V supply voltage. Both opamps occupy 0.04 mm^2.

The constant-g_m rail-to-rail input stage and class-AB driver circuit are described in Section II and Section III, respectively. Section IV describes the topology of the compact opamp. The overall design and the frequency compensation are described in Section V. The realizations and measurement results are discussed in Section VI. Finally, some conclusions are drawn in Section VII.

II. Constant-GM Rail-to-Rail Input Stage

In order to obtain a reasonable signal-to-noise ratio in low-voltage design, the input stage should be able to deal with common-mode input voltages from rail-to-rail. This can be achieved by placing an N-channel and a P-channel differential input pair in parallel, as is shown in Fig. 1 [5]. The N-channel input pair, $M_1 - M_2$, is able to reach the positive supply rail while the P-channel input pair, $M_3 - M_4$, is able to reach

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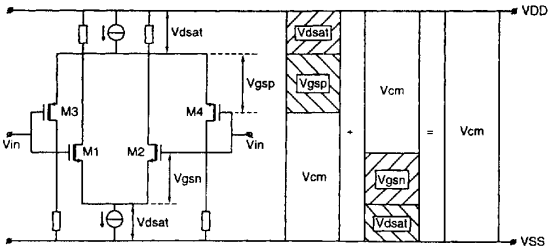


Fig. 1. Common-mode input range of the rail-to-rail input stage. The supply voltage is larger than $V_{\rm gsp} + V_{\rm gsn} + 2V_{\rm dsat}$.

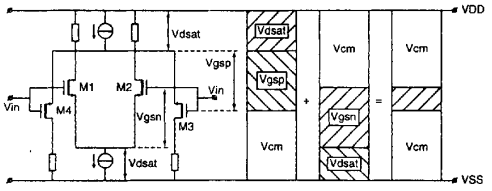


Fig. 2. Common-mode input range of the rail-to-rail input stage. The supply voltage is smaller than $V_{\rm gsp} + V_{\rm gsn} + 2V_{\rm dsat}$.

the negative supply rail. This input stage requires a supply voltage of at least:

$$V_{\rm sup,min} = V_{\rm gsp} + V_{\rm gsn} + 2V_{\rm dsat} \qquad (1)$$

where $V_{\rm gsn}$ and $V_{\rm gsp}$ are the gate-source voltage of an N-channel and the gate-source voltage of a P-channel transistor, respectively. $V_{\rm dsat}$ is the voltage across a current source which is necessary to ensure that it operates as a current source. If the supply voltage is below $V_{\rm sup,min}$ the input stage ceases to operate in the middle of the common-mode input range, as is shown in Fig. 2.

A drawback of the rail-to-rail input stage is that its g_m varies by a factor of two over the common-mode input range, as shown in Fig. 3. This large variation of the g_m impedes an optimal frequency compensation [5]. An optimal frequency compensation requires a constant g_m of the input stage. In order to obtain a constant g_m over the common-mode input range, the g_m at the lower and upper part of the common-mode input range has to be increased by a factor of two. Since the g_m of a MOS transistor operating in strong inversion is proportional to the square-root of its drain current, the tail-current of the actual active input pair could be increased by a factor of four.

This principle is realized in the circuit as shown in Fig. 4 [6]. The g_m-control is implemented by means of two current switches, M_5 and M_8, and two current mirrors, $M_6 - M_7$ and $M_9 - M_{10}$, each with a gain of three. The principles of the g_m-control can be best understood by dividing the common-mode input range into three parts.

If low common-mode input voltages are applied, i.e., voltages between $V_{\rm SS}$ and $V_{\rm SS} + 1$ V, only the P-channel input pair operates. The N-channel current switch conducts while the P-channel one is off. The N-channel current switch takes away the current $I_{\rm ref1}$ and directs it to the current mirror, $M_6 - M_7$, where it is multiplied by a factor three and added to $I_{\rm ref2}$. Since $I_{\rm ref1}$ and $I_{\rm ref2}$ are equal, the tail-current of the P-channel input equals $4I_{\rm ref}$.

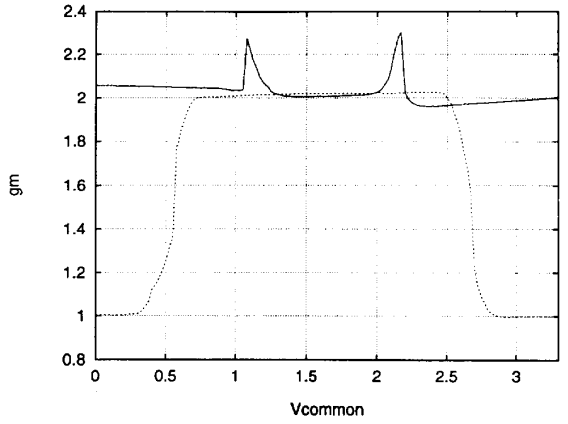


Fig. 3. Normalized g_m versus the common-mode inputvoltage for:
- - - - - Rail-to-rail input stage;
——— Rail-to-rail input stage with three-times current mirrors.

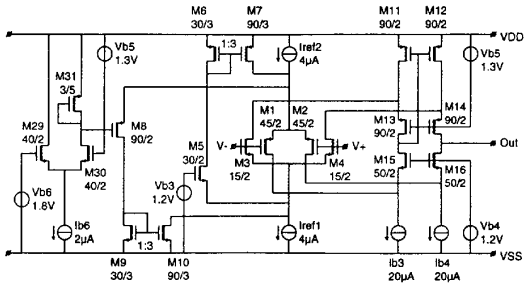


Fig. 4. Rail-to-rail input stage with g_m-control by three-times current mirrors.

If intermediate common-mode input voltages are applied, i.e., voltages between $V_{\rm SS}$ + 1.3 V and $V_{\rm DD}$ − 1.3 V, the P-channel as well as the N-channel input pair operate. Now, both current switches are off. The result is that the tail currents of the N-channel input pair and that of the P-channel input pair are equal to $I_{\rm ref}$.

If high common-mode input voltages are applied, i.e., voltages between $V_{\rm DD}$ −1 V and $V_{\rm DD}$, only the N-channel input pair operates. The P-channel current switch conducts while the N-channel current switch is off. The P-channel current switch takes away the current $I_{\rm ref2}$ and feeds it into the current mirror, $M_9 - M_{10}$, where it is multiplied by a factor 3 and added to the current $I_{\rm ref1}$. The result is that the tail-current of the N-channel input pair equals $4I_{\rm ref}$.

It can be calculated that for each part of the common-mode input range the g_m is given by:

$$g_m = \sqrt{KI_{\rm ref}}$$
$$\text{with } K = \mu_p C_{\rm ox}\left(\frac{W}{L}\right)_p = \mu_N C_{\rm ox}\left(\frac{W}{L}\right)_N \qquad (2)$$

where μ is the mobility of the charge carriers, $C_{\rm ox}$ is the normalized oxide capacitance, W and L are the width and the length of a transistor, respectively. The subscripts N and P refer to an N-channel or P-channel input transistor, respectively.

From (2) it can be observed that for a constant g_m the W over L ratios of the P-channel and the N-channel input pair have to obey the following relation:

$$\frac{\mu_N}{\mu_P} = \frac{\left(\frac{W}{L}\right)_P}{\left(\frac{W}{L}\right)_N} \tag{3}$$

If the ratio μ_N over μ_P differs from its nominal value because of process variations, the g_m will have an additional variation. For example if μ_N over μ_P changes about 15%, the additional variation will be approximately 7.5%.

It can be concluded that the g_m is approximately constant over the common-mode input range except for two take-over ranges, i.e., common-mode input voltages between V_{SS} + 1 V and V_{SS} + 1.3 V and common-mode input voltages between V_{DD} − 1.3 V and V_{DD} − 1 V, where the g_m varies only 15%, as is shown in Fig. 3. In the take-over ranges the current through one of the current switches changes from 0 to I_{ref}, or vice versa.

The offset of the rail-to-rail input stage changes over the common-mode input range because the N-channel input pair and the P-channel input pair have, in general, a different offset. This change in offset limits the CMRR of the input stage, since it is defined as the change of offset relative to the change in common-mode input voltage. To maximize the CMRR the change of offset should be spread out over a large part of the common-mode input range. In this circuit, the change of offset is spread out over the two take-over ranges of the current-switches. This allows a relatively large CMMR for these types of input stages.

At supply voltages below 2.9 V both current switches might conduct at the same common-mode input voltage. To prevent the positive feedback loop, $M_5 - M_{10}$, from becoming active, $M_{29} - M_{31}$ are added to the circuit. Each side of the differential pair, $M_{29} - M_{30}$, is connected via a voltage source, V_{b5} or V_{b6}, to either one of the supply-rails. The differential pair, $M_{29} - M_{30}$ measures the supply voltage. If the supply voltage is larger than 2.9 V the gate-voltage of the current switch, M_8, is biased by M_{31}. At supply voltages lower than 2.9 V, the differential pair gradually turns off M_8. Thus, the gate-voltage of the N-channel current switch moves towards the positive supply rail. This means that the current switch is always off at supply voltages below 2.9 V. In this way the positive feedback loop can never become active.

The current mirror, $M_{11} - M_{14}$, together with the folded cascodes, $M_{15} - M_{16}$, form a summing circuit. This summing circuit adds the signals coming from the complementary rail-to-rail input stage.

III. Rail-to-Rail Class-AB Output Stage

To make efficient use of the supply voltage and supply-current, an opamp requires class-AB biased output transistors connected in a common-source configuration. Moreover, the class-AB control should be compact to efficiently use die area.

The compact class-AB output stage is shown in Fig. 5 [7]. It consists of two common-source connected output transistors, M_{25} and M_{26}, which are directly driven by two in-phase signal currents, I_{in1} and I_{in2}. The floating class-AB control is formed by M_{19} and M_{20}. The stacked diode-connected transistors,

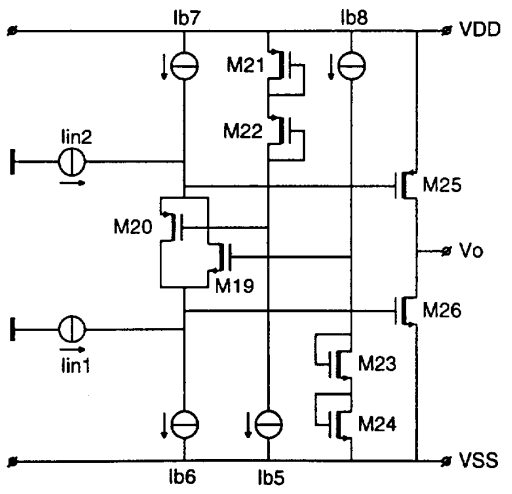


Fig. 5. Rail-to-rail output stage with floating class-AB control.

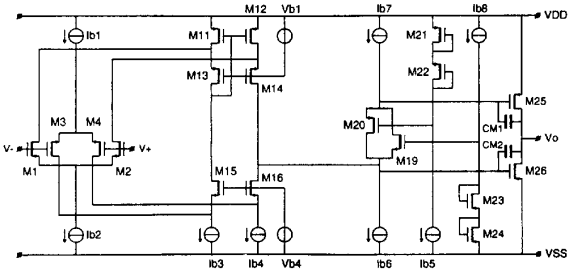


Fig. 6. Two-stage cascaded operational amplifier.

$M_{23} - M_{24}$ and $M_{21} - M_{22}$, bias the gates of the class-AB transistors M_{19} and M_{20}, respectively. As was shown in the previous section the minimum required supply voltage is limited by the demand for a fully rail-to-rail common-mode input range. Therefore, two stacked gate-source voltages are allowed in the class-AB output stage.

The floating class-AB control transistors, the stacked diode-connected transistors and the output transistors set up two translinear loops M_{20}, M_{21}, M_{22}, M_{25} and M_{19}, M_{23}, M_{24}, M_{26}, which determine the quiescent current in the output transistors. The class-AB action is performed by keeping the voltage between the gates of the output transistors constant. Suppose the in-phase signal current sources, I_{in1} and I_{in2}, are pushed into the class-AB output stage. As a result, the current of the P-channel class-AB transistor, M_{20}, increases while the current in the N-channel class-AB transistors, M_{19}, decreases by the same amount. Consequently, the gate-voltages of both the output transistors move up. Thus the output stage pulls a current from the output node. This action continues until the current through the P-channel class-AB transistor is equal to I_{b7}. Now, the current of the P-channel output transistor is kept at a minimum value, which can be set by W over L ratios of the class-AB control transistors. Note that the current through the N-channel output transistor is still able to increase. A similar discussion can be held when input signals are pulled from the class-AB output stage.

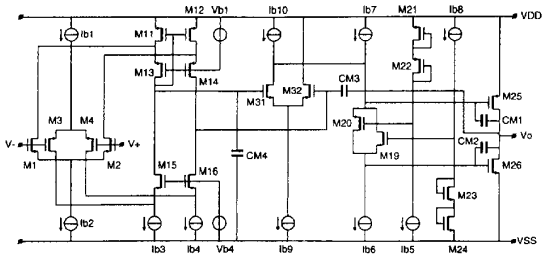


Fig. 7. Three-stage cascaded operational amplifier.

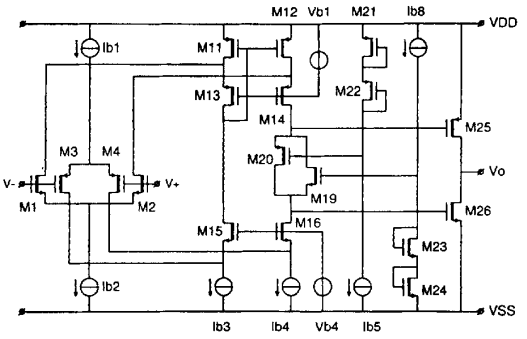


Fig. 8. Compact two-stage opamp. The floating class-AB control is biased by the cascodes of the summing circuit.

A drawback of the class-AB control is that the quiescent current of the output transistors depends on supply voltage variations. The supply voltage variations are directly put, by the gate-source voltages of the output transistors, across the finite output impedances of the floating class-AB transistors. The result is a power-supply dependent variation of the quiescent current.

IV. Topology of the Opamp

In the previous sections the rail-to-rail input stage and the rail-to-rail class-AB output stage have been described. In this section the overall topology of the operational amplifier will be described.

The conventional way to design a two-stage opamp is to place the input stage, $M_1 - M_4$ and $M_{11} - M_{16}$, and the class-AB output stage, $M_{19} - M_{26}$, in cascade, as is shown in Fig. 6. The capacitors C_{M1} and C_{M2} can be used to frequency compensate the opamp. For reasons of clarity, the g_m-control of the input stage has been omitted. Although a compact design is obtained, this approach has important drawbacks. Firstly, the gain of the amplifier decreases because the bias current sources of the class-AB control, I_{b6} and I_{b7}, are in parallel with the cascodes, M_{14} and M_{16}, of the summing circuit. Secondly, apart from the input transistors, $M_1 - M_4$, and $M_{11} - M_{12}$ and $I_{b3} - I_{b4}$ of the summing circuit , also the bias current sources of the class-AB control, I_{b6} and I_{b7}, contribute to the noise and offset of the amplifier. These bias sources contribute significantly to the input offset and noise, because the current gain between the bias sources of the class-AB control and the drain currents of the input transistors is equal to one.

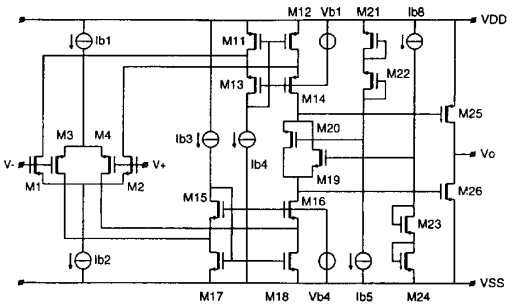


Fig. 9. Compact two-stage opamp. The summing circuit contains two current mirrors which are biased by two separate current sources.

Both drawbacks can be overcome by adding an intermediate circuit to the two stage cascaded opamp, as is shown in Fig. 7. The intermediate stage, M_{31} and M_{32}, increases the current gain between the input transistors, $M_1 - M_4$, and the bias currents of the class-AB control, I_{b6} and I_{b7}, so the noise and offset contribution of I_{b6} and I_{b7} can be neglected. The result is that the noise and offset of the operational amplifier is only determined by the input transistors, $M_1 - M_4$, and by $M_{11} - M_{12}$ and by $I_{b3} - I_{b4}$. The price to pay is more die area and a lower unity-gain frequency. In general, more stages result in a lower unity-gain frequency of the opamp. If nested Miller compensation is used, the unity-gain frequency decreases by a factor of two [5]. The die area is increased not only because an additional stage is needed, but also because additional capacitors, C_{M3} and C_{M4}, are needed to compensate the opamp. These capacitors, which are normally of the order of several pFs, occupy considerable die area.

An alternative way to reduce the noise and offset contribution of the class-AB control, without the cost of die area and a loss of unity-gain frequency, is to shift the floating class-AB control, M_{19} and M_{20}, into the summing circuit, $M_{11} - M_{16}$, as is shown in Fig. 8. The floating class-AB control is biased by the cascodes of the summing circuit. Now, the noise and offset of the amplifier are mainly determined by the input transistors and the summing circuit. This is also the case in the three stage amplifier as is shown in Fig. 7. The opamp is even smaller than the two-stage cascaded operational amplifier, as is shown in Fig. 6, because the bias sources of the class-AB control have been eliminated. Note that for reasons of simplicity, the C_{M1} and C_{M2} have been omitted.

A drawback of shifting the class-AB control into the summing circuit is that the quiescent current of the output transistors depends on the common-mode input voltage. When the common-mode input voltage varies, the tail currents of the input pairs, and therefore the currents through the cascodes, change. The result is that the bias current of the class-AB control, and consequently the quiescent current of the output transistors, depends on the common-mode input voltage. This problem can be overcome by using a summing circuit with two current mirrors, $M_{11} - M_{14}$ and $M_{15} - M_{18}$, which are biased by two separate current sources, I_{b3} and I_{b4}, as is shown in Fig. 9. Both sides of each current mirror are loaded by equal common-mode currents, coming from the input stage,

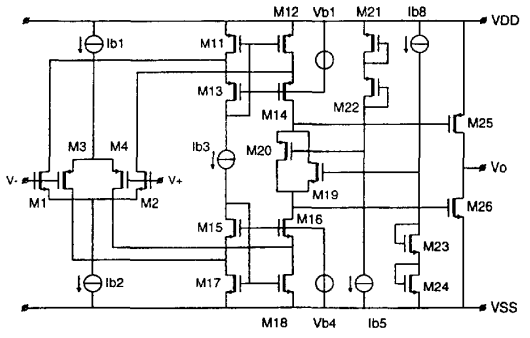


Fig. 10. Compact two-stage opamp. The summing circuit contains two current mirrors which are biased by one floating current source.

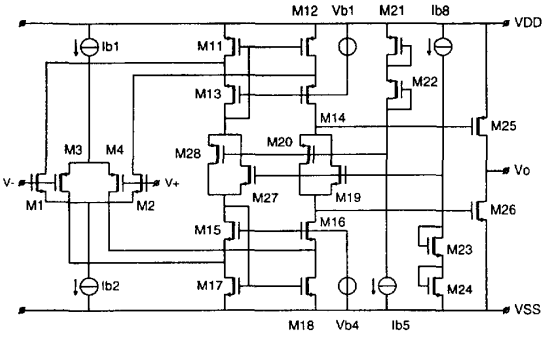


Fig. 11. Compact two-stage opamp. The floating current source is implemented by means of M_{27} and M_{28}.

$M_1 - M_4$. Since I_{b3} and I_{b4} have the same value, the output current of both current mirrors is equal to I_{b3}.

A drawback of the separate biased current mirrors is that the bias current sources of the current mirrors contribute to the noise of the amplifier because the current gain between the current sources and the drain currents of the input transistors is equal to one. Mismatch in the bias current sources will also contribute to the offset of the amplifier. To overcome these problems the current mirrors are biased by a floating current source, I_{b3}, as is shown in Fig. 10. Because of the floating architecture of the current source, it does not contribute to the noise and offset of the amplifier [8], [9].

As described in Section III, the class-AB control, and therefore the quiescent current in the output transistors, suffers from supply voltage variations. To make the quiescent current of the output transistors insensitive to supply voltage variations, the floating current source should have the same supply voltage dependency as the class-AB control. Fig. 11 shows the amplifier with a practical realization of such a floating current source, $M_{27} - M_{28}$. The floating current source has the same structure as the floating class-AB control. The value of the current source is set by two translinear loops, M_{11}, M_{21}, M_{22}, M_{28} and M_{17}, M_{23}, M_{24}, M_{27}. The mirrors, $M_{11} - M_{14}$ and $M_{15} - M_{18}$, are loaded by the drain currents of the input pairs $M_1 - M_2$ and $M_3 - M_4$, respectively. These drain currents, and consequently the gate-source voltages of M_{11} and M_{17}, change with the common-mode input voltage. If, for example, the common-mode input voltage approaches the positive supply rail, the g_m-control circuit increases the current of I_{b1} and decreases the current of I_{b2}. As a result, the gate-source voltage of M_{11} decreases while the gate-source voltage of M_{17} increases. However, this hardly effects the value of the floating current source, $M_{27} - M_{28}$, because an increase of the gate-source voltage of one mirror compensates for a decrease in the other mirror. The result is that the current of the floating-current source varies only 5% over the full common-mode input range, as is shown in Fig. 12.

Since the floating current source, $M_{27} - M_{28}$, has the same structure as the class-AB driver circuit, $M_{19} - M_{20}$, the supply voltage dependency of the current mirror compensates for the supply voltage dependency of the class-AB driver. The result is a quiescent current which is insensitive to supply voltage variations.

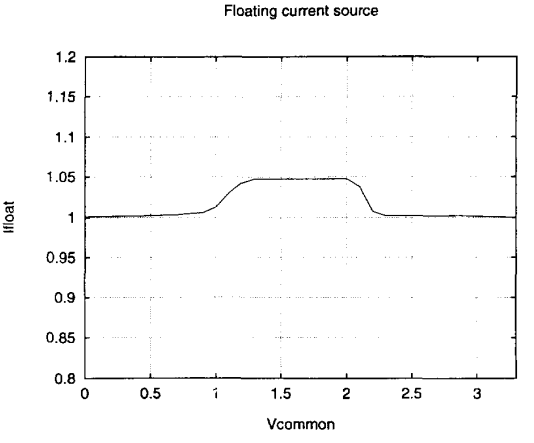


Fig. 12. Simulation result of the normalized value of the floating current source versus the common-mode input voltage.

The resulting two-stage topology is compact which makes it very suitable as a VLSI library cell. It has an offset and noise which are comparable to those of a three stage amplifier. Moreover, the quiescent current of the operational amplifier is insensitive to supply voltage variations.

V. Overall Design and Frequency Compensation

Using the topology as described in the previous section, a compact opamp with Miller compensation has been designed, and is shown Fig. 13. The opamp consists of the rail-to-rail input stage, $M_1 - M_4$, g_m-control, $M_5 - M_{10}$ and $M_{29} - M_{31}$, a summing circuit, $M_{11} - M_{18}$, and a rail-to-rail class-AB output stage, $M_{19} - M_{26}$. The floating current source, $M_{27} - M_{28}$, biases the summing circuit and the floating class-AB control. The opamp is compensated using the conventional Miller technique. The capacitors C_{M1} and C_{M2} around the output transistors, M_{25} and M_{26}, split apart the poles ensuring a 20 dB per decade roll off of the amplitude characteristic. The conventional Miller splitting shifts the output pole up to a frequency of approximately

$$\omega_{\text{out}} = \frac{g_{m_0}}{C_L} \tag{4}$$

where g_{m_0} is the transconductance of the output transistors and C_L is the load capacitor. In Fig. 14, a second design of the

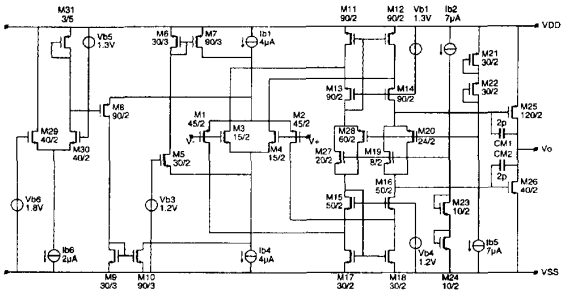


Fig. 13. Overall design of the compact rail-to-rail operational amplifier with Miller compensation.

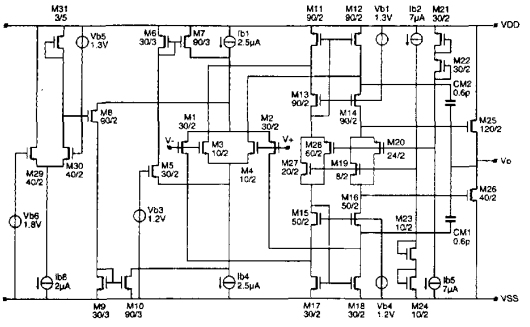


Fig. 14. Overall design of the compact rail-to-rail operational amplifier with cascoded-Miller compensation.

compact rail-to-rail opamp is shown. This opamp is basically the same as the opamp shown in Fig. 13, except for the frequency compensation scheme. This opamp is compensated by including the cascode stages, M_{14} and M_{16}, in the Miller loops. This compensation technique shifts the output pole to a frequency of approximately

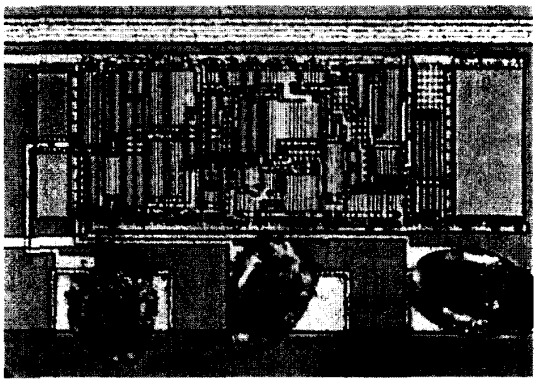
$$\omega_{\text{out}} = \frac{C_M}{C_{\text{GS.out}}} \frac{g_{m_0}}{C_L} \tag{5}$$

where C_M and $C_{\text{GS.out}}$ are the total Miller capacitor and the total gate-source capacitance of the output transistor, respectively.

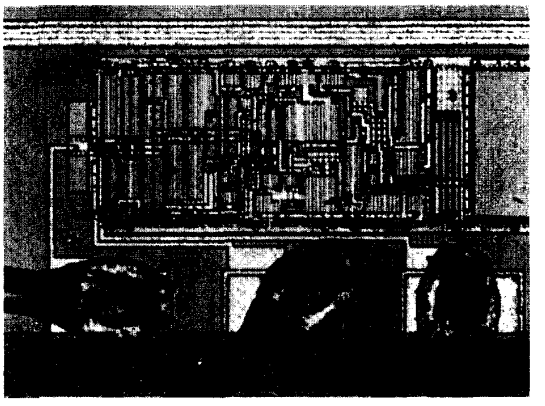
The output pole in (5), and therefore the unity-gain frequency of the cascoded Miller compensation, is a factor $C_M/C_{\text{GS,out}}$ larger than the output pole in (4). In the opamp as shown in Fig. 14, this ratio is chosen to be about 2.5, resulting in a unity-gain frequency of the compact opamp with cascoded Miller compensation which is about 2.5 times higher compared to the opamp with conventional Miller compensation.

VI. Realizations and Measurement Results

The opamps have been realized in a 1 μm BiCMOS process. The N-channel transistors and the P-channel transistors have threshold voltages of 0.64 V and -0.75 V, respectively. The micrograph of the compact opamp with Miller compensation and the micrograph of the opamp with cascoded-Miller compensation are shown in Fig. 15. A Bode plot of the compact opamp with Miller compensation is shown in Fig. 16. The opamp has a unity-gain frequency of 2.6 MHz, with a load capacitor of 10 pF. The unity-gain phase margin is 66°. Fig. 16 shows the Bode plot of the compact opamp with cascoded Miller compensation. The opamp has a unity-gain frequency of 6.4 MHz and a phase margin of 530, with the same capacitive load of 10 pF. To compare the amplifiers, the following figure of merit is used:



(a)



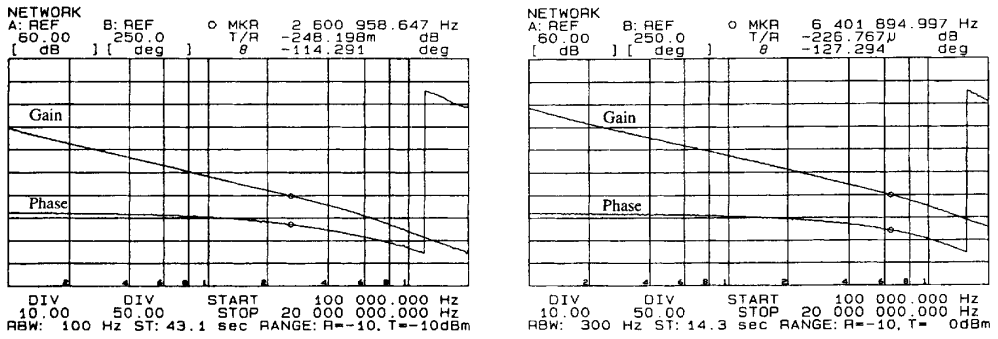
(b)

Fig. 15. Micrograph of the compactrail-to-rail operational amplifier with (a) Miller compensation. (b) cascoded-Miller compensation.

$$F = \frac{B}{P_{\text{sup}}}\bigg|_{C_L=10\,\text{pF}} \tag{6}$$

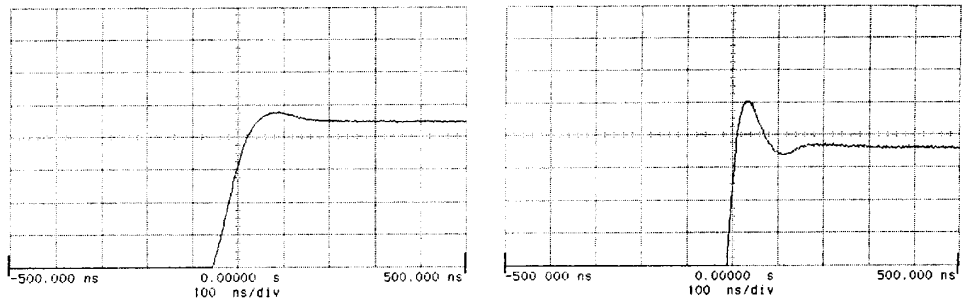
where B is the unity-gain frequency of the opamp, P_{sup} is the quiescent dissipation and C_L is the load capacitor [10]. The figure of Merits of the opamp with Miller compensation and that of the opamp with cascoded-Miller compensation are 4 and 11 MHz/mW, respectively, for a capacitive load of 10 pF. It can be concluded that the opamp with cascoded-Miller compensation uses the power about 2.5 times more efficiently, with respect to bandwidth than the Miller compensated opamp.

Fig. 17 shows the small signal step response of the opamp with Miller and cascoded-Miller compensation, respectively. The opamp with Miller compensation responds to small-signals within 1% of the final value in 220 ns, for a load of 10 pF and a step of 100 mV. The opamp with cascoded Miller compensation has a small signal-settling time 180 ns, for the same accurracy of 1%, capacitive load and step. The large signal step response of the opamps is shown in Fig. 18.



(a) (b)

Fig. 16. Bode plot of the compact rail-to-rail operational amplifier with (a) Miller compensation, and (b) cascoded-Miller compensation.



(a) (b)

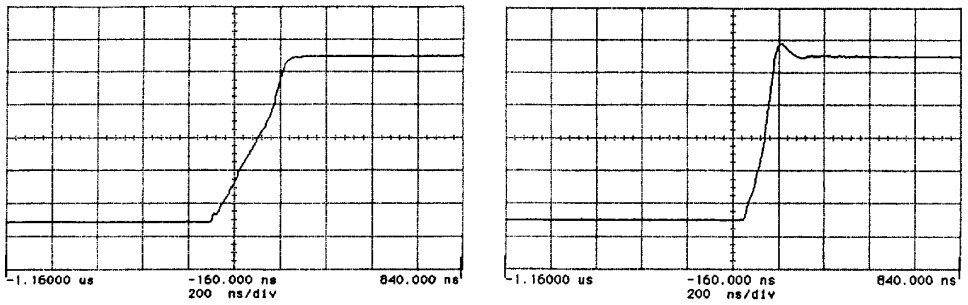
Fig. 17. Small-signal step response (V_{step} = 100 mV) of the compact rail-to-rail operational amplifier with (a) Miller compensation and (b) cascoded Miller compensation. (y-axis scale = 10 mV/div).

The 1% large-signal settling time for the compact opamp with Miller compensation is 440 ns, for a capacative load of 10 pF and a step of 1 V. The 1% large-signal settling time for the compact opamp with cascoded Miller compensation is 275 ns, for the same capacitive load and step. It can be concluded that the compact opamp with cascoded Miller compensation is faster than that with the Miller compensation.

From Fig. 18 it can be observed that the slew-rate of the opamps change by a factor of two. As was explained in Section II, in the intermediate common-mode, input voltage range in both input pairs are active. At the upper and lower part of the common-mode input range, the tail current of the actual active input pair is increased by a factor of four. Thus, in the outer parts of the common-mode input range, there is two times as much current to charge the compensation capacitor as there is in the intermediate part of the common-mode input range. Therefore, slew-rate changes by a factor of two. The slew-rate of the compact opamp with Miller compensation is 2 V/μs, when the common-voltage is in the range of V_{SS} + 1.3 V and V_{DD} − 1.3 V. It is 4 V/μs when the common-voltage is in the range of V_{SS} and V_{SS} + 1 V or in the range of V_{DD} − 1 V and V_{DD}. The slew-rate of the compact opamp with Miller compensation is 4 V/μs, when the common-voltage is in the range of V_{SS} + 1.3 V and V_{DD} − 1.3 V. It is 8 V/μm when the common-voltage is in the range of V_{SS} and V_{SS} + 1 V or in the range of V_{DD} − 1 V and V_{DD}.

At high output currents, the cascoded-Miller compensation could give rise to peaking [11]. However, at the maximum output current of this opamp, which has a value of 3 mA, the peaking is negligible. If the operational amplifier has to drive output currents much larger than 3 mA, the amplifier with Miller compensation should be used.

A list of specifications is given in Table I. The minimum supply voltage is 2.5 V. At this voltage both opamps dissipate only 0.45 mW. At supply voltages between 2.5 and 2.9 V the opamp is able to deal with common-mode voltages in the range from V_{SS} − 0.4 V to V_{DD} − 1.4 V. At supply voltages above 2.9 V, the opamps are able to deal with common-mode input voltages from rail-to-rail, or even beyond the rails. The common-mode input range is from V_{SS} − 0.4 V to V_{DD} + 0.5 V. The maximum supply voltage is 6 V and is determined by the process. The gain of both opamps is approximately 85 dB. The gain can be increased by applying gain boosting techniques to the cascodes M14 and M16 of the amplifiers as shown in Figs. 13 and 14 [12]. The offset of both opamps is about 5 mV, which is comparable to that of three-stage operational amplifiers. The offset can be reduced, to values of about 2 a 3 mV, by increasing the area of the input transistors and by using common-centroid layout structures. The CMRR of the opamps is determined by the change of offset relative to the change in common-mode input voltage. The offset changes gradually during the take-over ranges, i.e.,



(a) (b)

Fig. 18. Large-signal step response of (V_{step} = 1 V) the compact rail-to-rail operational amplifier with (a) Miller compensation; (b) cascoded-Miller compensation (y-axis scale = 200 mV/div).

TABLE I
MEASUREMENT RESULTS Vsupply = 3.3 V, Rload = 10 kΩ, Cload = 10 pf, TA = 27°C, UNLESS OTHERWISE STATED

Table I: Measurement results Vsupply=3.3V, Rload=10kΩ, Cload=10 pF, TA=27°C, unless otherwise stated

Parameter	opamp1	opamp2	
Die area	0.04	0.04	mm^2
Supply voltage range	2.5-6	2.5-6	V
Quiescent current	180	180	µA
Peak output current	3	3	mA
Common-mode input range V_{sup}: from 3 V to 6V V_{sup}: from 2.5 V to 2.9V	 V_{SS}-.4 to V_{DD}+.5 V_{SS}-.4 to V_{DD}-1.4	 V_{SS}-.4 to V_{DD}+.5 V_{SS}-.4 to V_{DD}-1.4	V
Output voltage swing	V_{SS}+0.1 to V_{DD}-0.2	V_{SS}+0.1 to V_{DD}-0.2	V
Offset voltage	4.0	5.0	mV
Input noise voltage@ 10 kHz	22	31	nV/√Hz
CMRR V_{common}: from V_{SS}-.4V to V_{SS}+1V and from: V_{SS}+1.3V to V_{DD}-1.3V and from V_{DD}-1V to V_{DD}+.5 V_{common}: from V_{SS}+1 V to V_{SS}+1.3V and from V_{DD}-1.3V to V_{DD}-1V	 70 43	 70 43	dB
Open-loop gain	85	87	dB
Unity-gain frequency	2.6	6.4	MHz
Unity-gain phase-margin	66	53	°
Slew-rate V_{common}: from V_{SS}+1.3V to V_{DD}-1.3V V_{common}: from V_{SS}-.4V to V_{SS}+1V and from V_{DD}-1V to V_{DD}+.5	 2 4	 4 8	V/µs
Large signal settling time (1%) V_{step}= 1V	440	275	ns
Small signal settling time (1%) V_{step}=100 mV	220	180	ns

Opamp 1 refers to the compact opamp with Miller compensation
Opamp 2 refers to the compact opamp with cascoded Miller compensation

common-mode voltages between V_{SS} + 1 V and V_{SS} + 1.3 V and common-voltages between V_{DD} − 1.3 V and V_{DD} − 1 V, of the current switches. Moreover, the change offset is spread out over two take-over ranges. In each take-over range the offset changes about 2 mV. The result is CMRR of 43 dB in the take-over ranges of the current switches. It increases up to 70 dB, in the other parts of the common-mode input voltage.

VII. CONCLUSION

A two stage compact operational amplifier with rail-to-rail input and output ranges has been presented. The opamp contains a rail-to-rail input stage with a g_m-control with three-times current mirrors and simple class-AB control. The g_m of the input stage varies only 15% over the common-mode input range.

The simple design of the opamp results in a very small die area of 0.04 mm^2. In spite of its simplicity it shows a very good performance. The offset and noise of the compact opamp are comparable to that of a three stage amplifier, because the floating class-AB control is shifted into the summing circuit. The summing circuit is biased by a floating current source which has the same structure as the class-AB control, resulting in a quiescent current which is independent of the supply voltage.

Using the compact amplifier, two designs have been realized. The key difference in the designs is in the frequency compensation scheme. The first design is compensated using Miller compensation. This results in a bandwidth-to-supply power ratio of 4 MHz/mW. The second amplifier is compensated using the cascoded Miller compensation, resulting in a bandwidth-to-supply-power ratio of 11 MHz/mW.

REFERENCES

[1] C. Mead and L. Conway, *Introduction to VLSI Systems*. Reading, MA: Addison-Wesley, 1980.
[2] J. H. Botma *et al.*, "A low-voltage CMOS operational amplifier with a rail-to-rail constant-gm input stage and a class AB rail-to-rail output stage," in *Proc. ISCAS 93*, pp. 1314–1317.
[3] J. N. Babanezhad, "A rail-to-rail CMOS Op amp," *IEEE J. Solid-State Circ.*, vol. 23, pp. 1414–1417, 1988.
[4] W.-C. S. Wu, "Digital-compatible high-performance operational amplifier with rail-to-rail input and output ranges," *IEEE J. Solid-State Circ.*, vol. 29, no. 1, Jan. 1994.
[5] J. H. Huijsing and D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output ranges," *IEEE J. Solid-State Circ.*, vol. SC-20, pp. 1144–1150, Dec. 1985.
[6] R. Hogervorst *et al.*, "CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage," *Analog Integrated Circ. Signal Proc.*, vol. 5, no. 2, pp. 135–146, Mar. 1994.
[7] D. M. Montecelli, "A quad CMOS single-supply op amp with rail-to-rail output swing," *IEEE J. Solid-State Circ.*, vol. SC-21, pp. 1026–1034, Dec. 1986.
[8] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. H. Huijsing, "A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," in *Dig. ISSCC '94*, Feb. 1994, San Francisco, CA, pp. 244–245.
[9] J. H. Huijsing and J. P. Tero, "Combination driver-summing circuit for rail-to-rail differential amplifier," US Pat. Appl. Ser. No. 36774, filed Mar. 25, 1993.
[10] M. J. Fonderie and J. H. Huijsing, *Design of low-voltage bipolar operational amplifiers*. Norwell, MA: Kluwer, 1993, p 171.
[11] R. G. H. Eschauzier and J. H. Huijsing, "An operational amplifier with multipath Miller zero cancellation for RHP zero removal," in *Proc. ESSCIRC* , (Seville, Spain), Sept. 1993, pp. 122–125.
[12] K. Bult and G. J. G. M Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC Gain," *IEEE J. Solid-State Circ.*, vol. 25, pp. 1379–1383, Dec. 1990.

Ron Hogervorst, for a photograph and biography, see this issue, p. 1504

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He joined Hawker Siddeley Dynamics in 1966 and worked on satellite attitude control and propulsion systems. He joined Plesset Research in 1972 and designed high frequency integrated circuits for mobile radio and radar applications in both silicon and gallium arsenide technologies. In 1979 he moved to Ferranti Semiconductors to lead a group manufacturing and developing RF bipolar power transistors, and since 1984, he has been with Philips Semiconductors in Sunnyvale CA, where he is currently Design Engineering Manager for LAN products. As such, he is involved in the development of wired and wireless LAN circuits in bipolar, CMOS, BiCMOS technologies and his current areas of interests are in analog signal processing, high speed data recovery and generation and low voltage circuit techniques.

Ruud G. H. Eschauzier, for a photograph and biography, see this issue, p. 1504.

Johan H. Huijsing, for a photograph and biography, see this issue, p. 1504.