

A Compact SPICE Model for Organic TFTs and Applications to Logic Circuit Design

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Abstract—This work introduces a compact DC model developed for Organic Thin Film Transistors (OTFTs) and its SPICE implementation. The model relies on a modified version of the Gradual Channel Approximation (GCA) that takes into account the contact effects, occurring at non-ohmic metal/organic semiconductor junctions, modeling them as reverse biased Schottky diodes. The model also comprises channel length modulation and scalability of drain current with respect to channel length. To show the suitability of the model, we used it to design an inverter and a ring oscillator circuit. Furthermore, an experimental validation of the OTFTs has been done at the level of the single device as well as with a discrete-component setup based on two OTFTs connected into an inverter configuration. The experimental tests were based on OTFTs that use small molecules in binder matrix as an active layer. The experimental data on the fabricated devices have been found in good agreement with SPICE simulation results, paving the way to the use of the model and the device for the design of OTFT-based integrated circuits.

Index Terms—Organic thin film transistors (OTFTs), SPICE modeling, flexible electronics.

I. INTRODUCTION

CHARGE transport mechanisms in organic field-effect transistors (OFETs) have been investigated since the late eighties [1]. After more than a decade of interdisciplinary research efforts to better understand the materials, processing, and device architecture requirements, it is now possible to satisfy both performance and reliability requirements needed in product applications [2]. Flexible active matrix backplanes based on solution-processed organic field-effect transistors on low-temperature plastic substrates have been demonstrated [3], and are now capable of driving thin film displays, based on either liquid-crystal displays (LCD) or organic light-emitting diodes (OLED), as well as large-area sensor arrays, such as organic photodetectors (OPD) [4].

Progress has also been made in fabricating electronic circuits based on OFETs for applications in radio frequency identification tagging (RFID) [5], chemical and biochemical

sensors [6], [7], and in developing new platforms for processing logic data based on OFET devices and logic gates [8]. In the meantime, the initial challenges in production of high performance air-stable organic materials in gram scale are now solved, as required for manufacturing OFET scalable circuits and related products. It is now clear that state-of-the-art p-type OFETs with suitable materials and device structures can exhibit speed performance, stability and uniformity of parameters over large-areas comparable to those of a Si Thin Film Transistor. Although the performance and integration scale of organic thin film transistor-based circuits are not comparable with those achieved by silicon in VLSI/ULSI CMOS technology, the possibility to design and simulate analogue and digital circuits that can be fabricated on thin and flexible substrates makes the corresponding technology platforms very attractive.

Developing accurate models of OFET devices is of essential importance in order to allow adapting standard design and verification tools and use well-established design and simulation techniques to approach more complex integrated organic electronic circuits and systems, and predict their behavior prior to prototype manufacturing and scale up. Also it is critical to develop the equivalent circuit models for OFETs, in a way they are simple enough to perform circuit simulations at transistor-level transient mode in a relatively short time. For that, it is also essential to develop simulation models sufficiently accurate to capture the physical effects that govern charge transport mechanisms occurring in such devices, and translating them into suitable behavioral models for both DC and transient analysis.

The first attempts to develop OFET compact device models were focusing on the peculiar charge transport mechanisms occurring in the channel made by an organic semiconductor material, based on theories developed so far such as variable range hopping [9], [10]. In more recent works the compact models have been adapted to include the effect of non-ohmic contacts, often occurring at the interface between source and drain contacts with the organic semiconductor channel [11], and the dependence of contact resistance on both the gate voltage and charge trapping mechanisms in grain boundaries of polycrystalline organic semiconductors, of particular relevance in staggered transistor devices [12], when the gate length is reduced in the attempt of improving the speed performance of OFET-based logics [13].

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Manuscript received ***; revised ****.

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Another challenge to be faced with when developing models of OFETs is the possibility to convert physical models into SPICE-equivalent compact models. Whenever this is possible and accurate enough for representing the real behavior of OFET devices in their different working regimes, the equivalent compact model will inevitably result in a much more efficient tool for simulation and faster design of circuits at relatively high level of complexity, still making use of standard approaches for circuit design and simulation [14]. In the field of TFTs, in fact, given the diversity of device architectures, materials and fabrication technologies, creating one compact device model fitting all possible options remains an open challenge and the need of developing SPICE-equivalent standard models while extracting parameters from electrical device characterization is evident [15]. We note that the existing circuit simulation software SmartSpice by Silvaco Inc. includes an OTFT simulation model, which takes into account contact effects by simply introducing “extrinsic” linear resistances on the source and/or drain side of the device and not Schottky diodes or other non-linear elements [16]. Unlike this approach, we aim at explicitly accounting for non-ohmic contact behavior.

In this work, we report an implementation in SPICE of a compact DC model developed for Organic Thin Film Transistors (OTFTs) and tested on devices that use small molecules in a binder matrix as active organic semiconductor layer. The compact model is highly accurate, yet founded on the original Gradual Channel Approximation (GCA) theory for a unified transistor model proposed by Shockley in 1952 [17], and includes contact effects of non-ohmic junctions, as well as the effect of channel length scaling and gate voltage, which allows working out the modulation of drain current as a function of the device channel length for design and simulation of high performance device architectures and circuits. The experimental data are obtained from a consistent set of fabricated p-type devices with different geometries [18], adapted to represent the characteristics of OFET devices made by given fabrication techniques. The simulation results are then validated against experimental data in fair agreement with each other. The approach is further extended by deriving the DC characteristic of an inverter gate, and using it in the simulation of a ring oscillator based on the same inverter. From the evaluation of performance of these circuits, the proposed model and approach are suitable now for use in standard design kits to allow design of complex electronic circuits based on a subset of the fabricated test structure devices.

II. DEVICE MANUFACTURING

P-channel OTFTs, with staggered top-gate configuration (Fig. 1), were fabricated on heat-stabilized, low roughness polyethylene-naphthalate PEN foils (Teonex®Q65FA, 125 μm thick) by using solution processed semiconductor and dielectric. Patterning of the source and drain gold contacts, deposited by evaporation, were made by standard optically lithography and wet etching. A self-assembled monolayer of pentafluorobenzene thiol (PFBT) was deposited by spin coating on the metal contacts in order to improve the structural properties of organic layer [19] and carrier injection

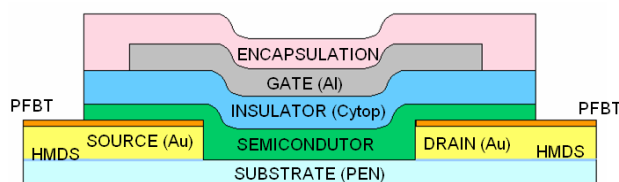


Fig. 1. Section of the layout of the p-channel OTFT.

from the electrodes. Small-molecule organic semiconductor (SmartKem®p-FLEX™, by SmartKem-Ltd, 30 nm thick) and polymer gate dielectric (Cytop™, 550nm thick, relative dielectric constant ~ 2.1) were sequentially deposited by spin coating. Finally, gate electrode (evaporated Al, 50 nm thick) and device islands were photolithographically defined. All curing steps were carried out below 100° C to be compatible with the PEN substrate. The OTFTs sizes were in the range from 2 to 100 μm for channel length L , and 50, 100 and 200 μm for channel width W .

III. DC MODEL OF THE DEVICE

The electrical characteristics of OTFTs often show some peculiarities that are not present in the characteristics of conventional crystalline silicon MOSFETs and that are not reproduced by the existing compact models. In particular, the drain current obtained from the transfer characteristics at low V_{DS} of OTFTs, above the threshold regime, frequently has a power law dependence on the gate voltage that differs from the linear behavior predicted by the GCA of a conventional MOSFET for a low drain-source voltage drop. The exponent of the power law is often found greater than 1, giving the transfer characteristics in above threshold a convex function behavior that cannot be ascribed to series resistance effects but has to be attributed to the intrinsic dependence of the carrier mobility upon charge concentration in the organic semiconductor [20]. On the other hand, often it is found that, in below threshold regime, the transfer characteristics of OTFTs have an exponential like behavior.

Moreover, the output characteristics of OTFTs often undergo contact resistance effects that are related to the presence of non-ohmic metal/organic semiconductor junctions. It is found [13] that, in normal operation, the electrical behavior of the metal/organic semiconductor on the source side of the OTFT is similar to that of a reverse biased leaky Schottky barrier junction. In addition, the reverse current is gate voltage dependent [13]. The presence of such junction can appreciably reduce the output current with respect to estimations made by using the square-law behavior of the GCA theory. In fact, the presence of a reverse biased Schottky junction at source side of the device determines a voltage drop between the metal contact and the organic semiconductor [12], [13], reducing the effective gate-to-source and drain-to-source voltage seen at the ends of the channel. Since the relevance of these contact effects depends on the ratio between the contact and channel resistance, their influence becomes progressively more important as the channel length is scaled down [12],

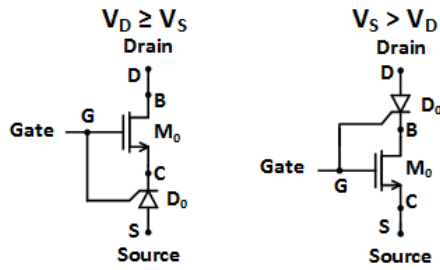


Fig. 2. Equivalent circuit representing the OTFT model.

[13]. Hence, it is very important to take into account these effects in the development of a compact model that has to be used to design circuits that employs short channel OTFTs. Most of the OTFT models already proposed do not explicitly account for contact effects [21], [22], [23], [24] or do it in a phenomenological way [25]. A quite small number of compact models that accounts for non-ohmic source and drain contacts have already been proposed [26], [27]. Nevertheless they often employ a somewhat non-physical modeling of the metal/organic semiconductor interface. In fact, in [26] the source junction is modeled as forward biased Schottky diode, while it is commonly accepted that physically it is a reverse biased junction, and in [27] a “contact” TFT is introduced, while, in our paper, a gated diode is considered.

For these reasons we have developed a compact DC model that can take into account non-linearity in the $I_D - V_{GS}$ curves as well as contact effects in the $I_D - V_{DS}$ curves. The model has been tested on experimental data of the OTFTs fabricated as described in Sec. II.

The model illustrates a real OTFT as a serial combination of an “ideal” OTFT which closely follows the GCA (M_0 in Fig. 2), with a leaky reverse biased Schottky diode (D_0 in Fig. 2) existing on source terminal side. Additionally, reverse current of this diode depends on V_{GS} and therefore we call it as a gated diode. For convenience, the equations describing the model were written with respect to n-type devices, but clearly can be easily adapted to p-type devices.

Analogously to [20], we choose to model the current-voltage relationship of M_0 as:

$$I_{OTFT} = F(V_{GC}) - F(V_{GD}) + I_{off} F(V) = K_1 \frac{W_{eff}}{L_{Early}} \left(V_{SS} \log \left(1 + e^{\frac{V - V_{FB}}{V_{SS}}} \right) \right)^m \quad (1)$$

$$I_{off} = I_0 \frac{W_{eff}}{L_{Early}} V_{DC}$$

$$L_{Early} = L - dL_{Vds} |V_{DC}|$$

where K_1 is a prefactor dependent on the carrier mobility and on the gate insulator capacitance per unit area; W_{eff} is the effective channel width of the OTFT; L is the geometrical (as drawn) length of the channel; V_{SS} is a parameter dependent on the subthreshold slope of the transfer characteristics; V_{DC} , V_{GC} and V_{GD} are the potential drop between D, C and G terminals (see Fig. 2); V_{FB} is a voltage related to the threshold voltage of the OTFT; I_{off} is the off current; m is an exponent related to the above threshold behavior of the transfer characteristics; L_{Early} is the channel effective

length due to drain bias modulation; dL_{Vds} is a parameter determining the channel length modulation; and I_0 is the off current prefactor. Since source and drain contacts are symmetric, a metal/organic semiconductor junction is formed also on the drain end of the channel: this has no impact on the operation of the OTFTs since, in normal operation, the resulting Schottky diode is polarized in forward bias, thus determining only a small voltage drop on the drain junction that has been neglected in our model. This is why in normal operation (Fig. 2, left), we safely assume $V_{DB} = 0$.

At this point, we note that the core function $y = \log(1 + e^x)^m$ of Eqs. (1) behaves like $y = x^m$ (power law) for $x > 0$ and like $y = e^{mx}$ (exponential law) for $x < 0$, and, hence, is able to model the transfer characteristics of the “ideal” OTFT either above or below the subthreshold regime, with a single analytical equation. Another advantage of Eqs. (1) is that it automatically fulfill the GCA theory. In fact, if we neglect the I_{off} term, the underlying structure of (1) is

$$I_{OTFT} = F(V_{GC}) - F(V_{GD}) \quad (2)$$

and this is exactly the functional form that is obtained when applying the GCA with F proportional to the integral of the channel conductance. The various parameters used in Eqs. (1) have been determined using an optimizing procedure on the transfer and output characteristics of long channel devices, in which contact effects are negligible.

The I-V relationship of the contact diode D_0 is modeled by the following equations [13]:

$$I_{rev} = I_{00d} W_{nom} \left[\left(\frac{\max(V_{GS} - V_{gg0}, 0)}{V_\infty} \right)^\beta + \left(\frac{V_{gmin} - V_{gg0}}{V_\infty} \right)^\beta \right] e^{\left(\frac{V_{CD}}{V_{diode}} \right)^\alpha}; \quad (3)$$

$$I_{diode} = -I_{rev} \left(e^{-\frac{qV_{CS}}{\eta\kappa T}} - 1 \right)$$

where V_{CS} (V_{GS}) is the potential drop between C and S (G and S) terminals; I_{rev} is the diode reverse current which depends on both V_{CS} (Schottky effect) as well V_{GS} (gated diode); I_{00d} is the diode reverse current prefactor; $V_\infty = 1V$ is a normalization coefficient; V_{diode} and α are parameters determining the I_{rev} dependency upon V_{CS} ; β , V_{gmin} and V_{gg0} are parameters determining the I_{rev} dependency upon V_{GS} ; η is the diode ideality factor; and q , κ and T have their usual meanings: elementary charge, Boltzmann constant and absolute temperature.

In Eqs. (3) the first term describes the power law dependence of the reverse current upon the gate bias found in OTFTs [13]. The exponential term, instead, represents the dependence of I_{rev} upon the potential drop on the metal/organic semiconductor junction and takes into account the presence of the Schottky barrier lowering effect [28]. The parameter β is a strictly positive real number: while determining the numerical value of the parameters, we impose the condition that V_{gmin} is strictly greater than V_{gg0} . In this way the quantity in square bracket in Eq. (3) is always strictly positive, because of the presence of the max operator and the aforementioned constraint on V_{gmin} and V_{gg0} .

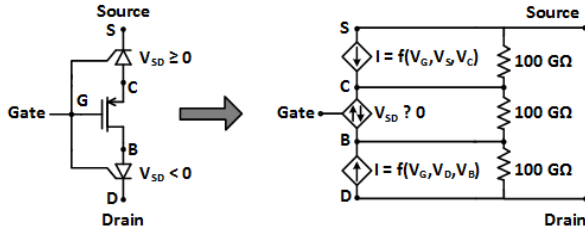


Fig. 3. SPICE equivalent implementation of the OTFT model.

As stated above, the presence of the reverse biased Schottky diode in series to the source determines a potential drop that reduces the effective gate bias (V_{GC}) seen by M_0 , thus reducing the output current. In this way, the saturation current of short channel OTFT is affected by the saturation of D_0 . It has to be pointed out that there is no explicit solution for the potential of V_C . Instead, it is computed by a software for circuit simulation (e.g., Verilog-a) by solving the following equality with respect to V_{CS} :

$$I_{diode}(V_{CS}, V_{GS}) = I_{OTFT}(V_{CS}, V_{GS}, V_{DS}) \quad (4)$$

The parameters I_{00d} , V_{gg0} , V_{gmin} , V_{diode} , β and α used in the diode equation [eq. (3)] have been determined by fitting with Eq. (4) the transfer and output characteristics of short channel devices, in which contact effects are prominent.

IV. SPICE IMPLEMENTATION

In order to define the p-OTFT model in SPICE we used a behavioral approach, grouping several components into a functional block. To implement Eqs. (1)-(3) we used voltage controlled current sources (VCCS), as in Fig. 3. Using the SPICE function “VALUE”, each current contribution is represented in the model as a different current source.

In Fig. 2 illustrating the DC model of the device, the location of the Schottky diode in the device network as well as the sign of the current passing through the channel of M_0 , the “ideal” transistor (GCA), depends on the sign of the potential drop between S and D nodes. In the SPICE implementation of the model, we have considered that the sign of V_{DS} may change and, therefore, two gated diodes have been included in the scheme of Fig. 3. The corresponding I-V relationships (GDiodeS and GDiodeD in the SPICE model of Fig. 4) are formulated in order to model a p-type OTFT: the model is obtained from Eqs. (1)-(3), valid for a n-type OTFT, by changing the signs of currents and potential drops. The inversion of sign of the currents in the model is implicitly obtained by reverting the order of the terminals appearing in the current sources declarations with respect to the order in which they would appear from a straightforward implementation of Eqs. (1)-(3). Likewise, the inversions of sign of the voltage drops is implicitly obtained by reverting the order of the terminals appearing in each of the voltage drop operators of the model. The same approach was followed to express the current contribution of M_0 . Depending on the sign of V_{DS} , one of the gated diodes of Fig. 3 is short circuited. This leads to the fact that the voltage regulating the current contribution

```
.SUBCKT p-OTFT_L100 pg ps pd
RINT1 pc pb 100G
RINT2 pb pd 100G
RINT3 ps pc 100G

GDiodeS ps pc VALUE {-(I00d*Weff *
+(PWR(MAX(V(ps,pg) - Vgg0), 0), beta_exp) + PWR(Vgmin - Vgg0, beta_exp)) *
+exp(PWR(V(ps,pc)/Vdiode, alfa_exp)) *
+(exp(-(V(ps,pc)/(0.026*eta))) - 1)}

GIFT pc pb VALUE {IF((V(ps,pd)>0), (K1 * (Weff/(L - dL_Vds * ABS(V(pc,pd)))) *
+(PWR((Vss * LOG(1+exp((V(pc,pg) - Vfb)/Vss))), m_exp) -
+PWR((Vss * LOG(1 + exp((V(pd,pg) - Vfb)/Vss))), m_exp) +
+(100 * (Weff/(L - dL_Vds * ABS(V(pc,pd)))) * V(pc,pd))), (K1 *
+(Weff/(L - dL_Vds * ABS(V(ps,pb)))) *
+(PWR((Vss * LOG(1+exp((V(ps,pg) - Vfb)/Vss))), m_exp) -
+PWR((Vss * LOG(1 + exp((V(pb,pg) - Vfb)/Vss))), m_exp) +
+(100 * (Weff/(L - dL_Vds * ABS(V(ps,pb)))) * V(ps,pb))))}

GDiodeD pd pb VALUE {-(I00d*Weff *
+(PWR(MAX(V(pd,pg) - Vgg0), 0), beta_exp) + PWR(Vgmin - Vgg0, beta_exp)) *
+exp(PWR(V(pd,pb)/Vdiode, alfa_exp)) *
+(exp(-(V(pd,pb)/(0.026*eta))) - 1)}

* PARAMS:
***GEOMETRY
.PARAM Weff = 245
.PARAM L = 100
***TFT PARAMETERS
.PARAM m_exp = 2.490
.PARAM K1 = 2.070e-010
.PARAM Vfb = -11.317
.PARAM Vss = 2.856
.PARAM I00 = 1.959e-015
.PARAM dL_Vds = 0.117
*****
.ENDS p-OTFT_L100

***DIODE PARAMETERS
.PARAM alfa_exp = 0.167
.PARAM beta_exp = 2.353
.PARAM eta = 1
.PARAM Vdiode = 0.667
.PARAM I00d = 4.021e-012
.PARAM Vgmin = -24.930
.PARAM Vgg0 = -25.930
```

Fig. 4. Code of the OTFT SPICE model.

of M_0 is in one case ($V_{DS} > 0$) that on the terminals pd and pc (d and c nodes) and in the other case ($V_{DS} < 0$) that on the terminals pb and ps (b and s nodes). These two cases are implemented in SPICE by an “if” condition.

Differently from Fig. 2, the SPICE model needs additional resistors in order to avoid convergence problems due to serially connected dependent current sources. These resistors, with a value of 100 GΩ, practically behave as an open circuit and do not corrupt the drain current.

The complete SPICE model for the p-type OTFT, with all parameter values included, is given in Fig. 4, where pc, pd, pb, ps, pg correspond to C, D, B, S and G nodes of Fig. 3. To show the accuracy of the SPICE model, we plot simulation results and experimental data together in Figs. 5(a)-5(d) for a long ($L = 100 \mu m$) and a short ($L = 10 \mu m$) channel device ($W = 200 \mu m$ in all cases). The supplied voltage is $V_{DD} = 50 V$. We sweep V_{SD} for a set of V_{SG} in Figs. 5(a)-5(b) and V_{SG} for a set of V_{SD} in Figs. 5(c)-5(d). Figs. 5(a)-5(d) clearly show that the effect of the channel length modulation and the scalability of the drain current are effectively accounted for in the model. The compactness of the model allows the fabricated devices to be efficiently simulated.

V. APPLICATION EXAMPLES

In this Section we discuss some application examples designed using the SPICE model introduced in this paper. In particular, we focus on an inverter and a ring oscillator. The simplest inverter topologies using only one type of transistor, p-type in our case, composed of only two transistors and requiring a single voltage supply, still resulting in a reasonable output in terms of gain and noise margin behavior, are the

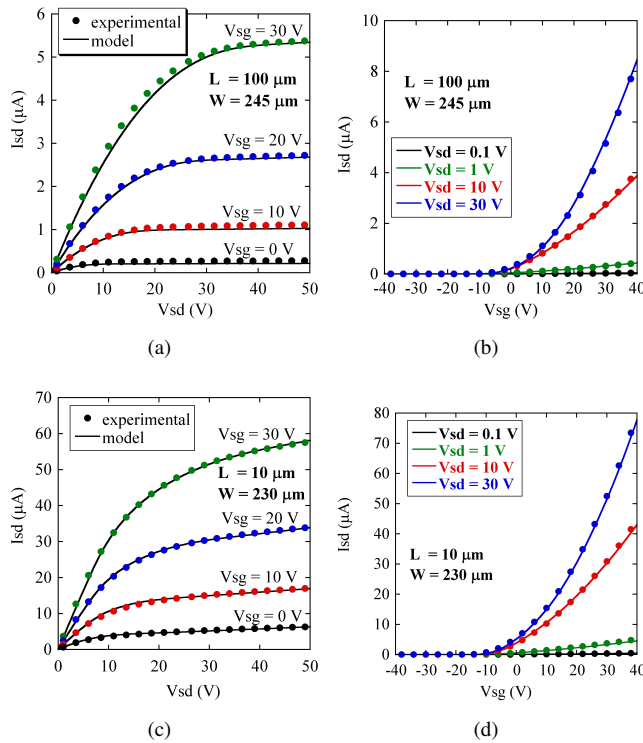


Fig. 5. Output characteristics I_{SD} vs V_{SD} and transfer characteristics I_{SD} vs V_{SG} for several OTFT with $W = 200 \mu\text{m}$ and different L : (a) I_{SD} vs V_{SD} for $L = 100 \mu\text{m}$; (b) I_{SD} vs V_{SG} for $L = 100 \mu\text{m}$; (c) I_{SD} vs V_{SD} for $L = 10 \mu\text{m}$; (d) I_{SD} vs V_{SG} for $L = 10 \mu\text{m}$. Open circles represent measured data, continuous line the model output.

diode loaded or current source loaded (CSL), also known as zero V_{GS} loaded, circuits [29], [30]. For the inverter design employing depletion type transistors both for the driver and the load transistor, it is more appropriate to use, rather than the diode loaded one, a CSL type inverter, whose electrical scheme is illustrated in Fig. 6(a). In this scheme, the load transistor is connected in a zero source-gate configuration. Since all the OTFTs are depletion type, the load transistor behaves as a current source as long as it operates in saturation region. The ratio of M_D and M_L sizes determines the location of the trip (middle) point, the limits of high and low level, and the sharpness (gain) of the VTC curve. In particular, to pull down the output, the load transistor must be r times larger than the load. For this reason we set this aspect ratio as $r = 10$ ($W_D = W_L = 200 \mu\text{m}$, $L_D = 100 \mu\text{m}$, $L_L = 10 \mu\text{m}$), which is not an optimized value but corresponds to the sizes of available OTFTs. For these OTFTs, we can use for our simulations the parameter set calculated from the experimental data.

The voltage transfer characteristics (VTC) as well as the gain (derivative of VTC) curve are drawn in Fig. 6(b). Here, the supply voltage ranges from 0 to 50 V and the input is swept between these values as well. For the high level of input, the output reaches 0 V although the opposite is not valid for the low level of input. This typical situation of a CSL type inverter can be improved by optimizing the ratio of load and driver transistors. On the other hand, due to low output resistance of the inverter, the gain is around 4. This is still an acceptable

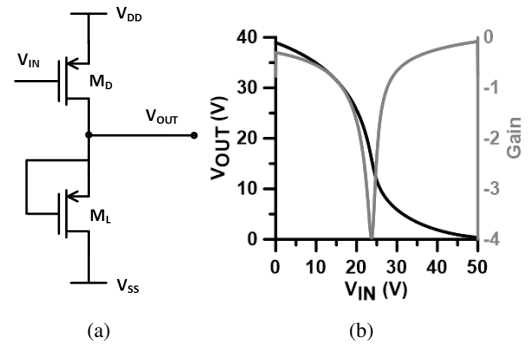


Fig. 6. (a) Topology of the CSL inverter. (b) Voltage transfer characteristics (VTC) and gain of the inverter.

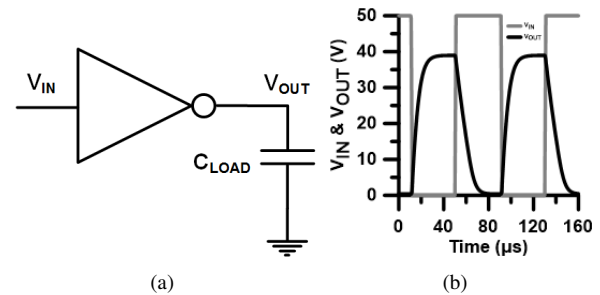


Fig. 7. (a) Scheme of an inverter with a capacitive load. (b) Output of the inverter for an ideal square wave input.

value for an OTFT based inverter circuit [31]. Moreover, we also simulated the same topology with long channel devices ($L = 100 \mu\text{m}$), sacrificing speed but increasing the output resistance of the inverter, and obtained a gain of 20 which is a very good value for OTFT based inverters [30]. Clearly, better performances can be obtained using improved topologies with a larger number of devices and external bias voltages [30]: these topologies are beyond the scope of this paper.

To design the ring oscillator, all the device intrinsic and parasitic capacitances are combined into an equivalent load capacitance at the output node for simplicity (C_{LOAD} in Fig. 7(a)). The value of this capacitor (2pF) results from a (worst case) approximation [32] based on the geometry and typical parameters [18] of the device. Under this assumption, we simulate a single inverter excited by an ideal square wave, and report the results in Fig. 7(b), where the input and output waveforms of the inverter are shown. With a square wave input of 12.5 kHz frequency, the rise and fall behavior of the output can be clearly observed.

The ring oscillator circuit (Fig. 8(a)) is designed with an odd number of inverter stages. In particular, a chain of 11 inverters has been used to obtain a square wave output with reasonable low and high levels. The result of the SPICE simulations with our OTFT model is given in Fig. 8(b). We obtain a low-to-high propagation delay equal to $\tau_{PLH} = 7.81 \mu\text{s}$, and a high-to-low propagation delay equal to $\tau_{PHL} = 10.16 \mu\text{s}$. The frequency of operation is measured to be 4.82 kHz , a value in agreement with the measured rise and fall times and number of stages. Also note that, the high and low level of outputs agree with Fig. 6(b). The frequency of oscillation may be increased by

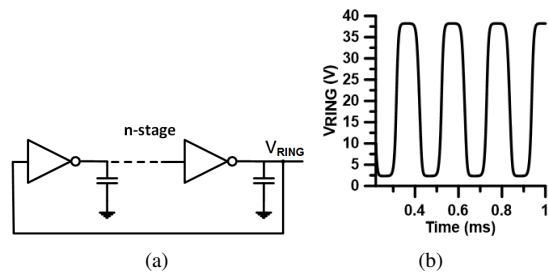


Fig. 8. (a) Electrical scheme of a ring oscillator. (b) Output waveform.

decreasing the number of stages. However, setting the number of stages below a critical value degrades the high and low levels of the output. For such a case, the shape of the output waveform becomes more sinusoidal, which is the case of some works [31], [33], [34], [35]. In contrast, the number of stages are usually chosen much larger than the minimum value, i.e. much greater than 3, in order to decrease the sensitivity of frequency with respect to number of stages and obtain a square wave at the output [32]. We have simulated ring oscillators consisting of different number of stages and confirmed these expectations as well as a frequency inversely proportional to the number of stages.

VI. EXPERIMENTAL RESULTS

In this Section we report experimental results obtained on the designed inverter. Our experiments were carried out by using discrete OTFTs externally connected into the inverter configuration. The approach is limited by the use of discrete components, instead of integrated ones, still it is effective in proving the suitability of the model and the performance of the fabricated devices, in view of more complex designs based on the integration of more than two devices.

The experimental setup consists of the devices under testing, a probe system (Süss MicroTec PM5 Probe Station) and a 4200-SCS Keithley® parameter analyzer. The die hosting the OTFTs is placed on the probe station and contacted with appropriate probes (probe tips $7 \mu\text{m}$ radius). By this way, the connections for the CSL topology are realized externally. The die contains a matrix array composed of sub-cells within unit cells where each sub-cell contains differently sized transistors while the larger unit cells are identical each other. The given OTFTs used in the experiments have been always chosen randomly in the available matrix and characterized before their use. As stated before, the DC measurements have been conducted with the Keithley® 4200-SCS parameter analyzer.

A typical way to examine the inverter circuit performance is to change the dimensions (as the design parameter) of M_L and M_D and observe the shift in VTC curves. Additionally, we can compare these experimental results with SPICE simulations in order to verify the accuracy of our model for the inverter circuit. For SPICE simulations we used the compact DC model, while, for the experiments, the measurements were done under standard conditions (in terms of air, light and temperature) and repeated more than once by choosing different unit cells on the die. We observed consistent results and, thus, concluded that there is not a significant mismatch on the same die.

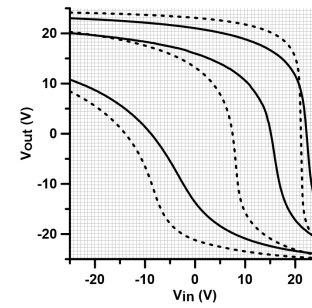


Fig. 9. Comparison between experimental VTCs (solid line) and SPICE simulations (dashed line) of inverters with different sizes: from left to right $L_L = \{5 \mu\text{m}, 20 \mu\text{m}, 50 \mu\text{m}\}$.

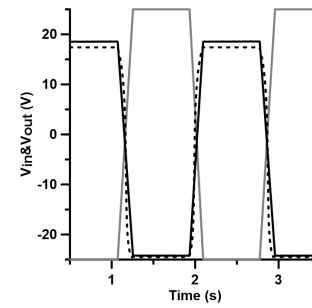


Fig. 10. Truth table of the inverter: input (solid grey line) and ideal (dashed line) and experimental output (solid black line).

The width of both the driver and load transistor were fixed as $W_D = W_L = 200 \mu\text{m}$, and the length of the driver transistor as $L_D = 100 \mu\text{m}$. Then, we carried out experiments and simulations by selecting load transistors with different values of L_L , that is, $L_L = \{5 \mu\text{m}, 20 \mu\text{m}, 50 \mu\text{m}\}$. The experimental and simulation results for these cases are shown in Fig. 9, where the most left curves correspond to the minimum size load transistor case and the most right curves to the maximum size load transistor case. It appears clear from Fig. 9 that, for the larger values of channel length of the load transistor, the VTC curve reaches the rails and exhibits a sharp transition (high gain) while sacrificing the symmetry of the curve results in a shifted trip point and therefore reduced noise margin. On the other side, choosing a small value for L_L results in a degraded performance in terms of gain and maximum and minimum levels observed at the output. We note that simulation and experimental results are in good agreement. The only difference is the presence of a slight shift between the corresponding curves. This mismatch may be due to the extraction of OTFT model parameters from characterization data performed in a different die, and to additional contact resistance of the measurement setup, before compensation.

Finally, we illustrate a graphical representation of the truth table of the inverter as in Fig. 10. Here we apply an ideal square wave input with very large rise and fall times and therefore the output waveform exhibits a static, i.e., DC characteristics, behavior. Experimental and simulation results are in agreement as expected.

VII. CONCLUSION

In this work, we presented a compact model for OTFTs that has been tested on devices fabricated with an active layer making use of small molecules in a binder matrix. The model includes contact effects of the non-ohmic junctions, comprises channel length modulation and scalability of drain current with respect to channel length of the device. The SPICE model was implemented with a behavioral approach to mimic the mathematical equations of the device and, then, used to design an inverter circuit and a ring oscillator. In particular, an inverter with a gain of 4 for the simplest case and a ring oscillator, which consists of 11 stages, operating at a frequency of 4.82kHz , have been designed. Experimental tests were also performed on single OTFTs externally connected in the inverter configuration. The good performance obtained allows us to conclude that the fabricated devices are suitable for the design of OTFT integrated digital circuits and, in the long term, for applications in wearable electronics, flexible sensors and large area electronics.

ACKNOWLEDGMENT

This work has been partially funded by MIUR by means of the national Program PON R&C 2007-2013, project "Elettronica su Plastica per Sistemi Smart disposable" (PON02 00355 3416798). The Authors would also like to acknowledge Matteo Rapisarda and Sabrina Calvi for device fabrication and Lucia V. Gambuzza for her collaboration during measurements.

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