INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2015; **00**:1–16
Published online in Wiley InterScience (www.interscience.wiley.com).

A Comparative Design Study of Continuous-Time Incremental Sigma-Delta ADC Architectures

Sha Tao* and Ana Rusu*

KTH Royal Institute of Technology, Isafjordsgatan 22, 16440 Kista, Stockholm, Sweden

SUMMARY

This paper presents a comparative design study of continuous-time (CT) incremental sigma-delta (IΣΔ) ADCs, which can expand another dimension of the IΣΔ ADC world that is dominated by discrete-time implementations. Several CT IΣΔ ADC architectures are introduced and analyzed aiming to reduce the modulator's sampling frequency and consequently the power dissipation. Based on the analytical results, three CT IΣΔ ADCs are selected to be examined, implemented, and tested. The three ADC prototypes, fabricated in a standard 0.18 μm CMOS technology, demonstrate competitive figure-of-merits in terms of power efficiency compared to the state-of-the-art counterparts. Copyright © 2015 John Wiley & Sons, Ltd.

Received ...

KEY WORDS: A/D conversion; incremental sigma-delta; continuous-time; extended-range; two-step

1. INTRODUCTION

Incremental sigma-delta (ΣΔ) analog-to-digital converters (ADCs) are commonly used in instrumentation and biosensor applications [1, 2], which typically feature signal bandwidth from kilohertz to megahertz and medium-to-high resolution. Unlike conventional ΣΔ ADCs, the analog loop filter and digital filter in IΣΔ ADCs are reset after oversampling each input sample. As a result, IΣΔ ADCs can offer sample-by-sample conversion much like Nyquist-rate ADCs. Additionally, comparing to ultra-low-power successive-approximation-register (SAR) ADCs, which feature medium-resolution, IΣΔ ADCs relax the requirements of the analog front-end (AFE) circuitry: the variable-gain amplifier (VGA) can be eliminated, and the active anti-aliasing filter (AAF) can be replaced by a passive filter. During the last decade, different approaches have been proposed to significantly enhance the conversion speed and/or resolution of IΣΔ ADCs. The most popular alternatives are high-order architectures [3, 4, 19]. Other popular alternatives are the extended counting (EC) [5, 6] and the extended range (ER) [2] architectures, which combine the IΣΔ ADC with a low-power Nyquist-rate ADC. The main difference between the two is that in an EC ADC, the IΣΔ ADC hardware is usually reused and reconfigured as a cyclic ADC, while in an ER ADC, the residue of the IΣΔ is processed by another Nyquist-rate ADC. Recent advances in IΣΔ ADCs showcase further improvement in power efficiency, by employing multi-bit quantizers [7, 8], inverter-based integrators [9, 10], and reconfigurable pipelined IΣΔ architectures [11].

So far, discrete-time (DT) implementations have been the primary focus of the IΣΔ ADC design. Only a few continuous-time (CT) prototypes have been reported in literature, including the 1st-order CT IΣΔ ADCs used in a temperature sensor [12] as well as in integrated biosensor systems [13, 14], and a 3rd-order CT IΣΔ ADC targeting multi-channel applications[15]. One advantage of

*Correspondence to: Sha Tao and Ana Rusu, KTH Royal Institute of Technology, Isafjordsgatan 22, 16440 Kista, Stockholm, Sweden. Email: stao@kth.se;arusu@kth.se

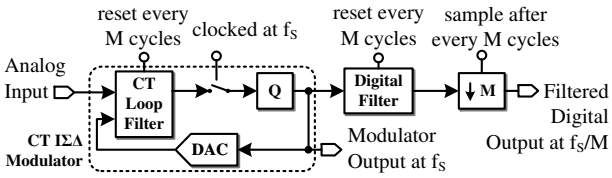


Figure 1. Generic block diagram of a CT IΣΔ ADC.

the CT implementation over its DT counterpart is the implicit anti-aliasing feature [16]. In addition, the CT implementation is much easier to drive since it usually presents a resistive impedance to the preceding stage while its DT counterpart commonly presents a switched capacitor load. This reduces the power consumption of the driver amplifier. Furthermore, the absence of switches in the CT loop filter relaxes the settling and bandwidth requirements of the active blocks, thus potentially leading to reduced power dissipation [17]. On the other hand, CT implementation suffers from several design challenges, such as larger integrator gain error and increased sensitivity to clock jitter compared with its DT counterpart. These performance limiting non-idealities have to be carefully considered so as to take full advantage of CT implementation.

This paper intends to contribute with additional exploration of CT IΣΔ ADCs by: i) analyzing different CT IΣΔ ADC architectures and demonstrating their theoretical resolutions; ii) evaluating the effects of critical circuit non-idealities and discussing the corresponding countermeasures; iii) implementing and testing three power-efficient CT IΣΔ ADCs. The paper is organized as follows. Section 2 presents several CT IΣΔ ADC architectures and compares their theoretical resolutions. The impact of circuit non-idealities is analyzed in Section 3, and the circuit implementation is shown in Section 4. Experimental results of three CT IΣΔ prototype ADCs are presented in Section 5. Finally, Section 6 draws the conclusions.

2. THEORETICAL PERFORMANCE

A generic block diagram of a CT IΣΔ ADC is depicted in Figure 1. Instead of running continuously, the CT IΣΔ modulator is clocked at an oversampling rate of f_S, for M cycles and then its loop filter is reset. The modulator output (at a rate of f_S) is sent to the digital filter. After M cycles, both the loop filter and the digital filter are reset. The final output data rate is at f_S/M, which corresponds to the effective conversion rate. The number of cycles in each conversion, M, is equivalent to the oversampling ratio (OSR) in the ΣΔ ADC.

This study is only limited to the single-bit architecture since it greatly minimizes the digital filter complexity and avoids the need of linearization techniques in the feedback DAC. Moreover, as the objective is to improve power efficiency rather than area efficiency, the first-order and the EC IΣΔ ADCs are excluded from this study. As in conventional ΣΔ ADCs, the resolution of single-bit IΣΔ ADCs can be enhanced by employing a large M or a high-order loop filter, with either single-loop (SL) or multistage noise-shaping (MASH) topologies. The possible implementations of the aforementioned cases are a 2nd-order CT IΣΔ ADC (CT-IΣΔ_{Mod2}) using a large M, a 4th-order SL CT IΣΔ ADC (CT-IΣΔ_{Mod4}), and a 4th-order 2-2 MASH CT IΣΔ ADC (CT-IΣΔ_{MASH22}), illustrated by their respective block diagram in Figs. 2-4. For IΣΔ ADCs with a feed-forward topology, the conversion residue can be obtained directly at the output of the last integrator [1]. This property provides the possibility to reduce the quantization error by digitizing the residue and combining it with the decimated modulator output. This method can be applied to a high-order CT IΣΔ ADC with ER [17] and a two-step CT IΣΔ ADC [18]. The former employs extra SAR A/D conversion cycles to encode the residue from an IΣΔ ADC while the latter pipelines two IΣΔ ADCs, one for coarse conversion, and the other for fine conversion. These two architectures, i.e, a 2nd-order CT IΣΔ ADC with an ER SAR ADC (CT-IΣΔ_{ER}) and a two-step CT IΣΔ ADC (CT-IΣΔ_{2Step}), are illustrated in Fig. 5 and Fig. 6, respectively. In order to evaluate the power efficiency

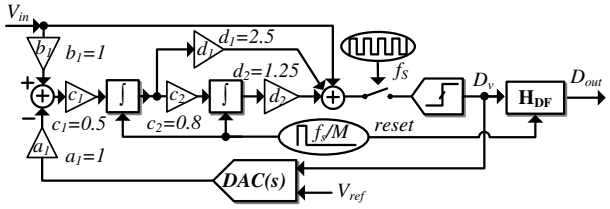


Figure 2. A 2^{nd}-order CT IΣΔ ADC.

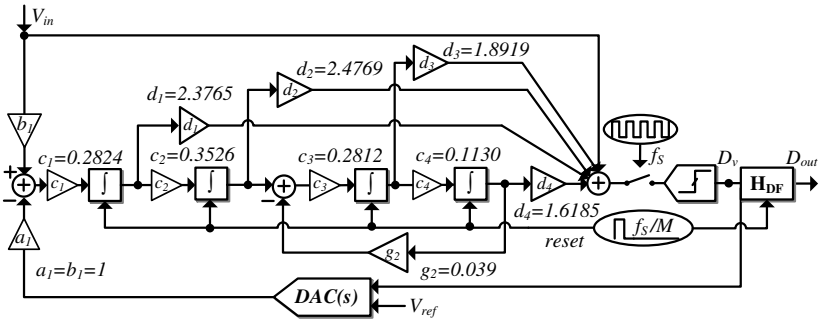


Figure 3. A 4^{th}-order SL CT IΣΔ ADC.

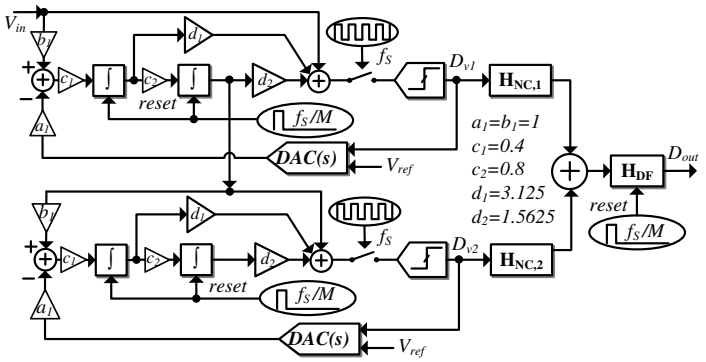


Figure 4. A 4^{th}-order 2-2 MASH CT IΣΔ ADC.

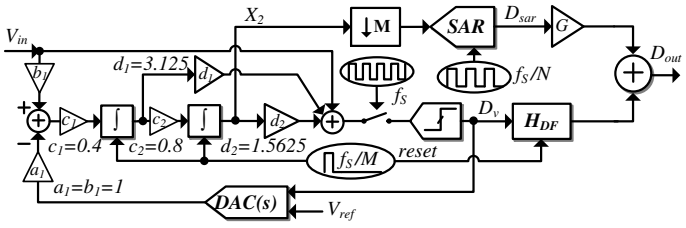


Figure 5. A 2^{nd}-order CT IΣΔ ADC with ER SAR ADC.

of these architectures, their theoretical performance is firstly derived in this section. Additionally, behavioral models are built upon these CT IΣΔ ADC architectures to verify the analytical results. The results would serve as references for choosing the most suitable architectures to be further investigated and implemented.

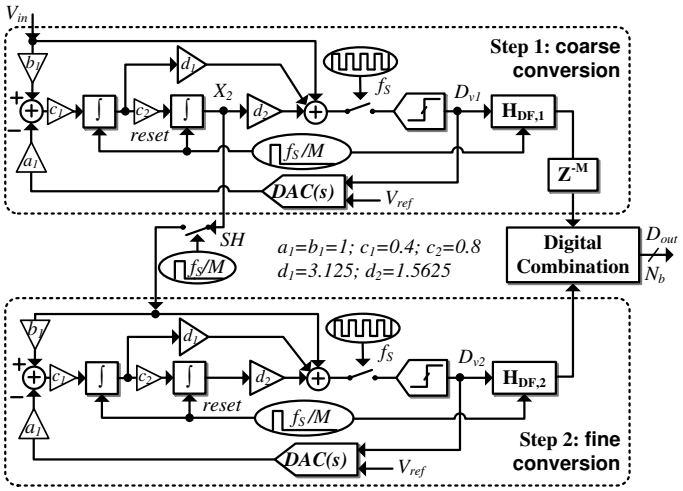


Figure 6. A two-step CT IΣΔ ADC.

To estimate the maximum achievable theoretical resolution of different ADC architectures, time-domain analysis [1, 19] was performed to derive the output of the last integrator after M cycles as well as the quantization error of each conversion. The main differences of CT IΣΔ ADCs with respect to their DT counterparts are the derivation of the loop filter coefficients as well as the design of the digital filter [17]. Detailed theoretical analysis and the associated design methodology of CT IΣΔ ADC architectures can be found in [15, 18]. By assuming the input to be constant or slow-varying during one conversion, the signal-to-quantization noise ratio (SQNR) of the architectures shown in Figs. 2-6, can be expressed as:

$$\begin{aligned}\mathrm{SQNR}_{\mathrm{Mod2}}\ [\mathrm{dB}] &\approx 6.02\log_2\left(u_{max}/2\cdot M(M-1)\right)\\ &\quad + 6.02\log_2\left(c_2c_1b_1\right) + 1.76\end{aligned} \tag{1}$$

$$\begin{aligned}\mathrm{SQNR}_{\mathrm{Mod4}}\ [\mathrm{dB}] &\approx 6.02\log_2(u_{\max}V_{ref}\cdot\frac{(M+4-1)!}{4!(M-1)!}+1)\\ &\quad + 6.02\log_2(b_1c_1c_2c_3c_4d_4/g_2) + 1.76\end{aligned} \tag{2}$$

$$\begin{aligned}\mathrm{SQNR}_{\mathrm{MASH22}}\ [\mathrm{dB}] &\approx 6.02\log_2(u_{\max}V_{ref}\cdot\frac{(M+4-1)!}{4!(M-1)!}+1)\\ &\quad + 6.02\log_2(b_1c_1c_2) + 1.76\end{aligned} \tag{3}$$

$$\mathrm{SQNR}_{\mathrm{ER}}\ [\mathrm{dB}] \approx 20\log_{10}(\sqrt{\frac{3}{2}}M^2) + 20\log_{10}(b_1c_1c_2) + B_{ER} \tag{4}$$

$$\begin{aligned}\mathrm{SQNR}_{\mathrm{2Step}}\ [\mathrm{dB}] &\approx 20\log_{10}\left[\frac{2V_{ref}}{u_{max}V_{ref}}\frac{1}{M(M-1)}\right]\\ &\quad + 20\log_{10}\left[\frac{2V_{ref}}{V_{res,peak}}\frac{1}{M(M-1)}\right]\end{aligned} \tag{5}$$

where $V_{res,peak}$ denotes the peak amplitude of the residue voltage; V_{ref} is the DAC reference voltage; u_{max} is used to limit the input to a fraction of V_{ref}; and B_{ER} is the number of bits in the SAR ADC for the ER conversion. The digital filter transfer function, $H_{DF}(z)$, for each ADC architecture can be derived as:

$$H_{DF}^{Mod2}(z) = \frac{2!}{M^2}\left(\frac{z^{-1}}{1-z^{-1}}\right)^2 \tag{6}$$

$$H_{DF}^{ER}(z) = \left[\frac{z^{-2}}{(1-z^{-1})^2} + \frac{1}{2}\frac{z^{-1}}{1-z^{-1}}\right]\frac{2}{M^2} \tag{7}$$

$$H_{DF}^{Mod4}(z) = \frac{4!}{M^4}\left(\frac{z^{-1}}{1-z^{-1}}\right)^4 \tag{8}$$

$$\begin{aligned} H_{NC,1}^{MASH22}(z) &= z^{-1}\cdot z^{-1} \\ H_{NC,2}^{MASH22}(z) &= \frac{1}{2}\frac{1}{c_1c_2}(1-z^{-1})^2 \end{aligned} \tag{9}$$

$$\begin{aligned} H_{DF,S1}^{2Step}(z) &= \left[\frac{z^{-2}}{(1-z^{-1})^2} + \frac{1}{2}\frac{z^{-1}}{1-z^{-1}}\right]\frac{2}{M(M-1)} \\ H_{DF,S2}^{2Step}(z) &= \frac{2!}{M^2}\left(\frac{z^{-1}}{1-z^{-1}}\right)^2 \end{aligned} \tag{10}$$

After the decimation and digital combination, the final digital output, D_{out}, of each ADC architecture, can be expressed as:

$$D_{out}^{Mod2} = D_v(M)\cdot H_{DF}^{Mod2} \tag{11}$$

$$D_{out}^{Mod4} = D_v(M)\cdot H_{DF}^{Mod4} \tag{12}$$

$$D_{out}^{MASH22} = [D_{v1}(M)\cdot H_{NC,1} + D_{v2}(M)\cdot H_{NC,2}]\cdot H_{DF}^{Mod4} \tag{13}$$

$$D_{out}^{ER} = D_v(M)\cdot H_{DF}^{ER} + G\cdot D_{sar},\ \text{where } G = \frac{1}{a_1c_1c_2} \tag{14}$$

$$D_{out}^{2Step} = \frac{2^{N_b/2}D_{v1}(M)\cdot H_{DF,s1}^{2Step} + D_{v2}(M)\cdot H_{DF,s2}^{2Step}}{2^{N_b/2}} \tag{15}$$

Matlab/Simulink simulations are performed on these architectures while different values of M are employed. The simulated signal-to-quantization-noise ratios (SQNRs) are shown in Figure 7. For comparison, the theoretical SQNRs calculated from (1)-(5) are also plotted. For the CT-I$\Sigma\Delta_{\text{ER}}$, two different resolutions are used for the ER conversion: B_{ER} = 6 and 8 bits. Both resolutions can be easily achieved by a low-power SAR ADC. Figure 7 reveals that the analytical estimations agree well with the simulation results. Figure 7 also shows that the CT-I$\Sigma\Delta_{\text{Mod2}}$ needs a much larger M to achieve a certain SQNR than others, but it requires the minimum analog hardware and a simpler digital filter. With regard to the high-order SL architecture, i.e., the CT-I$\Sigma\Delta_{\text{Mod4}}$, the conversion goes faster. However, its loop filter coefficients (c_1-c_4) need to be scaled down significantly to maintain stability, especially when employing a single-bit quantizer. This translates to a substantial reduction in the maximum achievable SQNR, according to (2). The CT-I$\Sigma\Delta_{\text{MASH22}}$ alleviates the stability problem by employing a cascaded structure to implement a 4$^{\text{th}}$-order noise shaping. However, the effectiveness of the noise shaping in CT ΣΔ MASH architectures suffers from high sensitivity to integrator gain errors, as these coefficients are present in the noise cancellation logics, e.g., c_1 and c_2 in (9). As for CT-I$\Sigma\Delta_{\text{ER}}$, the 8-bit case requires the smallest M when the SQNR is less than 90 dB, with the addition of an ultra-low-power SAR ADC. When the SQNR goes above 90 dB, the CT-I$\Sigma\Delta_{\text{2Step}}$ takes over, and becomes the most efficient solution. Although the CT-I$\Sigma\Delta_{\text{2Step}}$ requires more hardware than the other alternatives, it can provide high-resolution without sacrificing the conversion rate.

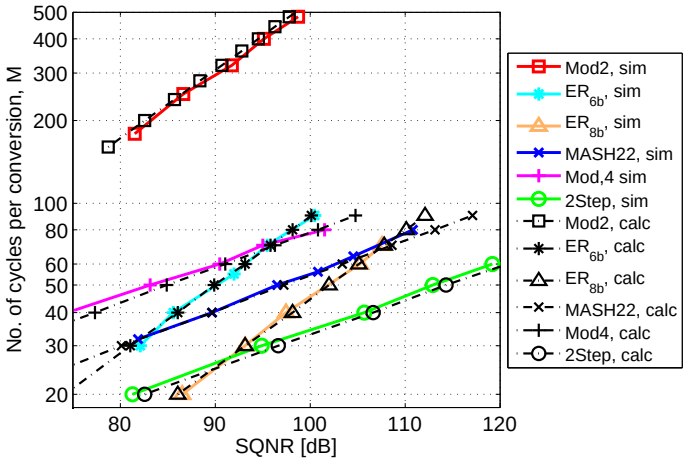


Figure 7. Required number of cycles per conversion, M, as a function of the calculated SQNRs (dashed lines) and the simulated SQNRs (solid lines).

3. NON-IDEAL BEHAVIOR

So far, the architectures have been studied under ideal conditions. This section investigates the impact of circuit non-idealities. According to the previous discussion, CT-I$\Sigma\Delta_{\text{Mod2}}$ leads to minimum circuit complexity, CT-I$\Sigma\Delta_{\text{ER}}$ (B_{ER} = 8 bit) potentially consumes the lowest power, and CT-I$\Sigma\Delta_{\text{2Step}}$ is the most efficient when a high resolution is desired. These three architectures are thus selected for further investigation and implementation. The implementation case studies target a typical biosensor application that features a 14-bit dynamic range (DR) and a 4 kHz signal bandwidth (BW). To leave sufficient margins to account for the effects of circuit non-idealities, M = 40 is selected for CT-I$\Sigma\Delta_{\text{ER}}$ and CT-I$\Sigma\Delta_{\text{2Step}}$, while M = 320 is chosen for CT-I$\Sigma\Delta_{\text{Mod2}}$. The resultant clock frequencies are $f_S = 320$ kHz and $f_S = 2.56$ MHz.

The effect of non-idealities in the feedback DAC is firstly evaluated. The sensitivity to clock jitter is studied by simulating the signal-to-noise and distortion ratio (SNDR) over various standard deviation, σ_j, of the clock period. In such a low-speed application, the excess loop delay (ELD) does not play a dominant role [20]. A fixed ELD of $t_d = 1\%T_S$, which can be easily achieved by a latched comparator using standard CMOS technologies, is introduced to the jittered DAC waveform. Figure 8 shows the simulated SNDRs under the influence of clock jitter, in which the different effects on the first and second stage of the CT-I$\Sigma\Delta_{\text{2Step}}$ are presented separately. The jitter induced timing error would give rise to the in-band noise floor, which limits the maximum performance of these architectures. The maximum allowable jitter values of different architectures depend on both the in-band quantization noise and the jitter induced in-band noise. Clock jitter starts to take effect when the architecture's SNR is limited by the jitter induced white noise rather than the noise-shaped quantization noise. The jitter induced in-band noise is proportional to σ_j^2, and inversely proportional to M [20]. According to Figure 8, to achieve a 14-bit resolution, a σ_j of $0.01\%T_S$ is allowed for CT-I$\Sigma\Delta_{\text{ER}}$ and CT-I$\Sigma\Delta_{\text{2Step}}$ (stage 1), and a σ_j of $0.03\%T_S$ is required for CT-I$\Sigma\Delta_{\text{Mod2}}$. For the CT-I$\Sigma\Delta_{\text{2Step}}$ (stage 2), no noticeable performance degradation is observed for $\sigma_j \leq 0.1\%T_S$. Note that the absolute jitter tolerance of CT-I$\Sigma\Delta_{\text{Mod2}}$ is actually tougher than the other two, since its clock frequency is 8 times greater.

The non-idealities in the integrators are modeled assuming an active-RC implementation. The impact of process variation is evaluated by introducing a random variation, Δ_{RC}, in the integrator scaling coefficients, c_1 and c_2. The impact of Δ_{RC} can be regarded as modifying the ideal transfer function of each integrator by a gain error, which in turn modifies the aggressiveness of the NTF. The tolerable gain error induced by Δ_{RC} depends on the number of cycles per conversion, M, the order of the respective modulator, and the conversion step of the ADC (in the case of CT-I$\Sigma\Delta_{\text{ER}}$ and CT-I$\Sigma\Delta_{\text{2Step}}$). For the CT-I$\Sigma\Delta_{\text{Mod2}}$, the simulation results shown in Figure 9 (a) indicate that a

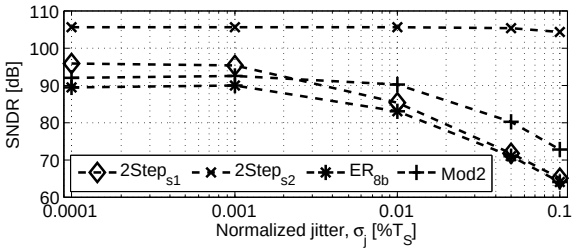


Figure 8. Simulated SNDR of CT-IΣΔ_{Mod2}, CT-IΣΔ_{ER}, and CT-IΣΔ_{2Step} versus clock jitter with a fixed ELD of $1\%T_S$.

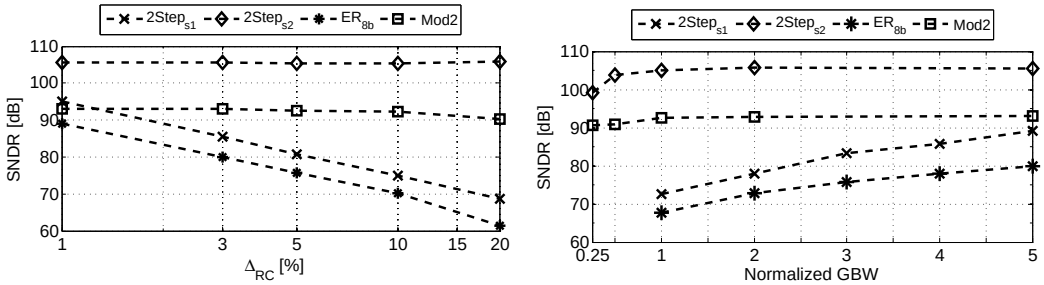


Figure 9. Simulated SNDRs of CT-IΣΔ_{Mod2}, CT-IΣΔ_{ER}, and CT-IΣΔ_{2Step} under the influence of (a) integrator coefficient variation, (b) amplifier finite GBW. Both amplifiers in each modulator are of the same GBW. The RC products in each modulator are assumed to suffer from the same spread.

coefficient tuning circuit may not be necessary, as there is no significant SNDR degradation when the coefficient variation rises up to 20%. It is worth mentioning that the RC product is assumed to suffer from the same spread. A more realistic estimation can be obtained from Monte-Carlo simulations at transistor level. The CT-IΣΔ_{ER} and the first stage of CT-IΣΔ_{2Step}, on the other hand, are sensitive to coefficient variation. Without digital calibration, this indicates that high-precision tunning circuitry ($\leq$1% accuracy) is needed for both architectures.

Single-pole models are used to simulate the amplifier finite gain-bandwidth product (GBW), with a dominant pole at ω_P and a DC gain of A_{DC}. The impact of finite GBW corresponds to adding a gain error as well as an additional pole into the integrator transfer function. The finite GBW induced gain error has similar effect as the integrator coefficient variation discussed previously. So its impact on the ADC's SNDR performance should be similar to the one presented in Figure 9 (a). The effect of the additional non-dominant pole would increment the order of the respective loop filter. Its impact is not as critical as the gain error. As shown in Figure 9 (b), when the normalized GBW is larger than $0.25f_S$, there is no degradation in the SNDR of the CT-IΣΔ_{Mod2}. The same applies to the impact on the SNDR perfromance of CT-IΣΔ_{2Step} due to the finite GBW of the amplifiers in its second stage. On the contrary, when the normalized GBW is less than $5f_S$, the SNDR of CT-IΣΔ_{ER} cannot meet the target DR requirement. Similarly, the finite GBW of the amplifiers in the first stage of CT-IΣΔ_{2Step} affect the overall SNDR performance of the ADC. Compared to the CT-IΣΔ_{Mod2}, the f_S in both the CT-IΣΔ_{ER} and CT-IΣΔ_{2Step} is much lower, however, it does not translate into a relaxed GBW requirement.

For the CT-IΣΔ_{ER} and CT-IΣΔ_{2Step}, the performance degradation due to finite GBW and coefficient variation can be explained by the mismatch between the analog and digital transfer functions. Therefore, digital calibration is required in both cases. In [17], an optimized noise cancellation (NC) filter was developed for a 3$^{\text{rd}}$-order CT ER IΣΔ ADC to alleviate the noise leakage when using large number of bits in the ER conversion. By applying the optimized NC filter, as shown in Figure 10 (a) and (b), the CT-IΣΔ_{ER}'s sensitivity to coefficient variation and finite GBW is considerably reduced. For the CT-IΣΔ_{2Step}, the correction techniques proposed in

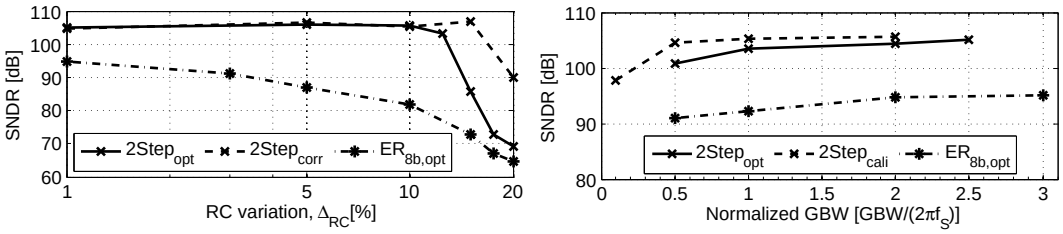


Figure 10. Simulated SNDRs of CT-I$\Sigma\Delta_{\text{ER}}$ and CT-I$\Sigma\Delta_{\text{2Step}}$ under the influence of (a) integrator coefficient variation with calibration and (b) amplifier finite GBW with calibration.

[21] are first applied to counteract the gain errors induced by the coefficient variation and the finite GBW. Specifically, a digital correction term, $corr_{RC} = 1/(g_{err,RC_{11}} \times g_{err,RC_{12}})$, is added to the combination logic of the two-step ADC to compensate for coefficient variation. The gain errors induced by the coefficient variation of the two integrators in the coarse conversion stage are:

$$g_{err,RC_{11}} = g_{err,RC_{12}} = \frac{1}{1+\Delta_{RC}}, \tag{16}$$

where both RC products are assumed to suffer from the same spread. The weighted combination in (15) thus becomes:

$$D_{out}^{2Step,corr} = corr_{RC} \cdot D_{v1}(M) \cdot H_{DF,S1}^{2Step} + \frac{D_{v2}}{2^{N/2}} \cdot H_{DF,S2}^{2Step}. \tag{17}$$

The SNDR versus RC variation after applying this technique is shown in Figure 10 (a), as the curve labeled 2Step$_{\text{corr}}$. Similarly, to compensate for the finite GBW, a gain term, $k_{cali} = 1/g_{err,GBW}$ is added at each integrator to adjust the signal transfer function accordingly, where,

$$g_{err,GBW} = \frac{GBW}{GBW + (a_1c_1 + b_1c_1 + c_2)}. \tag{18}$$

Figure 10 (b) shows, as the curve labeled 2Step$_{\text{cali}}$, the SNDR versus finite GBW, when this calibration technique is applied in the coarse conversion stage. These two error correction/calibration methods, however, have their limitations. One practical issue in the RC variation correction technique is the difficulty in detecting the gain error with high-precision from a real-world measurement setup. The finite GBW calibration technique, on the other hand, works only under the condition that a single-pole gain error model is used for each integrator. Due to the aforementioned limitations, a less deterministic method, adapted from the one in [17] is applied so as to compensate for the impacts of finite GBW and RC variation. The main idea is to employ the built-in Matlab "global optimization algorithms" [22] to refine the SNDR performance. These algorithms find the optimal digital filter coefficients when non-idealities are considered. Compared to many deterministic methods presented in the literature, this alternative is more flexible and can be used at different levels of the design flow. Figure 10 shows that when the optimal filter is used in the coarse conversion stage, the CT-I$\Sigma\Delta_{\text{2Step}}$ can take better advantage of the two-step conversion with more relaxed requirements for the circuit blocks.

The effect of finite DC gain has also been evaluated. The finite DC gain would shift the pole of the integrator transfer function, which in turn degrades the noise shaping performance. The required DC gain depends on M, modulator order, aggressiveness of the NTF, as well as the location of the integrator. Figure 11 shows the simulated SNDR versus the amplifer finite DC gain. It can be seen that a DC gain as low as 20-30 dB can be allowed in the second stage of CT-I$\Sigma\Delta_{\text{2Step}}$, while a DC gain of 60 dB is not sufficient for the CT-I$\Sigma\Delta_{\text{Mod2}}$ to achieve the target DR. For the CT-I$\Sigma\Delta_{\text{ER}}$ and the first stage of CT-I$\Sigma\Delta_{\text{2Step}}$, the aforementioned optimal digital filter is needed so as to greatly relax the DC gain requirements. It is worth mentioning that when other non-idealities, e.g., circuit noise and harmonic distortion, are taken into consideration, the minimum allowable DC gain will increase.

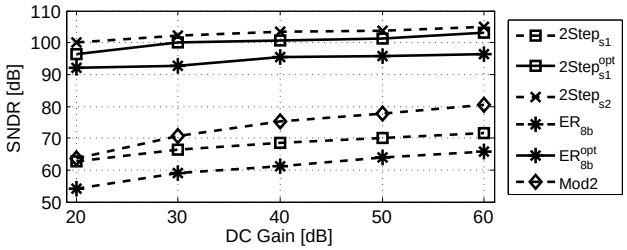


Figure 11. Simulated SNDR of CT-IΣΔ$_{\text{Mod2}}$, CT-IΣΔ$_{\text{ER}}$, and CT-IΣΔ$_{\text{2Step}}$ under the influence of amplifier finite DC gain. Both the amplifiers in each modulator are of the same DC gain.

Table I. Specifications of circuit blocks in CT-IΣΔ$_{\text{Mod2}}$, CT-IΣΔ$_{\text{ER}}$, and CT-IΣΔ$_{\text{2Step}}$ for 14-bit resolution.

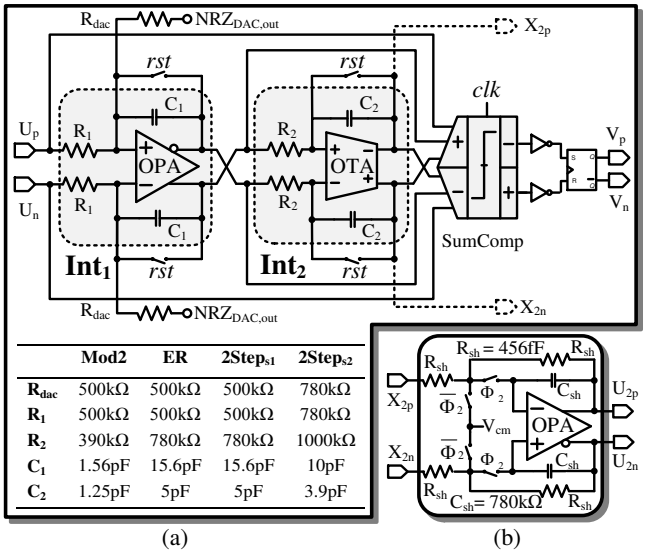
IΣΔ$_{\text{Mod2}}$	
f_S	2.56 MHz
Circuit Noise	1 μV_{rms}
GBW/$(2\pi f_S)$	[1, 0.5]
RC Variation	$\leq$30%
DC Gain [dB]	[80, 60]
Clock Jitter	$\leq 0.03\% T_S$

IΣΔ$_{\text{ER}}$		SAR$_{\text{ER}}$	
f_S	320 kHz	f_{SAR}	$\frac{f_S}{40} \times N$
Circuit Noise	1 μV_{rms}	Circuit Noise	1 μV_{rms}
GBW/$(2\pi f_S)$	[2, 1]	Comparator Offset	0.1 mV
RC Variation	$\leq$ 5%	DAC Slew Rate	$2f_{SAR}$
DC Gain [dB]	[50, 40]	DAC Bandwidth	$3f_{SAR}$
Clock Jitter	$\leq 0.01\% T_S$	Clock Cycles, N	13

IΣΔ$_{\text{2Step}}$	IΣΔ$_{\text{2Step}_{s1}}$	IΣΔM$_{\text{2Step}_{s2}}$
f_S	320 kHz	320 kHz
Circuit Noise	1 μV_{rms}	9 μV_{rms}
GBW/$(2\pi f_S)$	[1, 0.5]	[0.5, 0.3]
RC Variation	$\leq$ 10%	$\leq$ 20%
DC Gain [dB]	[50, 30]	[30, 20]
Clock Jitter	$\leq 0.01\% T_S$	$\leq 0.1\% T_S$

4. CIRCUIT IMPLEMENTATION

Prior to circuit implementation, behavioral simulations have been performed in Cadence using Verilog-A models for the three CT IΣΔ ADCs. As a result, Table I summarizes the specifications of the building blocks in each ADC architecture, in order to achieve a 14-bit resolution. The aforementioned calibration techniques have been applied to the CT-IΣΔ$_{\text{ER}}$ and CT-IΣΔ$_{\text{2Step}}$. The schematics of the 2$^{\text{nd}}$-order CT IΣΔ modulator used in three ADCs and the SH in the CT-IΣΔ$_{\text{2Step}}$ are shown in Figure 12. Active-RC integrators are used for better linearity, larger signal swing and less sensitivity to parasitics compared to their G$_{\text{m}}$C counterparts. The integrating resistors and capacitors are sized by considering both the thermal noise limitations as well as the loading condition of the amplifiers. The capacitors in the SH are sized considering the trade-off among accuracy, settling and loading conditions. For flexibility, the digital filters, the combination logic, as well as the SAR ADC are implemented in Matlab. The digital filter benchmark and its implementation details can be found in [23]. The modeled non-idealities of the SAR ADC in the CT-IΣΔ$_{\text{ER}}$ are shown in Table I. In order to counteract the non-idealities in the DAC, i.e, the finite slew rate and bandwidth, extra clock cycles are allocated for the SAR A/D conversion to compensate for the inadequate settling. In the case of the 8-bit SAR ADC, for instance, four clock cycles are added to correct the most-significant bits $b_7 - b_4$, resulting in $1 + 8 + 4 = 13$ clock cycles per conversion.



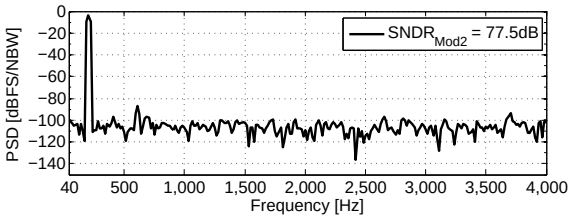
	Mod2	ER	2Steps1	2Steps2
R_{dac}	500kΩ	500kΩ	500kΩ	780kΩ
R_1	500kΩ	500kΩ	500kΩ	780kΩ
R_2	390kΩ	780kΩ	780kΩ	1000kΩ
C_1	1.56pF	15.6pF	15.6pF	10pF
C_2	1.25pF	5pF	5pF	3.9pF

Figure 12. Schematics of (a) the 2nd-order CT IΣΔ modulator and (b) the SH in the CT-IΣΔ_{2Step}. The X_2 (dashed lines), are sampled for the SAR conversion (in the CT-IΣΔ_{ER}) and for the fine conversion (in the CT-IΣΔ_{2Step}).

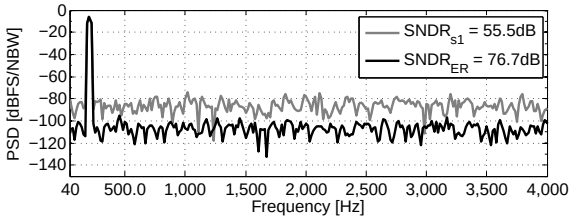
As shown in section 3, the circuit non-idealities in the first stage of the CT-IΣΔ_{ER} and CT-IΣΔ_{2Step} limit the overall performance. The first integrator also dominates the noise and linearity performance of the entire ADC. Therefore, a two-stage Class-A/Class-AB low noise amplifier [18] is used for the 1st Opamp in both ADCs. The output stage operates in the Class-AB mode, and therefore the peak transient current delivered to the capacitive load can be much larger than the quiescent current. A two-stage Miller compensated Opamp is used in the 1st integrator of both the CT-IΣΔ_{Mod2} and the CT-IΣΔ_{2Step} (fine conversion stage) as well as in the inter-stage SH of the CT-IΣΔ_{2Step}. With less capacitive loading and better noise shaping in the loop filters, the amplifiers in the 2nd integrators of all the modulators are implemented by a current mirror OTA. The bias currents in different amplifiers are adjusted to meet the corresponding specifications for GBW, DC gain, and slew-rate. For each CT IΣΔ modulator, the weighted addition of feed-forward paths is implemented with no additional power and area by reusing the input stage of a two-stage dynamic comparator [18]. The integrator outputs and the ADC input are connected to the comparator through three differential pairs, which are added in current. The weights in the current addition, which correspond to the feed-forward coefficients, are implemented by sizing the input transistors with different W/L ratios. Figure 13 shows the post-layout simulation results of the three ADCs implemented as they are described in this section. It can be seen that an SNDR of 77.5 dB, 76.7 dB and 79.2 dB is obtained from a post-layout simulation with transient noise activated for the CT-IΣΔ_{Mod2} ADC, CT-IΣΔ_{ER} ADC and CT-IΣΔ_{2Step} ADC, respectively.

5. EXPERIMENTAL RESULTS

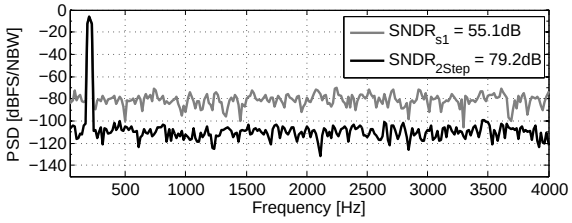
The three CT IΣΔ ADCs were fabricated on a single chip using a $0.18\ \mu m$ CMOS technology. The analog circuitry is powered by a 1.2 V supply. A 1.8 V digital supply is used as only 1.8-3.3V digital I/Os are available. Three samples of the prototype chip are assembled into three evaluation boards (EVBs) shown in Figure 14. In the case of CT-IΣΔ_{ER}, only the 2nd-order CT IΣΔ modulator and the on-chip analog buffers were fabricated. As for the 8-bit SAR ADC, an area of $0.3\ mm^2$ is estimated according to [25], in which a SAR ADC was implemented in the same technology node. A power consumption of $0.85\ \mu W$ at 8 kS/s is also estimated for the 8-bit SAR ADC according to [25].



(a)



(b)



(c)

Figure 13. Post-layout transient noise simulation results: PSDs of (a) the CT-IΣΔ$_{Mod2}$ ADC, (b) the CT-IΣΔ$_{ER}$ ADC and (c) the CT-IΣΔ$_{2Step}$ ADC.

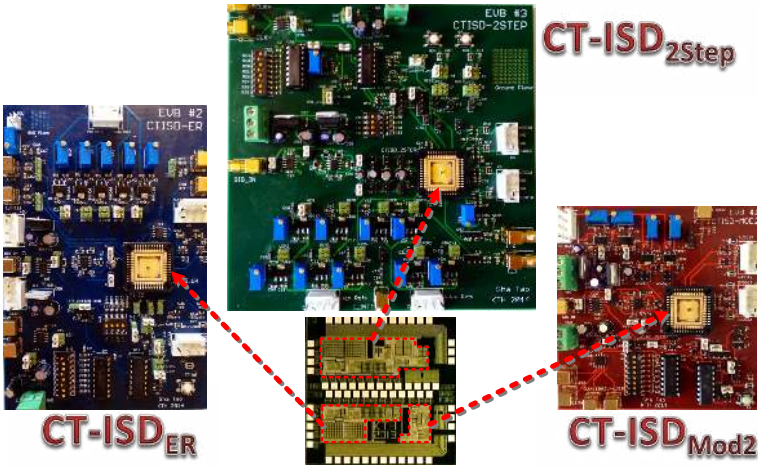


Figure 14. Chip micrograph and photos of the EVBs.

5.1. Test Setup

The signal conditioning blocks are similar among the three measurement setups. The input test signal is processed by a single-ended to differential conversion buffer to drive the differential inputs of the ADC. In addition, a RC filter is placed between the buffer and the ADC so as to reduce the noise contributed by the driving circuits.

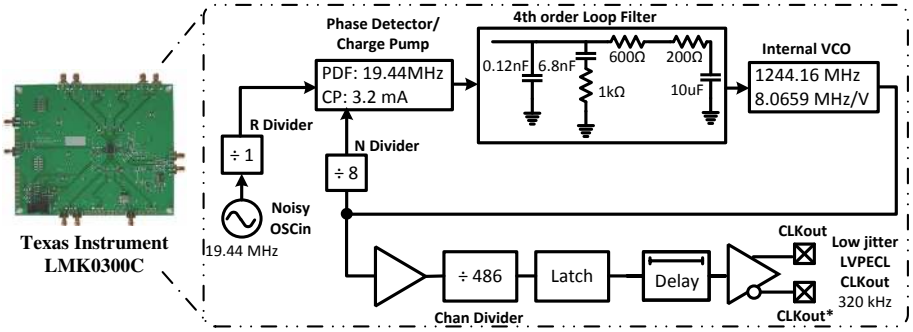


Figure 15. Clock conditioning block for low jitter master clock generation.

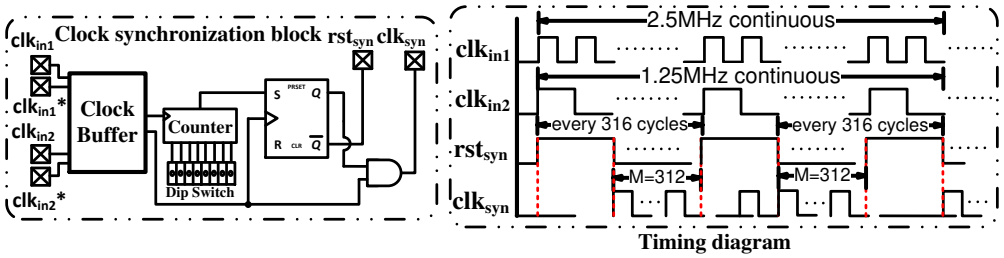
The main difference among the test setups lies in the clock conditioning and synchronization blocks that are used to generate the clock and reset signals for the chip operations. To make sure that the ADCs' performance are not limited by clock jitter, a phase-locked-loop (PLL) in combination with a voltage-controlled oscillator (VCO) is used to condition a noisy clock signal. This is done by configuring a precision clock conditioner (LMK03000C [24]) differently so as to generate the low jitter master clock signals for each of the setup. For instance, Figure15 illustrates the configuration for generating a low jitter 320 kHz clock. Different clock synchronization blocks, using the generated low jitter signals as master clocks, are implemented with discrete components on the EVBs. These blocks, shown in Figure 16, are used to supply the clock and reset signals required for the chip operations.

The data acquisition and post-processing for each measurement setup is described in brief as follows. 1) CT-I$\Sigma\Delta_{\text{Mod2}}$: The modulator output, v, and the reset signal, rst, are firstly captured by a logic analyzer, and then imported into Matlab for digital filtering and post-processing (FFT and windowing); 2) CT-I$\Sigma\Delta_{\text{ER}}$: The 2$^{\text{nd}}$ integrator's output, X_2, used for the ER conversion, is buffered by a high-precision differential to single-ended amplifier whose output is then connected to an oscilloscope through a coaxial cable. Both the digital signals (v and rst_{syn}) and the buffered analog output are synchronized and sampled by the oscilloscope using the oversampling clock, clk_{in}. The sampled data are then imported into Matlab in order to perform the SAR A/D conversion, digital filtering, and post-processing; 3) CT-I$\Sigma\Delta_{\text{2Step}}$: The digital output data streams, i.e., modulators outputs (v_1 and v_2), oversampling clocks (clk_1 and clk_2), as well as the reset signals (rst_1 and rst_2) are captured by the logic analyzer. These data streams are then imported into Matlab where they are processed by the digital filters and combination logic.

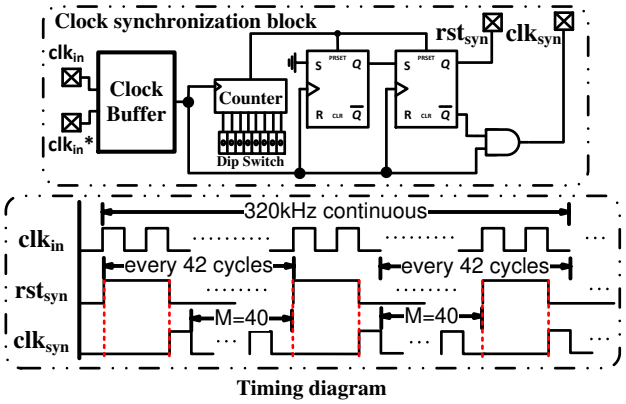
5.2. *Measurement Results*

The measured PSDs of the three prototype ADCs are shown in Figure 17 for a 0.68 V_{pp} sinusoidal input at 171.1 Hz. A 1024-point fast Fourier transform (FFT) using Blackman-Harris window is applied to compute the PSDs. These PSD plots have been used to measure the spurious-free dynamic range (SFDR) and the peak SNDR presented in Table II. The DR presented in Table II has been estimated from the SNDR versus input amplitude plot shown in Figure 18. Additionally, Figure19 demonstrates that the peak SNDRs do not suffer significant degradation over in-band frequencies. The measured performance is summarized in Table II. As the SAR ADC was not implemented on-chip, a power consumption of 0.85 μW at 8 kS/s is estimated for the 8-bit SAR ADC according to [25]. When comparing the measured SNDRs with the post-layout transient noise simulation performance presented in Figure 13, there is around 3.8 dB degradation in all three cases. Further inspection on the EVBs revealed that the buffer amplifier preceding the ADC was most likely the main cause for the increment in the ADC's noise floor.

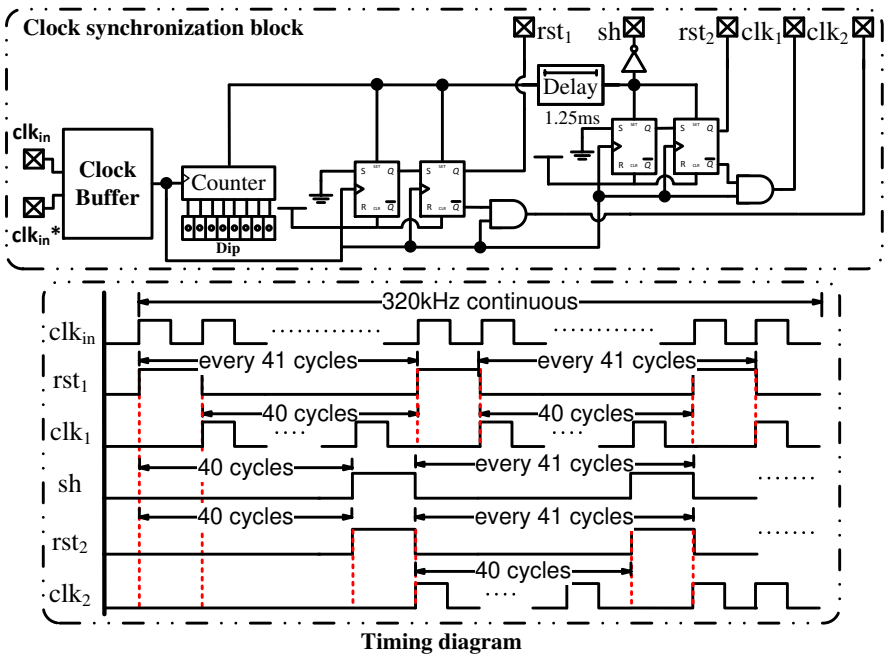
A comparison of the CT I$\Sigma\Delta$ ADCs in this work with the existing I$\Sigma\Delta$ prototype ADCs is shown in Figure 20. All the existing CT I$\Sigma\Delta$ ADCs and some representative DT I$\Sigma\Delta$ ADCs have been included in this comparison. Note that only in [3] the power consumption of the digital filter is



(a)



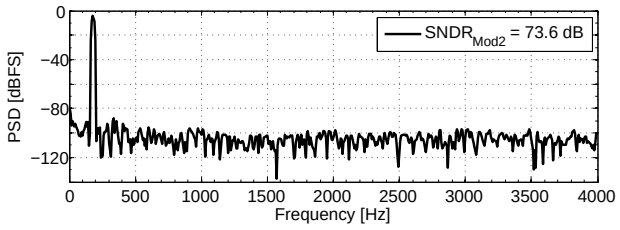
(b)



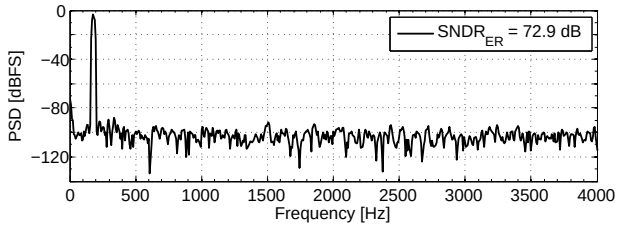
(c)

Figure 16. Clock synchronization blocks and the timing diagrams of (a) the CT-IΣΔ$_{Mod2}$ ADC, (b) the CT-IΣΔ$_{ER}$ ADC and (c) the CT-IΣΔ$_{2Step}$ ADC.

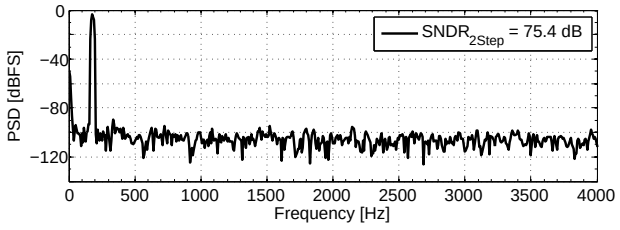
included. As shown in Figure 20, the three implemented CT IΣΔ ADCs improve noticeably the FOMs of existing CT IΣΔ ADCs. In addition, the achieved FOM of the three prototype ADCs are competitive among different types of state-of-the-art IΣΔ ADCs.



(a)



(b)



(c)

Figure 17. Measured PSDs of (a) the CT-I$\Sigma\Delta_{Mod2}$ ADC, (b) the CT-I$\Sigma\Delta_{ER}$ ADC and (c) the CT-I$\Sigma\Delta_{2Step}$ ADC, for inputs at 171.1 Hz.

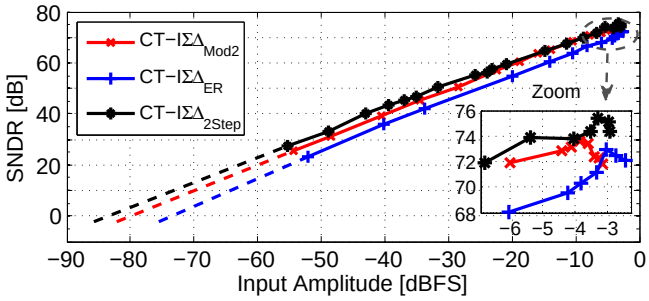


Figure 18. Measured SNDR versus input amplitude with a 171.1 Hz input tone. For inputs below -55 dB$_{FS}$ the curves are extrapolated.

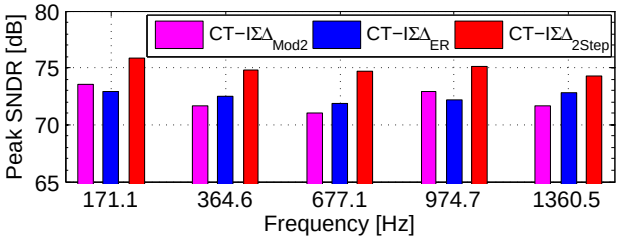


Figure 19. Measured SNDR over various in-band test frequencies.

Table II. Summary of Measured Performance

	CT-IΣΔ$_{\text{Mod2}}$	CT-IΣΔ$_{\text{ER}}$	CT-IΣΔ$_{\text{2Step}}$
Signal Bandwidth	4 kHz	4 kHz	4 kHz
Clock Frequency	2.5 MHz[a]	320 kHz	320 kHz
DR	80.13 dB	77.56 dB	85.74 dB
SFDR	84.34 dB	85.24 dB	85.96 dB
peak SNDR	73.60 dB	72.93 dB	75.42 dB
Power [μW]	50.88	29.45+0.85[b]	34.80
Active Area [mm^2]	0.06	0.20+0.30[c]	0.33
FOM [dB][d]	152.56	154.14	156.03

[a] A rounded 2.5 MHz clock frequency (instead of 2.56 MHz) was used due to the limited sampling resolution of the logic analyzer.
[b] A 0.85 μW consumption is estimated for the SAR ADC [25].
[c] The area of the 8-bit SAR ADC is estimated as 0.30 mm^2 [25].
[d] FOM[dB] = SNDR$_{\text{peak}}$[dB] + 10log($\frac{\text{BW}}{\text{Power}}$) [26].

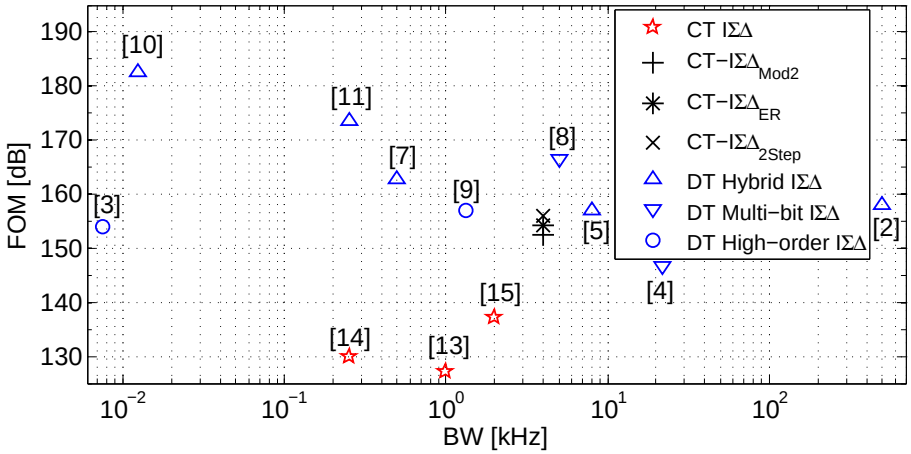


Figure 20. FOM comparison with state-of-the-art IΣΔ ADCs.

6. CONCLUSION

This paper investigated different CT IΣΔ ADC architectures. To improve the resolution beyond that achievable with the first-order IΣΔ ADC, several single-bit CT IΣΔ ADC architectures have been presented and compared with respect to their power efficiency. Based on the theoretical results, the 2$^{\text{nd}}$-order CT IΣΔ ADC, the ER CT IΣΔ ADC and the two-step CT IΣΔ ADC, have been selected as implementation case studies. Critical non-idealities have been investigated to evaluate their impact on the performance of the three CT IΣΔ ADCs. These three ADCs have been implemented, fabricated and measured. The competitive FOMs achieved by the three prototype ADCs demonstrate that they are promising candidates for low-power medium-high resolution applications.

ACKNOWLEDGEMENT

This work has been funded by Swedish Research Council (VR).We would like to thank Saul Rodriguez from KTH, Martin Gustafsson from Maxim Integrated and Julian Garcia from Bombardier for their extensive support and advices regarding the chip implementation and measurement issues. We also appreciate Håkan Bengtsson, Giti Amozandeh and Mikael Pettersson K from Ericsson AB for valuable discussions and comments during the design review. In addition, we want to acknowledge Agilent Technologies and Texas Instruments for supplying the necessary lab equipment and evaluation board.

REFERENCES

1. J. Markus, J. Silva, G.C. Temes, Theory and applications of incremental ΔΣ converters, IEEE Trans. Circuits Syst. I Regul. Pap. 51 (2004) 678–690.
2. A. Agah, K. Vleugels, P. Griffin, M. Ronaghi, J.D. Plummer, B. A.Wooley, A High-Resolution Low-Power Incremental ΣΔ ADC With Extended Range for Biosensor Arrays, IEEE J. Solid-State Circuits. 45 (2010) 1099–1110.
3. V. Quiquempoix, P. Deval, A. Barreto, G. Bellini, J. Mrkus, J. Silva, et al., A low-power 22-bit incremental ADC, IEEE J. Solid-State Circuits. 41 (2006) 1562–1571.
4. W. Yu, M. Aslan, G.C. Temes, 82 dB SNDR 20-Channel Incremental ADC with Optimal Decimation Filter and Digital Correction, in: IEEE Cust. Integr. Circuits Conf., 2010: pp. 1–4.
5. P. Rombouts, W. De Wilde, L. Weyten, A 13.5-b 1.2-V micropower extended counting A/D converter, IEEE J. Solid-State Circuits Solid-State Circuits. 36 (2001) 176–183.
6. L. Rossi, S. Tanner, P.-A. Farine, Performance analysis of a hybrid incremental and cyclic A/D conversion principle, IEEE Trans. Circuits Syst. I Regul. Pap. 56 (2009) 1383–1390.
7. A. Agnes, E. Bonizzoni, F. Maloberti, High-resolution multi-bit second-order incremental converter with 1.5-μV residual offset and 94-dB SFDR, Analog Integr. Circuits Signal Process. 72 (2012) 531–539.
8. Y. Liu, E. Bonizzoni, A. D´Amato, F. Maloberti, A 105-dB SNDR, 10 kSps multi-level second-order incremental converter with smart-DEM consuming 280 μW and 3.3-V supply, in: IEEE Eur. Solid State Circuits Conf., 2013: pp. 371–374.
9. C. Chen, Z. Tan, M. Pertijs, A 1V 14b self-timed zero-crossing-based incremental ΔΣ ADC, in: IEEE Int. Solid-State Circuits Conf., 2013: pp. 274–276.
10. Y. Chae, K. Souri, K. Makinwa, A 6.3 μW 20 bit Incremental Zoom-ADC with 6 ppm INL and 1 μV Offset, IEEE J. Solid-State Circuits. 48 (2013) 3019–3027.
11. C. Chen, Y. Zhang, T. He, P.Y. Chiang, G.C. Temes, A Micro-Power Two-Step Incremental Analog-to-Digital Converter, IEEE J. Solid-State Circuits. 50 (2015) 1796–1808.
12. A. Bakker, J.H. Huijsing, Micropower CMOS temperature sensor with digital output, IEEE J. Solid-State Circuits. 31 (1996) 933–937.
13. M. Mollazadeh, K. Murari, G. Cauwenberghs, N. Thakor, Micropower CMOS Integrated Low-Noise Amplification, Filtering, and Digitization of Multimodal Neuropotentials, IEEE Trans. Biomed. Circuits Syst. 3 (2009) 1–10.
14. Y.M. Chi, G. Cauwenberghs, Micropower Integrated Bioamplifier and Auto-ranging ADC for Wireless and Implantable Medical Instrumentation, in: Eur. Solid State Circuits Conf., 2010: pp. 334–337.
15. J. Garcia, S. Rodriguez, A. Rusu, A Low-Power CT Incremental 3rd Order ΣΔ ADC for Biosensor Applications, IEEE Trans. Circuits Syst. I, Reg. Pap. 60 (2013) 25–36.
16. M. Ortmanns, F. Gerfers, Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations, Springer Verlag, 2006.
17. J. Garcia, S. Rodriguez, A. Rusu, On Continuous-Time Incremental Sigma-Delta ADCs with Extended Range, IEEE Trans. Instrum. Meas. 62 (2013) 60–70.
18. S. Tao, A. Rusu, A Power-Efficient Continuous-Time Incremental Sigma-Delta ADC for Neural Recording Systems, IEEE Trans. Circuits Syst. I Regul. Pap. 62 (2015) 1489-1498.
19. J. Markus, Higher-order Incremental Delta-Sigma Analog-to-Digital Converters, Ph.D. dissertation, Budapest University of Technology and Economics, 2005.
20. S. Tao, S. Rodriguez, A. Rusu, DAC Waveform Effects in CT Incremental ΣΔ ADCs for Biosensor Applications, in: IEEE Int. New Circuits Syst. Conf., 2013: pp. 1–4.
21. M. Ortmanns, F. Gerfers, Y. Manoli, A Case Study on a 2-1-1 Cascaded Continuous-Time Sigma-Delta Modulator, IEEE Trans. Circuits Syst. I Regul. Pap. 52 (2005) 1515–1525.
22. Mathworks, MATLAB R2013a fmincon documentation, 2013. http://www.mathworks.com/help/optim/ug/fmincon.html.
23. J. Garcia, Digitally Enhanced Continuous-Time Sigma-Delta Analogue-to-Digital Converters, Ph.D. dissertation, KTH Royal Institute of Technology, 2012.
24. Texas Instruments, LMK03000 Family Precision Clock Conditioner with Integrated VCO, 2013. http://www.ti.com/lit/ds/symlink/lmk03000.pdf.
25. J.-H. Tsai, H.-H. Wang, Y.-J. Chen, Y.-H. Wei, Y.-H. Kao, Y.-C. Yen, et al., A 1V-to-0.6V 9-bit 1.5-MS/s Reference-free Charge-sharing SAR ADC for Wireless-powered Implantable Telemetry, IEEE Trans. Circuits Syst. II Express Briefs. 61 (2014) 825–829.
26. R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters. New York: Wiley, 2005.

