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Research Article

A Comparative Study of Symmetrical Cockcroft-Walton Voltage Multipliers

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Decades after invention of the Cockcroft-Walton voltage multiplier, it is still being used in broad range of high voltage and ac to dc applications. High voltage ratio, low voltage stress on components, compactness, and high efficiency are its main features. Due to the problems of original circuit, reduction of output ripple and increase of accessible voltage level were the motivations for scientist to propose new topologies. In this article a comparative study on these voltage multipliers was presented. By simulations and experimental prototypes, characteristics of the topologies have been compared. In addition to the performances, components count, voltage stress on the components, and the difficulty and cost of construction are other factors which have been considered in this comparison. An easy to use table which summarized the characteristics of VMs was developed, which can be used as a decision mean for selecting of a topology based on the requirements. It is shown that, due to the application, sometimes a simple and not very famous topology is more effective than a famous one.

1. Introduction

High voltage dc power supplies are widely used for many applications, such as particle accelerators, X-ray systems, electron microscopes, photon multipliers, electrostatic systems, lasers systems, and electrostatic coating [1–5]. There are several approaches in producing high voltage dc sources depending on the desired voltage and current levels. A more usual choice when a power supply with high voltage and low current is needed is the Cockcroft-Walton voltage multiplier (CWVM). High voltage ratio, low voltage stress on the diodes and capacitors, compactness, and high efficiency are the main reasons for this choice [3, 5, 6]. Furthermore it can be used in medium voltage applications when the current is low and simple circuit is the matter, like portable pulsed power applications and handheld devices [7–9]. The CWVM has the unique characteristic of imposing equal voltage stresses on every stage. Its construction is also simple and easy to implement [10]. Usually, in modern types of voltage multipliers there are three stages; a high frequency inverter which produces fast dynamic voltage source with controllable duty cycle to control the current and voltage level, a transformer, and a CW voltage multiplier [11]. In this article only the topologies of VMs, regardless of inverter construction, are studied.

Historically the original idea was proposed by Greinacher in 1921. However, it did not get attention for a long time until Cockcroft and Walton performed their experiment using this circuit in 1932 [12]. Large output voltage ripple and output voltage drop were the main problems of the original half-wave voltage multiplier. Consequently, to overcome these problems, a symmetrical voltage multiplier (SVM) was developed by Heilpern in 1954 by adding an extra oscillating column of capacitors and a stack of rectifiers [1, 13] Because voltage ripple in a half-wave rectifier due to the charge and discharge of capacitors has almost a triangular-like shape, by using two voltage sources with 180° phase difference, the overall voltage ripple magnitude can be reduced greatly. If the ripple was an isosceles triangle shaped waveform, the opposite phase could exactly cancel out the voltage peaks so that the voltage ripple would be disappeared in the output voltage. However, this is not the case, so the ripple will not be removed completely, and the result is only reduction of ripple amplitude. This is the main feature of a symmetrical voltage multiplier. Based on

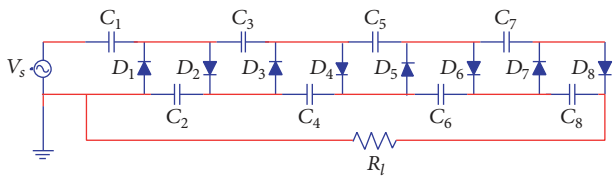

Figure 1: Schematic circuit of a basic 4-stage Cockcroft-Walton voltage multiplier.

this idea, recently a three-phase symmetrical voltage multiplier with six oscillating columns and one smoothening column has been proposed [2, 14]. Furthermore, there are other topologies which based on this idea have lower voltage ripple compared to the conventional one, which will be studied in this article. Other types of voltage multipliers based on CWVM have been developed recently which a CWVM is fed by a matrix converter [6]. The matrix converter generates an adjustable frequency and adjustable-amplitude current, which is injected into the CWVM to regulate the dc output voltage and smooth its ripple. However, in this article, the CWVM is the subject, regardless of how it may be fed.

The comparison of these VMs is important because selecting a topology for an application due to many factors involved is not a straightforward task. The range of output voltage level, necessary safety factors, ground-returned or bipolar output, and speed of response and so on are the main factors which should be considered in such selection. To the best of author's knowledge, until now such comparison has not been made.

This paper is organized as follows. The mathematical model of the CWVM is reviewed in Section 2. Symmetrical voltage multipliers are introduced in Section 3. Comparisons between the symmetrical VMs by simulation are presented in Section 4. In Section 5 experimental low voltage prototypes are constructed to justify the results of simulations. Finally conclusion is given in Section 6.

2. Basic Voltage Multiplier

Figure 1 shows a basic 4-stage Cockcroft-Walton voltage multiplier circuit. It consists of two capacitor columns, namely, oscillating and smoothening columns. Oscillating column capacitors (C_1, C_3, C_5, and C_7) are charged in half cycle by upward odd numbered diodes (D_1, D_3, D_5, and D_7, respectively) and in next half cycle the smoothening column capacitors (C_2, C_4, C_6, and C_8) are charged by downward even numbered didoes (D_2, D_4, D_6, and D_8). In steady state, in no-load condition, every capacitor in smoothening column is charged to $2V_{\max}$, that is, two times of maximum input voltage magnitude. Therefore, the maximum value of output voltage is $2nV_{\max}$ in which n is the number of multiplier stages (here $n = 4$).

However, this is not the case in presence of a load, which output voltage ripple exists and there is a drop in voltage due to the load current. To be clear, in Figure 2, simulation result of a basic half-wave Cockcroft-Walton voltage multiplier circuit, by Saber Synopsys software, is given. In the figure, the key parameters have been shown: ΔV_o is the voltage drop

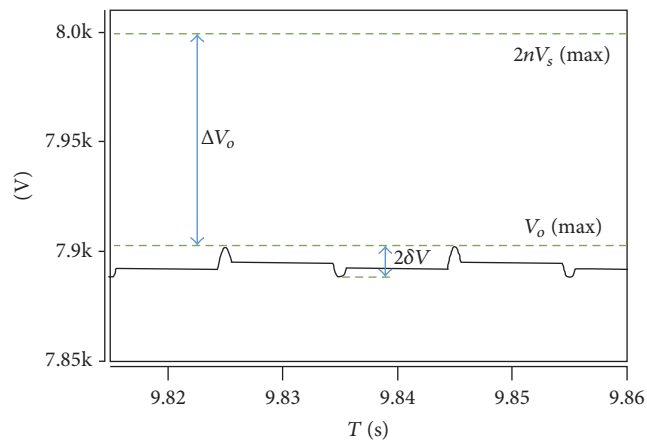

Figure 2: Simulation of a conventional 4-stage ($2n = 8$) Cockcroft-Walton voltage multiplier output voltage. In this example V_s(max) = 1000 V and capacitors are 1000 μF.

compared to the ideal case and $2\delta V$ is the peak-to-peak value of output voltage ripple due to the load current. To calculate the voltage ripple, we should consider the voltage ripple on every capacitor in smoothening column due to the load current. Let q be the charge transferred from C_{2n} to the load per cycle with a ripple voltage at capacitor C_{2n} [15–17]:

$$2\delta V_{2n} = \frac{q}{C_{2n}}. \tag{1}$$

Simultaneously C_{2n-2} transfers charge q to the load and q to C_{2n-1}. So the voltage ripple at capacitor C_{2n-2} is

$$2\delta V_{2n-2} = \frac{2q}{C_{2n-2}}. \tag{2}$$

By intuition,

$$2\delta V_{2n-2i} = \frac{(i+1)\,q}{C_{2n-2i}}. \tag{3}$$

Because ripples on all smoothening capacitors are in-phase, the total voltage ripple on load can be calculated by summation of all ripples values; that is,

$$2\delta V = q\left(\frac{1}{C_{2n}} + \frac{1}{C_{2n-2}} + \cdots + \frac{1}{C_2}\right). \tag{4}$$

Equal value capacitors (C) results in

$$2\delta V = \frac{q}{C}\left(\frac{n(n+1)}{2}\right) = \frac{I}{fC}\left(\frac{n(n+1)}{2}\right), \tag{5}$$

in which I is the load current and f is the frequency of input voltage. In addition to the voltage ripple, there is a voltage drop compared to no-load condition which is the consequences of uncompleted charging process of capacitors. From (3) it can be understood that C_2 loses nq charge during each cycle, so capacitor C_1 has to replenish it. Therefore, C_1 and C_2 charge up to (V_s(max) $- nq/CJ$) and ($2V_s$(max) $- nq/q$)

instead of $V_s(\max)$ and $2V_s(\max)$, respectively. In the same manner the voltage drop in all smoothening capacitors could be calculated. In general we will have [15]

$$\begin{aligned}\Delta V_2 &= \frac{q}{C}n,\\ \Delta V_4 &= \frac{q}{C}\left[2n + (n-1)\right],\\ &\vdots\\ \Delta V_{2n} &= \frac{q}{C}\left[2n + 2(n-1) + \cdots + 2\times 2 + 1\right].\end{aligned} \tag{6}$$

Adding all n voltage drops gives the total voltage drop on load:

$$\begin{aligned}\Delta V_{\text{total}} &= \frac{q}{C}\left(\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{n}{6}\right)\\ &= \frac{I}{fC}\left(\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{n}{6}\right).\end{aligned} \tag{7}$$

Recently with more detailed analysis it has been shown that the above formula needs a small correction [18]. However the difference is of secondary importance for practical use, because it does not concern the leading order in n. From (7) and (5) it is clear for a given value of n, by increasing load current, voltage drop and voltage ripple increase proportionally. To compensate this effect the value of $f \times C$ should be increased. Usually increasing frequency has lower cost compared to increasing the capacitors values. Moreover from these relations it is also clear that increasing number of stages will increase these drop voltage and ripple amplitude. Therefore, there is an optimum value for n which gives the maximum accessible output voltage when other parameters are fixed. This optimum value is as follows [13]:

$$n_{\text{opt}} = \sqrt{\frac{V_s(\max)\, fC}{I}}. \tag{8}$$

Hence, the maximum accessible voltage is as follows.

$$\begin{aligned}V_o(\max) &= 2n_{\text{opt}}V_s(\max)\\ &\quad - \frac{I}{fC}\left(\frac{2}{3}n_{\text{opt}}^3 + \frac{1}{2}n_{\text{opt}}^2 - \frac{n_{\text{opt}}}{6}\right).\end{aligned} \tag{9}$$

To exceed the restriction of (9) and also to decrease the output voltage ripple value, several configurations have been proposed which are the subject of next section. It is worth mentioning that a proper selection of nonequal value capacitors ($C_{2i} = C_{2i-1} = (n+1-i)C$) will result in better response compared to the classical case ($C_{2i} = C_{2i-1} = C$) [19]. The result can be extended to the symmetrical cases with minor modifications.

3. Symmetrical Versions of Voltage Multiplier

3.1. Conventional Symmetrical Voltage Multiplier. As mentioned in previous section, by increasing number of stages, the ripple amplitude and drop voltage increase significantly, which make the voltage multiplier inefficient. To solve this problem a symmetrical voltage multiplier (SVM) was developed by Heilpern in 1954 by appending an additional oscillating column of capacitors and a stack of rectifiers [1, 13]. As can be seen in Figure 2, ripple in half-wave CWVM is periodic with almost symmetrical shape relative to horizontal line; that is, peak and valley are almost equal with 180° phase difference. In SVM output voltage is the summation of two waveforms with 180° phase differences. If the shape of ripple was an isosceles triangle or any symmetrical waveform, the summation of two opposite phase could exactly cancel out the peak and valley of ripple. However, in practice, the ripple waveform is slightly distorted due to the discharge pattern or nonlinearity, and its periodical transient shape is formed depending on the time constant of the circuit [20]. Therefore the ripple still exists; however, its magnitude decreases greatly. This is the main reason of lower level of ripple in all symmetrical and multiphase versions of voltage multipliers. In Figure 3, the schematic diagram of a symmetrical voltage multiplier has been given. In fact in SVM, V_{s1} and V_{s2} have same magnitude with no phase difference, so V_{yo} has 180° phase shift related to V_{xo}. In Figure 4 the output voltage ripple for two different conditions has been shown. As can be seen, when V_{yo} and V_{xo} have 180° phase difference, that is, V_{s1} and V_{s2} are in-phase, amplitude of ripple is lower than the case in which V_{yo} and V_{xo} are in-phase.

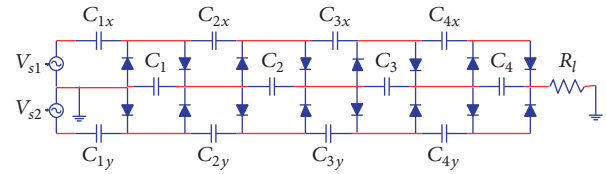

Figure 3: Schematic diagram of a 4-stage SVM.

It is shown that the ripple in symmetrical case compared to the original VM can be reduced approximately by the following formula [20]:

$$\begin{aligned}&2\delta V_s\\ &\cong \frac{I}{Cf}\frac{n(n+1)}{2}\left(1 - \frac{\pi}{4\sin^{-1}\left(\left(V_{\max} - \delta V\right)/V_{\max}\right)}\right),\end{aligned} \tag{10}$$

in which δV_s is the ripple of symmetrical VM and δV is the ripple of conventional VM.

In practice, any kind of asymmetry may result in higher value of ripple. It is known that the asymmetry of both input voltages and circuit elements can cause the ripple [21]. Also the circuit asymmetry causes odd harmonics, while the asymmetry in charge-discharge process of capacitors, which may arise from asymmetry in transformer outputs, causes the even harmonics [5]. For a symmetrical CW circuit, the fundamental harmonic due to the asymmetry of driving voltage is inevitable because of the difficulty of completely removing the symmetry deviation [22].

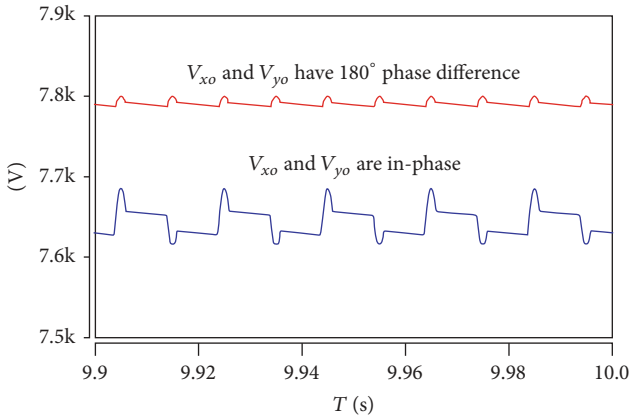

FIGURE 4: Output voltage ripple of a symmetrical voltage multiplier for two cases of in-phase and 180° out of phase power sources.

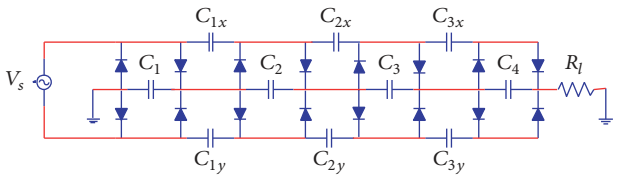

FIGURE 5: Schematic diagram of a 4-stage HSVM.

3.2. Hybrid Symmetrical Voltage Multiplier. Recently a new symmetrical voltage multiplier has been proposed [1]. Figure 5 shows the circuit diagram of 4 stages named Hybrid Symmetrical Voltage Multiplier, HSVM. It consists of a bridge rectifier with capacitor C_1 and a 3-stage SVM. As the proposed topology is a combination of diode-bridge rectifier and SVM, it is named HSVM. The first stage of the proposed topology does not have coupling capacitors; therefore, it saves two high voltage capacitors. This is the main advantage of this topology compared to the conventional SVM. Furthermore, due to its inventor claim, its faster transient response at startup compared with conventional SVM is its other superiority [1]. However, its main problem which makes it less effective is the lack of transformer ground. As can be seen in Figure 5, both x and y terminals are hot and so cannot be grounded. In SVM the center tap of the transformer is grounded; however, for HSVM, this is not the case. The author has not discussed this matter [1]. Due to this problem, in very high voltage applications, HSVM cannot be used for safety issue. In no-load condition we have $V_o = nV_s$. So to have same level of voltage scaling, the amplitude of input voltage which usually is the secondary of a transformer should be twice of that in conventional voltage multiplier. It means, for a given transformer, to have same level of output voltage, the number of elements is about two times of ordinary CWVM. This matter will be discussed in more detail in next sections.

3.3. Series-Connected Voltage Multiplier. As mentioned earlier the main features of a symmetrical voltage multiplier are lower voltage ripple and higher voltage level due to the complementary action of each half section of the multiplier. It means each half section compensates ripple of the other half due to 180° phase differences between the resulting voltage ripples. It is possible to have such condition with two series-connected voltage multipliers. In Figure 6 schematic diagram of such a series-connected voltage multiplier (SCVM) is shown. V_{s1} and V_{s2} usually are secondary windings of a high voltage transformer. With opposite sign of voltage sources, 180° phase difference between sources has been shown. Compared to a conventional one (Figure 1) it has two voltage sources (two secondary windings) and the same number of capacitors and diodes. However, based on previously mentioned symmetrical behavior, it has lower voltage ripple and drop values. Although it should be noticed that the voltage differences between two secondary windings (V_{s1} and V_{s2} in Figure 6) are equal to half of the output voltage and so when the output is a high voltage, this matter should be considered for insulators in construction of the transformer. This is the main problem of this topology that makes it ineffective especially in very high voltage.

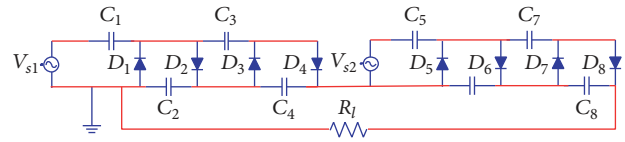

FIGURE 6: Schematic diagram of a series-connected voltage multiplier (SCVM).

Based on this idea, it is possible to build a three-phase (or even higher) VM with cascading three (or more) VMs whose power sources have 120° (360°/number of phases) phase differences with each other. The ripple of such 3-phase VM will be lower than that of two-phase symmetrical VMs. However three separate transformers and several times of components are needed, which make the circuit more costly and bulky [2, 14].

3.4. Series-Connected Positive-Negative Voltage Multiplier (SPNVM). When we cascade two conventional voltage multipliers with 180° out of phase voltage sources as Figure 6, the necessity of high voltage insulation between windings is a problem. Furthermore, compared to the conventional VM, two secondary windings with same voltage amplitude are needed. It is possible to solve this problem by another topology as shown in Figure 7 [23]. As shown, two positive and negative voltage multipliers with opposite direction have been connected in series to build a VM with higher output voltage and reduced ripple value. In this scheme, only one source (one secondary winding) is needed and due to the opposite direction of charge and discharge in positive and negative sections, output voltage ripple of each section compensates those of the other. So the resulting ripple is less than that of conventional VM. Compare to the SVM, this topology has lower number of components and problem of asymmetry of transformer does not exist; consequently the resulting harmonics, as discussed earlier [21, 22], have lower amplitude.

In Figure 7, C_1–C_4 consist of the positive section and C_5–C_8 consist of the negative section of SPNVM. If in this configuration we ground the negative side of the load, it will

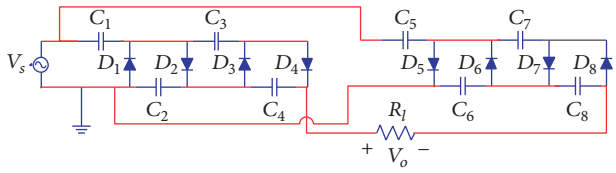

Figure 7: Schematic diagram of a series-connected positive-negative voltage multiplier.

impose a high value dc voltage on the source which usually is a transformer. To avoid this matter, it is better to ground the transformer. Therefore, in this VM, the output is not grounded. This matter restricts this topology to the cases where bipolar output voltage, and not ground-returned one, is needed. Therefore this topology can be used in portable and handheld apparatuses and applications with moderate output voltage, where grounding of load is not nessesary [7, 8].

4. Simulation Results

In this section, by Saber Synopsys software, simulation results of previously discussed VMs are compared. Input voltage and number of stages are chosen to get almost equal output voltage from all VMs. Therefore by consideration of devices count and output specifications of voltage multipliers, comparison is done. Nonideality of the components that are considered in simulations is ESR of capacitors (0.1 Ω), diodes forward voltage drop (0.7 V), input resistance of voltage sources (50 Ω), and inductance of transformer. To shorten the article, simulation results are given only for a case in which the parameters are the same as those for experimental work. It is clear that the operation of the VMs depends on the capacitors value, frequency of operation, number of stages, and load resistor. So, despite the difficulties and cost of high voltage prototypes, in performance comparison, there is no difference between several kilovolts or few volts VMs.

The structure of transformers of VMs is a matter which should be discussed in more detail. Some of the VMs use transformers with two secondary windings, such as SCVM and SVM. If we want to use the same transformer for all VMs, to have the same condition for comparison, a transformer with two secondary windings should be used. Then, in topologies that use one voltage source, series connection of secondary windings could be used. Therefore, for those topologies which need one secondary winding, the voltage would be twice of those with two secondary windings. However, in this case, the stress on components in SVM and SCVM is equal to half of that for other topologies and the number of stages should be doubled to have similar value of output voltage. HSVM also has the same condition and therefore, to decrease the number of stages, a transformer whose secondary voltage is twice of those for BVM and SPNVM could be used. It means there are two choices: first to use the same transformer for all VMs and second to consider the same stress on components. In simulations it is found that SCVM response is almost similar to that of SVM. Furthermore its transformer has the mentioned problem of extra voltage imposed between windings. So in simulations and experiments the SCVM was omitted.

In simulations and experiments, based on abovementioned matter about transformer, two versions of HSVM and SVM are considered. HSVM1 is an eight-stage VM with 10 V input. HSVM2 is a four-stage VM with 20 V input. SVM1 is an eight-stage VM with two 5 V inputs. And SVM2 is a four-stage VM with two 10 V inputs. SPNVM and BVM are four stages with 10 V input. It must be emphasized that the voltage stress on components in topologies depends on the transformer voltage. That is, the magnitude of voltage stress on HSVM1 and SVM1 components is half of that for others. So in components count we should consider this matter. We know that a capacitor with C value and V_b breakdown voltage can be built by four capacitors with C value and $V_b/2$ breakdown voltage, that is, parallel connection of two series-connected ones. Furthermore two diodes with $V_b/2$ breakdown voltage can build a diode with V_b breakdown voltage. Therefore, if the stress on components of VM_1 is twice of that for VM_2, in components count we can consider capacitors and diodes of VM_2 as basic components and multiply the number of capacitors of VM_1 by four and its diodes by two, to find out equivalent number of similar components. With this method we can correctly compare the number of components, that is, the cost of construction. This matter is considered in comparison between VMs. The discussed matter of this paragraph should be understood carefully to know why the proposed comparison in this article is fair.

The frequency of voltage sources (transformers output) is 2 KHz and capacitors in all VMs are 1.6 μF and load is a 51 kΩ resistor. In Figure 8 the transient responses and maximum value of VMs are given. Rise time of VMs was measured according to 10–90% of output voltage by software. We know that speed of VMs especially is an important factor when a VM wanted to be use in pulse mode. The maximum achievable frequency of operation clearly depends on rise time of the VM. As can be seen HSVM2 with highest value of output voltage and SPNVM with fastest response are the best. Furthermore, HSVM1 and SVM1 do not have satisfactory responses compared to others.

Figure 9 shows the ripples of voltage multipliers. It is true that SVM1 has the lowest absolute value of ripple. However if we calculate ratio of ripple to maximum value, that is, ripple factor for all VMs, it can be seen that SPNVM, SVM2, and HSVM2 with 0.007 have the best ripple factor and BVM, as expected, with 0.053 being the worst one.

5. Experimental Comparison

To verify the simulation results, prototypes of VMs have been constructed. BVM, SPNVM, HSVM1, HSVM2, SVM1, and SVM2 have been constructed for comparison. Input is a 2 kHz sinusoidal source with variable amplitude which combined with a ferrite core transformer provides the requested voltages. As in simulation a purely resistive 51 kΩ load is used. Capacitors are in range of 1.62 μF–1.72 μF and have been chosen among many, to be nearly equivalent. Reduction of error produced by nonequal value of capacitors when we compare the topologies was the reason of such selection. In

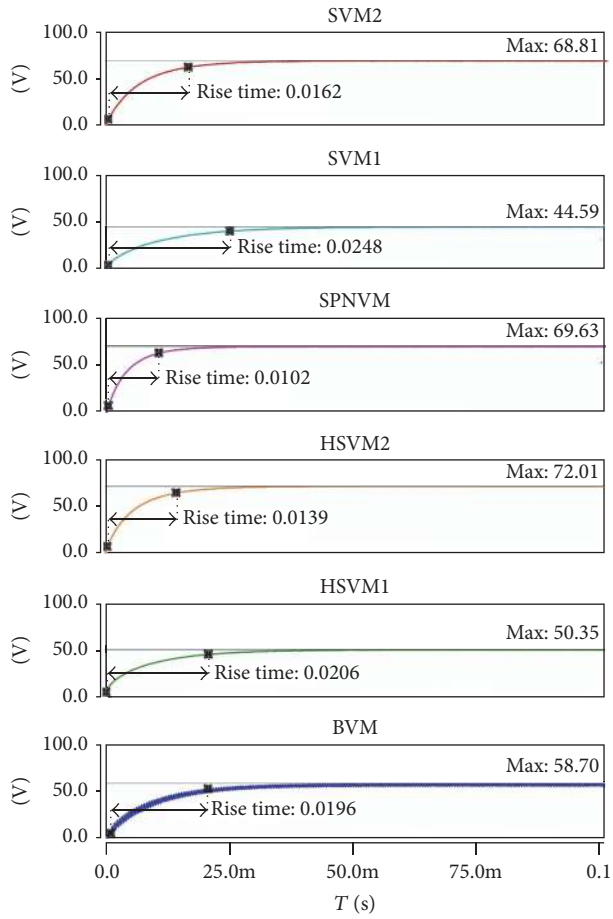

Figure 8: Simulation results: transient and maximum values of output voltages of VMs.

fact, because nonidealities of components have been considered in simulation, experimental prototypes have almost the same specifications as simulation.

In Figure 10, transient responses of VMs are shown. As can be seen SPNVM with a rise time of 14.39 ms has the fastest response and HSVM2 with 18.45 ms is in the second rank. The difference between rise time of VMs in simulation and experiments arises from this fact that the signal generator has a delay in its startup which could not be measured. Maximum output values in steady state are also shown. As simulation, HSVM2 with 70.4 V has the maximum output value.

In Figure 11 variations of VMs are shown. As expected, BVM has maximum peak-to-peak value of ripple with 3.04 V and SPNVM with 456 mV has the lowest value of ripple. By calculation, the ripple factor of SPNVM with 0.006 is the lowest one.

In Table 1 summary of simulation and experimental results are given. Some terms used in the table should be explained. The number of capacitors and diodes in first and second row shows the actual number of components, while base-cap number and base-diode number show the number of components with regard to voltage stress as discussed in simulation section. It means we have considered capacitors and diodes with lowest voltage stress as basic components. Then in VMs with twice voltage stress the number of capacitors is multiplied by four and that of diodes by two. For example, despite the higher actual value of components of HSVM1 relative to HSVM2, its base components number is less. Another term represents wire consumption in transformer construction and is defined as secondary wire factor.

6. Conclusion

Decades after invention of Cockcroft-Walton voltage multiplier, in broad range of high voltage and ac to dc conversion applications, it is still being used and has no competitor. In this paper a review over and a comparison between symmetrical versions of VMs were carried out. The features of different VMs as rise time, ripple, and output voltage are compared to each other with regard to the complexity of the topologies and number of components. In this comparison, some factors as voltage stress on components, number of components, and transformer construction cost are considered. In fact, the voltage stress on components can be used as a factor to evaluate the effective number of components and consequently the price of VMs.

Ground problem of transformer in some VMs makes them ineffective especially in very high voltage usage. However, in mobile apparatus and some low voltage applications, they still can be used. For example, SPNVM with

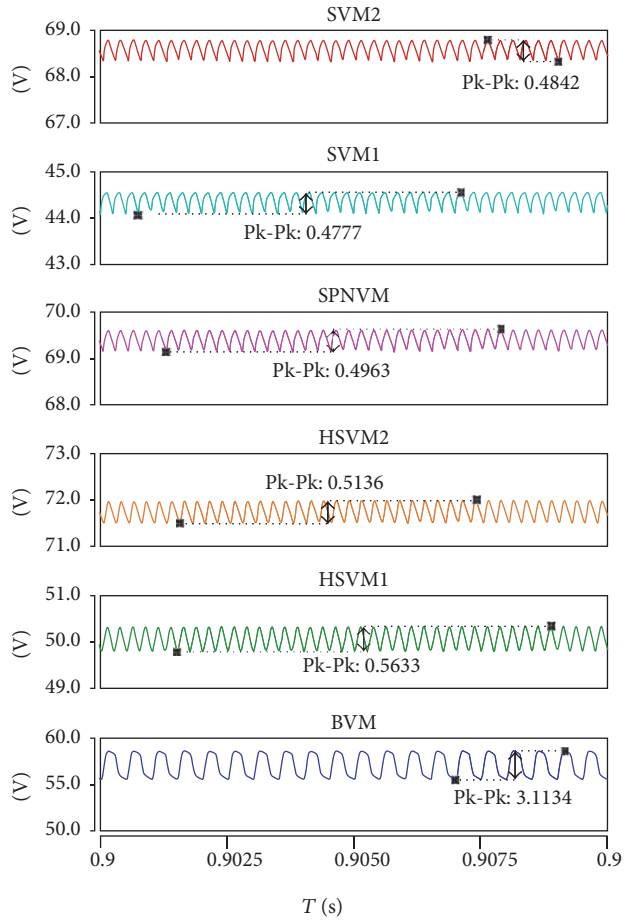

Figure 9: Simulation results: output ripples of voltage multipliers at steady state.

Table 1: Summary of VMs specifications.

Voltage Multiplier		BVM	HSVM1	HSVM2	SPNVM	SVM1	SVM2
Number of capacitors		8	22	10	8	24	12
Number of diodes		8	32	16	8	32	16
Number of secondary windings		one	one	one	one	Two	Two
Transformer windings voltage (V): V_{peak} (V)		10	10	20	10	5	10
Secondary wire factor		1	1	2	1	1	2
Voltage stress on components (V)		20	10	20	20	10	20
Base-cap number		32	22	40	32	24	48
Base-diode number		16	32	32	16	32	32
		Simulation results					
$C = 1.6\,\mu$F $R_l = 51\,k\Omega$ $f = 2$ kHz	V_{max} (V)	58.7	50.35	**72.01**	69.63	44.59	68.81
	Ripple (V)	3.11	0.563	0.513	0.496	0.477	0.484
	Ripple factor*	0.052	0.011	**0.007**	**0.007**	0.010	**0.007**
	Rise time (ms)	19.6	20.6	13.9	**10.2**	24.8	16.2
		Experimental results					
$C = 1.62$–$1.72\,\mu$F $R_l = 51\,k\Omega$ $f = 2$ kHz	V_{max} (V)	57.6	50.4	**70.4**	68.0	44.0	68.0
	Ripple (V)	3.04	0.648	0.500	0.456	0.560	0.480
	Ripple factor	0.052	0.012	0.007	**0.006**	0.012	0.007
	Rise time (ms)	22.7	21.1	18.45	**14.39**	27.32	20.23

*Ratio of ripple magnitude to the maximum output value.

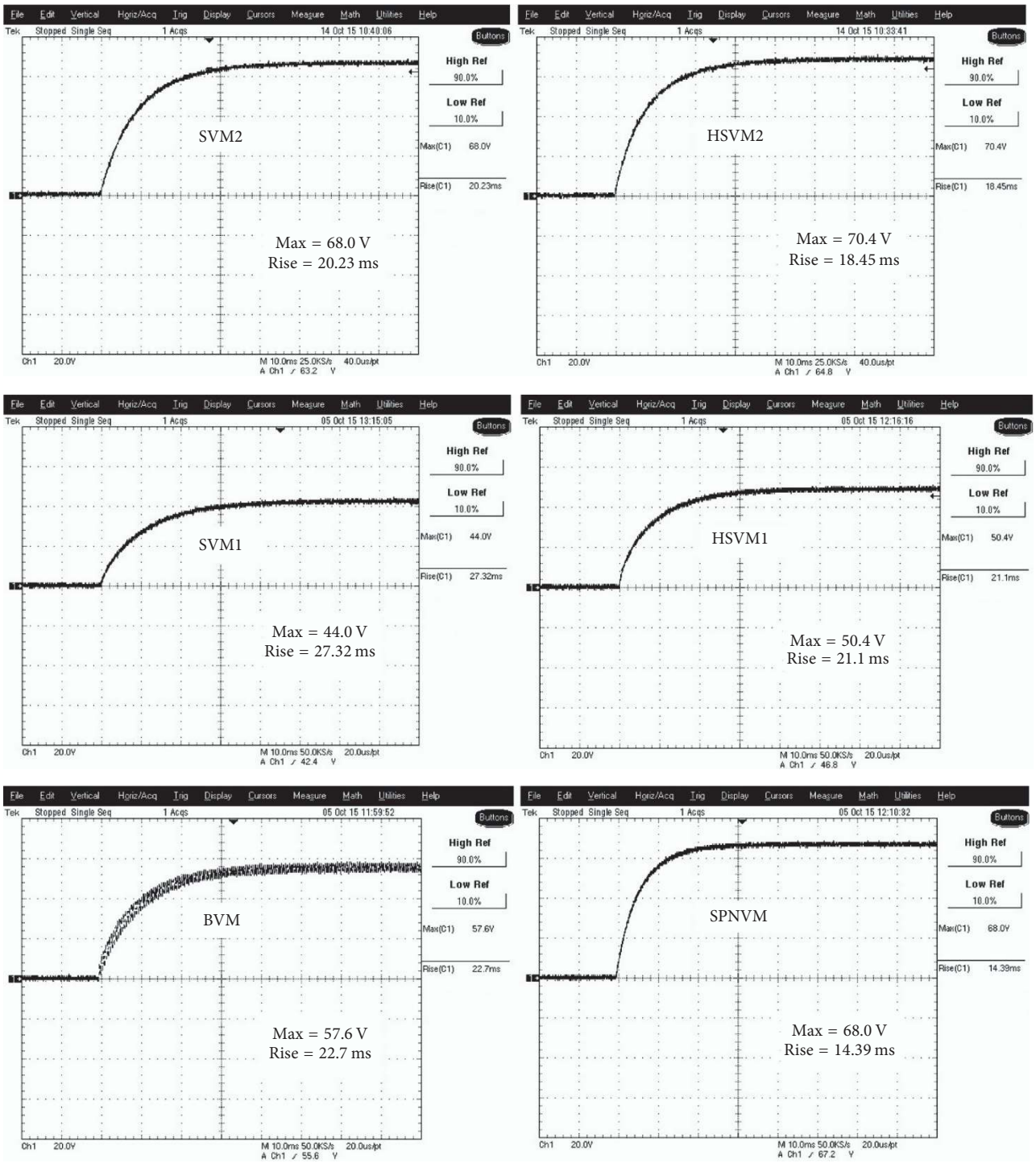

Figure 10: Experimental results: transient responses of VMs. SPNVM with 14.39 ms rise time has the fastest response and HSVM2 with 70.4 V has the maximum output value compared to others.

low components count and acceptable characteristics is an attractive choice which should not be ignored in such applications. With simulations and experimental prototypes, the responses of VMs were compared. The measured values of the prototype's waveforms agreed well with their counterparts simulations. In summary it is not possible to choose one topology as a perfect one. In fact, in each application based on the level of output voltage and therefore components price, with similar method used in Table 1, it is possible to compare the VMs and, therefore, to choose which of them is suitable for the proposed application. Furthermore, with this method, it is possible to understand if a VM has better performance compared to others and how much it costs for designer.

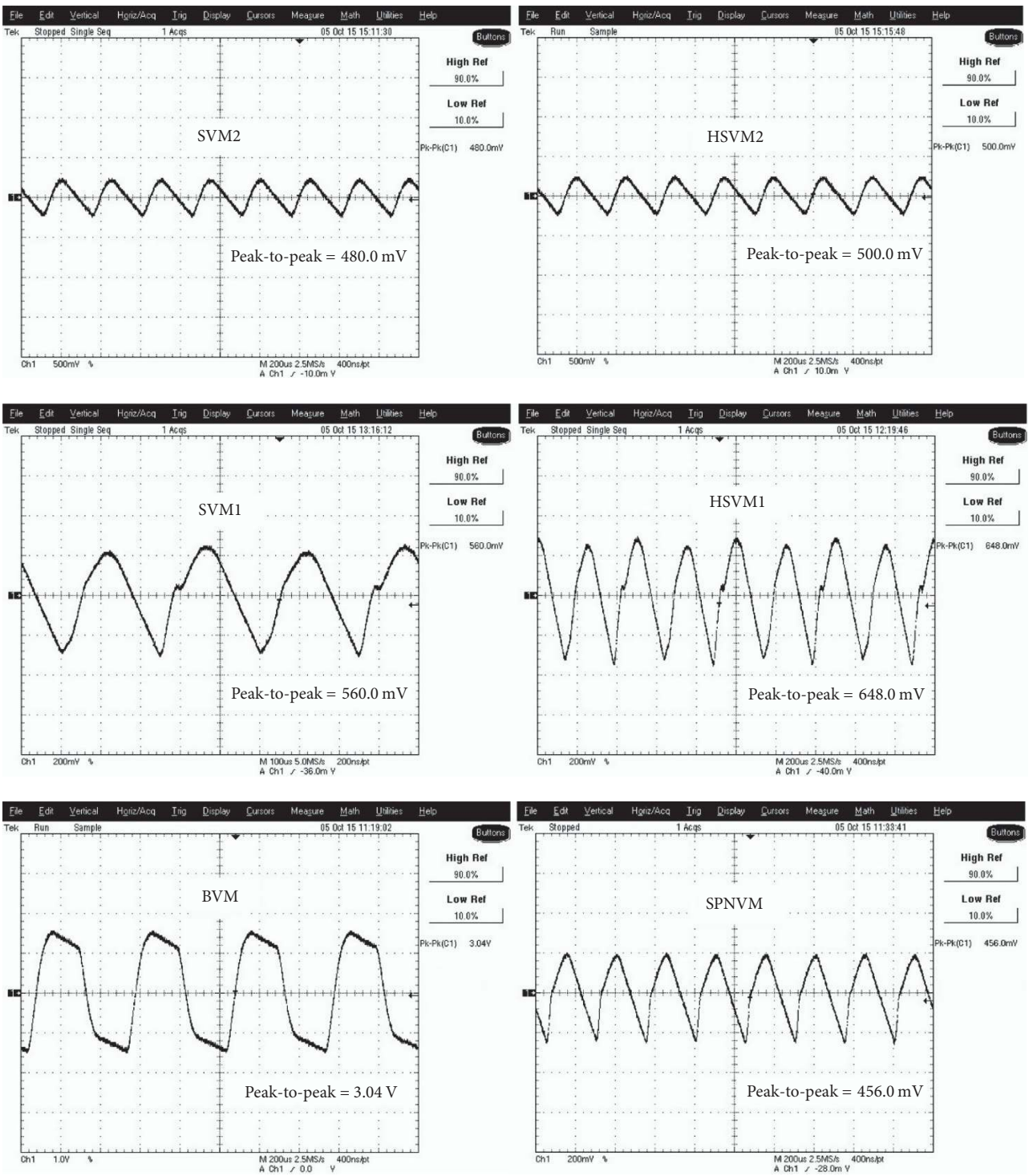

Figure 11: Experimental results: peak-to-peak value of ripple of VMs. SPNVM with 456 mV ripple has the smoothest response compared to others.

Competing Interests

The author declares that there is no conflict of interests regarding the publication of this paper.

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