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A comparative study of the electrical properties of TiO_2 films grown by high-pressure reactive sputtering and atomic layer deposition

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Abstract

Oxide–semiconductor interface quality of high-pressure reactive sputtered (HPRS) TiO_2 films annealed in O_2 at temperatures ranging from 600 to 900 °C, and atomic layer deposited (ALD) TiO_2 films grown at 225 or 275 °C from $TiCl_4$ or $Ti(OC_2H_5)_4$, and annealed at 750 °C in O_2, has been studied on silicon substrates. Our attention has been focused on the interfacial state and disordered-induced gap state densities. From our results, HPRS films annealed at 900 °C in oxygen atmosphere exhibit the best characteristics, with D_{it} density being the lowest value measured in this work (5–6 $\times$ 10^{11} cm^{-2} eV^{-1}), and undetectable conductance transients within our experimental limits. This result can be due to two contributions: the increase of the SiO_2 film thickness and the crystallinity, since in the films annealed at 900 °C rutile is the dominant crystalline phase, as revealed by transmission electron microscopy and infrared spectroscopy. In the case of annealing in the range of 600–800 °C, anatase and rutile phases coexist. Disorder-induced gap state (DIGS) density is greater for 700 °C annealed HPRS films than for 750 °C annealed ALD TiO_2 films, whereas 800 °C annealing offers DIGS density values similar to ALD cases. For ALD films, the studies clearly reveal the dependence of trap densities on the chemical route used.

1. Introduction

Titanium dioxide has been one of the most extensively studied oxides because of its remarkable optical and electrical properties [1–5]. Because of its high dielectric constant, it may be used in thin film capacitors. Also, it may serve as a prototypical alternate gate dielectric for deep-submicron MOSFETs or dynamic random access memory (DRAM) devices if it were accepted by the most modern CMOS fabrication facilities. Studies on thin films of TiO_2 typically report dielectric constants that range from 40 to 86. It is believed that this variability is related to the presence of low-permittivity interfacial layers and to the dependence of permittivity on crystalline phase. Titanium dioxide forms

a number of phases, of which the most common ones are anatase and rutile. The bandgap of the material is reported to be between 3.0 and 3.5 eV, depending on the crystalline phase and purity. The anomalously high permittivity of TiO_2, which arises through a strong contribution from soft phonons involving Ti ions, is not exhibited by the other group IVB metal oxides. On the other hand, Ti has different stable oxidation states of Ti^{3+} and Ti^{4+} which lead to a well-known problem with materials containing Ti–O bonds: a reduced oxide. Such a reduced oxide contains many oxygen vacancies which act as electron donors and high leakage paths [6]. Especially in the case of chemical deposition methods, such as atomic layer deposition (ALD) or chemical vapour deposition (CVD), impurity issues stem from the contamination of the deposited films with residual impurities coming from the nonreacted ligands. If titanium alkoxides are used in the process, excess carbon and hydrogen are found in the films, while in the case of titanium halides (chloride) the resulting films contain some chlorine. Such impurities are responsible for defects additional to the common lattice defects, distorting the oxide lattice, amorphizing the structure and inducing additional trap states in the dielectrics. The impurities can be partially annealed during the post-deposition heat treatments, but in general they serve as complementary sources of disorder-induced traps. Another important concern related to titanium dioxide is the variations in electron effective mass value. Monticone *et al* take the anatase TiO_2 electron effective mass to be equal to $m_e = 10\ m_0$ [7]. On the one hand, Pascual and co-workers obtained $m_e = 3\ m_0$ [8], whereas on the other hand Stamate recently reported a value of $m_e = (0.71–1.26)\ m_0$ [9].

As for deposition techniques, high-pressure reactive sputtering (HPRS) [10] is a combined physical and chemical deposition method in which the chamber pressure is several (two or three) order of magnitude higher than it usually is in other sputtering systems. So, the plasma region is confined very near to the target. For depositing oxide films, the only gas introduced into the chamber is oxygen; thus incorporation of foreign species into the films is avoided. However, ALD [11] is a very suitable technique for obtaining films with uniform thickness at low temperatures exploiting the binding energy difference between chemisorption and physisorption at the substrate surface. One reactant at a time is injected into the growth area, and following surface reactions, excess species and by-products are purged with an inert gas. So, films are grown by sequential surface reactions. This technique allows a precise control of film composition and thickness as the growth proceeds one monolayer at a time on an atomic scale.

The present work deals with the interface quality of TiO_2-based metal–insulator–semiconductor (MIS) structures, with TiO_2 being fabricated by one of the two techniques: HPRS and ALD. We use capacitance–voltage (C–V) technique to study the charge trapped in the insulator, deep level transient spectroscopy (DLTS) to study the trap distributions at the interface and conductance transient (G-t) technique to determine the energy and geometrical profiles of electrically active defects in the insulator bulk as these defects follow the disorder-induced gap state (DIGS) model [12]. It is worth mentioning here that such methods have not been applied earlier to HPRS and ALD TiO_2 films.

2. Experiment

2.1. Sample preparation

HPRS TiO_2/SiO_2 dielectric thin film stacks were grown on $\langle 1\,0\,0\rangle$ n-type low resistivity (5 Ω cm) silicon substrates. Before the films were deposited on the substrates, these were submitted to a complete RCA (Radio Corporation of America) cleaning [13]. This consists of three different steps: firstly, the Si surface is oxidized, secondly the grown oxide is removed and, finally, the Si surface is oxidized again. After RCA the oxide is removed in HF. So, the cleaning in the substrate is deep and the roughness of the insulator/semiconductor interface will be small. Then, a thin layer of SiO_2 was deposited by an ECR (electron cyclotron resonance) oxygen plasma oxidation. This process was conducted in a homemade chamber attached to an ECR Astex 4500 reactor. Substrate temperature was kept at 200 °C. High purity O_2 was the precursor gas for plasma oxidation of Si substrate. A 7 nm thick SiO_2 was obtained after the 60 min plasma oxidation process with a total oxygen flux of 30 sccm. Oxidized substrates were then rapid thermal annealed (RTA) at 900 °C during 30 s in order to improve the electrical quality of the interface. After 77.5 nm TiO_2 films were grown in an HPRS system at a pressure of 1 mbar during 3 h, the growing temperature was kept at 200 °C and the RF power was 600 W. Finally, some samples were *in situ* annealed in oxygen atmosphere at temperatures ranging from 600 to 900 °C. Al dots (0.124 mm^2) were thermally evaporated through a shadow mask as gate electrodes.

On the other hand, ALD films were grown in a flow-type low-pressure (250 Pa) reactor [14]. TiO_2 films were deposited from three different precursor systems employing titanium tetrachloride, $TiCl_4$, and titanium ethoxide, $Ti(OC_2H_5)_4$, as the metal precursors, while water, H_2O, or hydrogen peroxide, H_2O_2, vapours served as the oxygen precursors. In almost all cases an ALD cycle consisted of metal precursor pulse, purge, oxygen precursor pulse and another purge times with the length of 2 s. Due to the high reactivity of $TiCl_4$, shorter pulse time, 0.5 s, could be applied for that precursor. Nitrogen was used as the carrier of precursor as well as the purging gas. The growth temperatures (T_G) and precursors are listed in table 1. The $\langle 1\,0\,0\rangle$ n-type silicon substrates (14 Ω cm) used in our experiments were etched in HF and then rinsed in deionized water immediately before loading them into the reactor. The ALD TiO_2 films were grown on the bare substrates without using any buffer layers. The thickness value of the films deposited for electrical measurements was 20 nm. The relatively narrow band-gap is full of defects which make the material actually semiconducting. In fact, the TiO_2 films were too leaky in their as-grown stage, and therefore thermal annealing was used to improve dielectric properties of those films. These films were too thin for the reliable composition analysis and too leaky for the reliable capacitance measurements. However, the residual impurity content may be the main reason why the low-temperature ALD films are not always measurable without annealing. The annealing has been carried out *ex situ* at 750 °C in purified oxygen (99.999%) under atmospheric pressure for 10 min. After the film deposition and also after the annealing procedures, aluminium dot electrodes were e-beam evaporated through a shadow mask on the top of the dielectric films. The

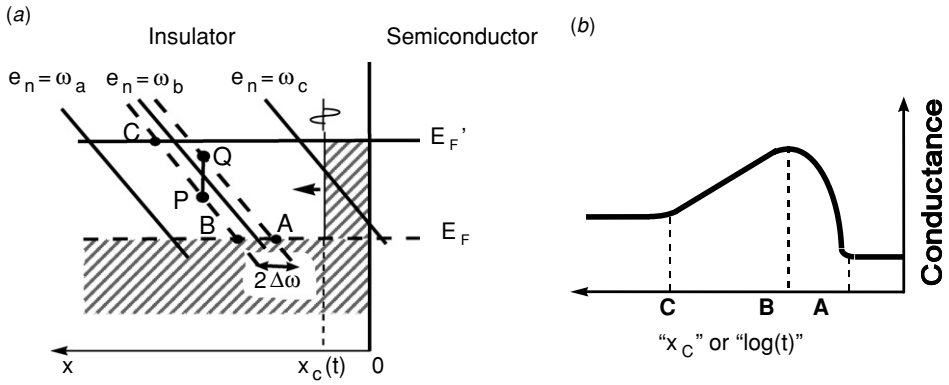

Figure 1. Schematic band diagram of an insulator–semiconductor interface illustrating the capture of electrons by DIGS continuum states during a conductance transient (*a*). General shape of the conductance transient (*b*).

Table 1. Growth temperatures (T_G) and time parameters of the atomic layer deposition processes of TiO_2 films. Electrical characterization results in terms of DIGS are also shown.

Samples	ALD precursors	Growing temperature (°C)	Number of cycles	Thickness (nm)	Maximum DIGS value ($\times 10^{11}$ cm^{-2} eV^{-1})
1012	$TiCl_4 - H_2O$	225	330	20	1.6
1018	$Ti(OC_2H_5)_4 - H_2O$	275	300	20	0.6
1025	$Ti(OC_2H_5)_4 - H_2O_2$	225	360	20	3
1024	$Ti(OC_2H_5)_4 - H_2O_2$	275	330	20	0.9

area of Al dots was 0.204 mm^2. The backsides of the silicon substrates were etched in HF and metallized by evaporating the Al electrodes to provide nearly ohmic contact to silicon. The thickness of the Al electrodes was 120–150 nm.

2.2. *Electrical characterization set-up*

C–V measurements were carried out at room temperature and at liquid nitrogen (77 K) temperature, putting the sample in a light-tight, electrically shielded box. The measurement set-up involved a 1 MHz Boonton 72B capacitance meter and a Keithley 617 programmable electrometer. *C–V* curves are only used to evaluate some features of MIS devices such as flatband voltage and hysteresis phenomena. This technique has been used to determine other features such as insulator thickness and interface state density, but in dielectric stacks, in high-k or in ultrathin layers, the interpretation of the results is different, because *C–V* curves do not fit well with classical models. However, DLTS is a suitable technique to measure interface trap concentrations. Since this technique is time sensitive, it allows differentiating contributions with different time constants due to both fast contributions of interface states and slow contributions corresponding to defects in the dielectric bulk. *C–V* measurements tend to overestimate the interface trap density because they cannot separate slow contributions. DLTS measurements, between 77 and 300 K, were carried out using a 1 MHz Boonton 72B capacitance meter and an HP54501 digital oscilloscope to record the capacitance transients. A Keithley 617 programmable electrometer introduces the quiescent bias, and an HP214B pulse generator introduces the filling pulse. To obtain the interface trap distribution within the forbidden gap, the bias voltage is chosen so that the MIS capacitor is just at the limit between depletion and weak inversion. This technique provides the energy distribution of interfacial states, but does not give information about the spatial distribution, i.e., about DIGS density. From the experimental conductance transients (G-t) measured at different frequencies and at several temperatures, we can obtain the DIGS density as a function of the spatial distance to the interface and of the energy positions. The basis of this technique (shown in figure 1) is explained in our earlier paper [17]. Conductance transients are produced by applying bias pulses that drive MIS structures from deep to weak inversion. There are empty DIGS states that can capture electrons (or holes) coming from the semiconductor conduction (valence) band. This process is assisted by tunnelling and is time consuming, so states near the interface capture electrons (holes) before states located farther away in the dielectric bulk. Conductance transient shape varies with frequency and temperature because only traps with emission and capture rates of the same order of magnitude than the measuring frequency contribute to the conductance. From the experimental conductance transients, $G(t)$, we can obtain the DIGS state density (N_{DIGS}) as a function of the spatial distance to the interface (x_c) and of the energy position, as follows [18]:

$$N_{\mathrm{DIGS}} = \frac{\Delta G/\omega}{0.4qA} \tag{1}$$

$$x_c(t) = x_{\mathrm{on}} \ln(\sigma_o v_{\mathrm{th}} n_s t) \tag{2}$$

$$E' - E(x_c, t) = H_{\mathrm{eff}} + kT \ln\left(\frac{\sigma_o v_{\mathrm{th}} N_c}{\omega/1.98}\right) - kT\frac{x_c(t)}{x_{\mathrm{on}}} \tag{3}$$

where $x_{\mathrm{on}} = \frac{\hbar}{2\sqrt{2m_{\mathrm{eff}}H_{\mathrm{eff}}}}$ is the tunnelling decay length, σ_0 is the carrier capture cross section value for $x = 0$, v_{th} is the carrier thermal velocity in the semiconductor, n_s is the free carrier density at the interface, ω is the angular frequency, A is the capacitor area and N_c is the effective conduction-band

Table 2. Grain size, permittivity and TiO_2 and SiO_2 thicknesses corresponding to films deposited by using HPRS, as a function of oxygen annealing temperature.

Annealing temperature (°C)	SiO_2 thickness (nm)	TiO_2 thickness (nm)	TiO_2 relative permittivity	Grain size (nm)
Unannealed	7	56	26.4	11
600	8.5	53	99.4	16
700	8.5	53	96.7	24
800	8.6	65	102.0	33
900	10.5	61	83.3	61

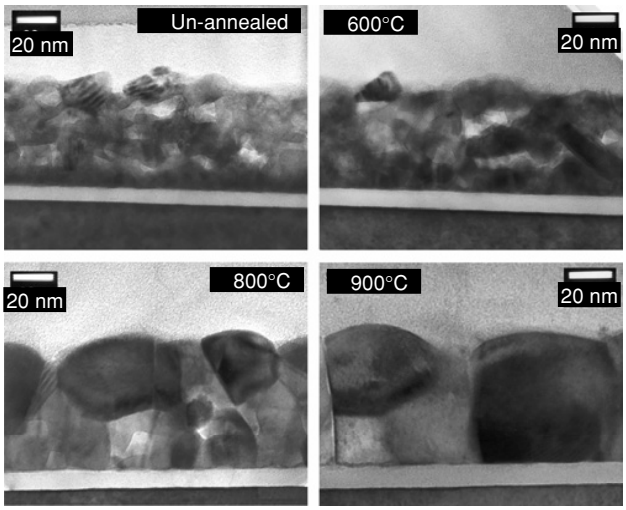

Figure 2. TEM pictures corresponding to HPRS TiO_2 films.

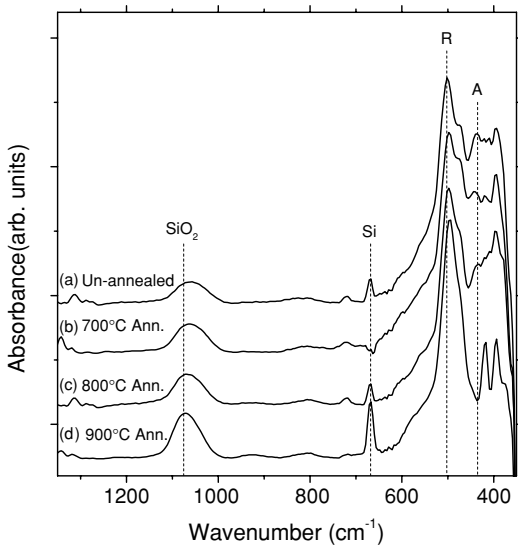

Figure 3. FTIR spectra corresponding to HPRS TiO_2 films.

density of states at the semiconductor (in the case of p-type semiconductors, we use N_v, the effective valence-band density of states). Finally, H_{eff} is the insulator–semiconductor energy barrier for minority carriers and E' means the carrier energy band edge at the insulator (E'_c for electrons and E'_v for holes).

G-t measurements were carried out using an HP 33120A arbitrary waveform generator, which apply the bias pulses, and an EG&G 5206 two phase lock-in analyser to measure the instantaneous conductance signal. Conductance transients were recorded by an HP 54501A digital oscilloscope. Temperature ranged from room temperature to 77 K, putting the samples in an Oxford DNI1710 cryostat. An Oxford ITC 502 controller was used to keep the temperature constant during measurements.

3. Results and discussion

3.1. Film composition and structure

Transmission electron microscopy (TEM) measurements clearly show that TiO_2 HPRS films are polycrystalline, and that grain average size increases when oxygen annealing temperature increases, as shown in figure 2. From film thickness values obtained by using these TEM pictures, we can obtain the permittivity values reported in table 2. The lower value of the permittivity exhibited by the sample annealed at 900 °C must be attributed to some inaccuracy in the determination of the SiO_2 film thickness. Fourier transform infrared spectroscopy (FTIR) spectra are shown in figure 3. FTIR measurements were carried out with a Magna-IR 750 Nicolet spectrometer working in transmission mode and normal incidence, providing a wavenumber resolution of 16 cm^{-1}. We have obtained absorption spectra in the range of 350–4000 cm^{-1}. The peak located at 435 cm^{-1} corresponds to the anatase phase, whereas the peak located at 502 cm^{-1} is associated with the rutile phase. Unannealed TiO_2 film is polycrystalline, and contains both anatase and rutile phases. Only after the oxygen annealing the films are completely crystallized, so unannealed samples exhibit low permittivity values, as shown in table 2. When the annealing temperature increases up to 800 °C, the rutile grain size increases, whereas the anatase grain size decreases. At 900 °C oxygen annealing, the rutile phase dominates, and anatase peak disappears.

The 20 nm thick ALD films were still too thin for the reliable composition analysis. However, electron probe microanalysis (EPMA) and time-of-flight elastic recoil detection (TOF-ERDA) measurements earlier performed for thicker films (100–200 nm) grown under similar conditions demonstrated that the concentration of residual chlorine may not exceed 0.1 at.% in the TiO_2 films grown from $TiCl_4$ and H_2O at 200–275 °C [14, 16] and the concentration of residual carbon was 0.5–1.0 at.% or lower in the films grown from $Ti(OC_2H_5)_4$ and H_2O at 200 °C and higher temperatures [15, 16]. The amount of residual hydrogen also remains at around 0.1 at.%. In the case of ALD TiO_2 films grown at temperatures 225–275 °C in this study, the reflection high energy electron diffraction (RHEED) analysis (figure 4) revealed textured polycrystalline anatase structure in as-deposited films, regardless of the metal precursor and the

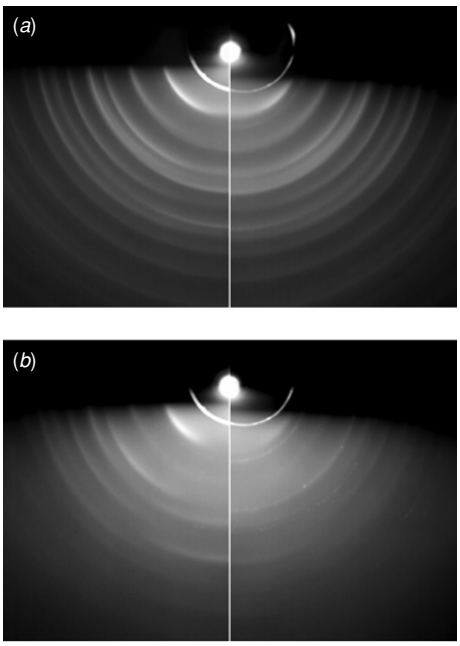

Figure 4. RHEED patterns from the selected TiO_2 films grown on Si(1 0 0) at (*a*) 225 °C from $TiCl_4$ and H_2O (1012 labelled sample in table 1), and (*b*) at 275 °C from $Ti(OC_2H_5)_4$ and H_2O (1024 labelled sample in table 1). Left sides of both panels (*a*) and (*b*) depict films in the as-deposited state, whereas annealed structures are shown on the right-hand side.

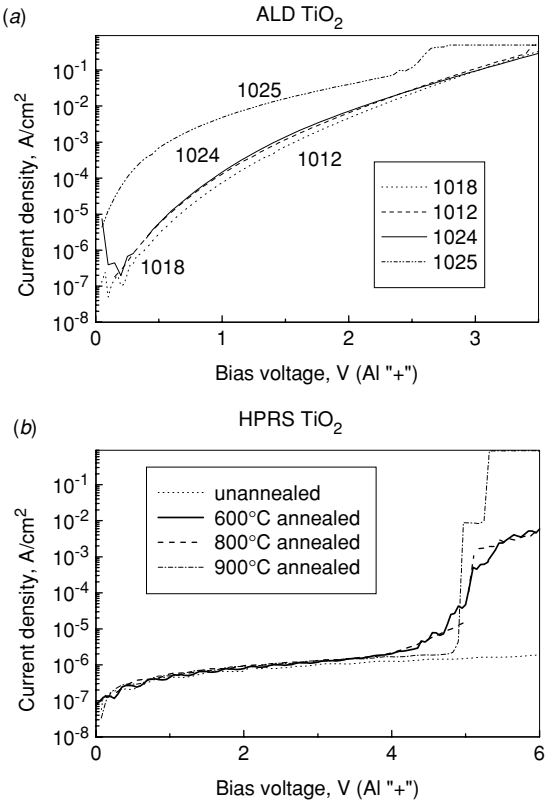

Figure 5. dc current–voltage characteristics corresponding to ALD TiO_2 films annealed at 750 °C (*a*) and HPRS TiO_2 films unannealed and annealed at several temperatures (*b*).

substrate temperature used. Intense (1 0 1), (2 0 0), (1 0 5), (2 1 1), (2 1 3), and (2 0 2) reflections of the anatase phase could all be detected in the films grown from ethoxide (figure 4(*b*)). The films grown from $TiCl_4$ were even more crystalline, decided on the basis of sharper reflections, higher reflection/background intensity ratio and appearance of reflections in the range of relatively small lattice parameters down to 0.76 Å (figure 4 (*a*)), compared to the films grown from ethoxide. The anatase crystallites were mixed with amorphous phase in all films. The films maintained anatase structure after thermal annealing at 750 °C in purified oxygen. Reflections from the rutile phase were observed neither in as-deposited nor in annealed films. The reflections from annealed films became, however, more diffuse compared to those in the as-deposited films, which refers to incomplete re-crystallization and, possibly, some effect of silicon diffused from the substrate into the films. The latter may be supported by the detection of some reflections of polycrystalline silicon, contributing to RHEED patterns. The rutile phase could not be achieved in such thin films grown at those low temperatures probably because even little amounts of impurities (carbon, hydrogen, chlorine) can prevent complete re-crystallization and cannot be efficiently annealed out either at 750 °C. Later, the studies have shown that in the films grown using H_2O_2 in addition to H_2O in otherwise identical experimental conditions possessed slightly higher amounts of residual carbon, while the amounts of residual hydrogen were comparable.

3.2. Electrical characterization

Figure 5 shows dc current–voltage characteristics obtained at room temperature for both ALD (*a*) and HPRS films (*b*). A better behaviour for HPRS samples can be clearly observed. These kinds of samples exhibit lower current density values and higher breakdown voltage than those grown by ALD regardless of the annealing conditions. This fact is directly related to the SiO_2 layer present in the HPRS films that keeps the current density under 10^{-4} A cm^{-2} up to voltages of 4 V. At the same time, ALD films grown on HF-etched Si did not have any chemically grown SiO_2 sub-layer, although some silicon-rich oxide interface layer can expectedly form during the growth process or ultrathin and inhomogeneous SiO_2 may regrow before TiO_2 deposition. Then, the measured current–voltage curve mostly depends on the conductive behaviour of the TiO_2 film. For all these samples, the dc behaviour is acceptable for voltages up to 2.5–3V, that is, for electric fields of 1.25–1.5 MV cm^{-1}.

Figure 6 shows capacitance–voltage curves obtained at liquid nitrogen temperature (*a*) and at room temperature (*b*) corresponding to unannealed HPRS, 700 °C annealed HPRS and 750 °C annealed ALD (labelled 1024 sample in table 1) films. As for *C*–*V* measured at 77 K, we see that unannealed films deposited by HPRS show positive flat-band voltage shift which means negative trapped charge in the insulator. Also, *C*–*V* curves have a considerable stretch out as well as hysteresis behaviour, thus indicating that interface states distribution follows the DIGS model [12]. However, annealed films, both atomic layer deposited and high-pressure sputtered, show flat-band voltage values very near to 0 V, and their *C*–*V* shapes are much less distorted, thus indicating better interface quality. It is worth to point out that the flat-band

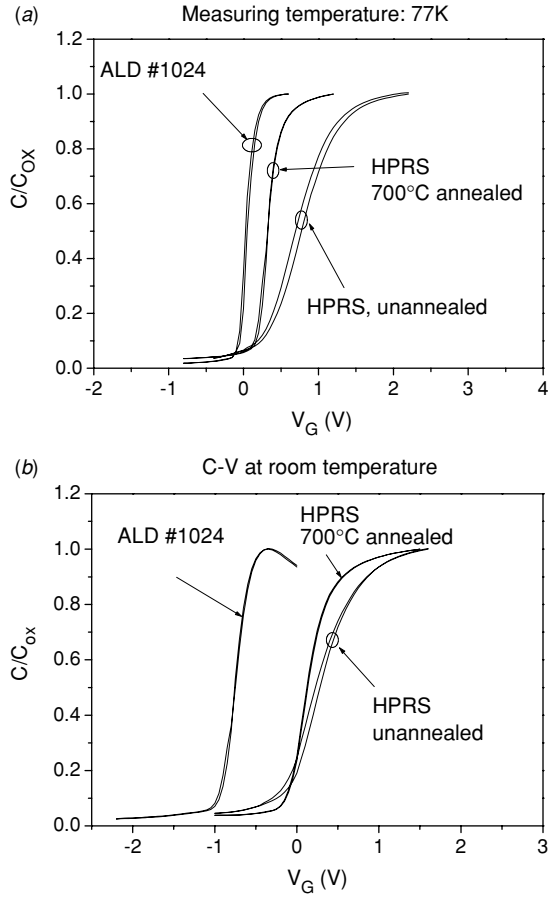

Figure 6. 1 MHz C–V curves measured at 77 K (a) and at room temperature (b) corresponding to unannealed HPRS, 700 °C annealed HPRS and 750 °C annealed ALD (1024 labelled sample in table 1) TiO_2 film-based MIS devices.

voltage corresponding to ALD samples clearly diminishes in C–V curves measured at room temperature with respect to those measured at 77 K, indicating that some electron traps are frozen at low temperatures. Electron traps are filled with electrons at low temperatures and, as temperature increases, they emit electrons decreasing in this way the negative charge in the dielectric and yielding negative shifts of the flat-band voltage.

DLTS measurements allow us to obtain interfacial state density distributions, as shown in figure 7. Unannealed HPRS films have D_{it} densities of 5×10^{12} cm^{-2} eV^{-1}, whereas for 700 °C annealed HPRS films we obtain lower D_{it} values (1×10^{12} cm^{-2} eV^{-1}). As for 750 °C annealed ALD films, D_{it} densities have intermediate values: (4–5) $\times 10^{12}$ cm^{-2} eV^{-1} ($TiCl_4$ and H_2O at 225 °C, $Ti(OC_2H_5)_4$ and H_2O_2 at 275 °C), 3×10^{12} cm^{-2} eV^{-1} ($Ti(OC_2H_5)_4$ and H_2O_2 at 225 °C) and (1–2) $\times 10^{12}$ cm^{-2} eV^{-1} ($Ti(OC_2H_5)_4$ and H_2O at 275 °C). It is possible that the $Ti(OC_2H_5)_4$ and H_2O precursor system provides the best uniformity and homogeneity at the particular temperature, while at lower temperatures assistance of H_2O_2 is required with the alkoxide process. Care must also be taken while drawing conclusions, because more systematic and detailed studies will first be needed in future devoted to the effect of precursor partial pressure and influence of the exposure times.

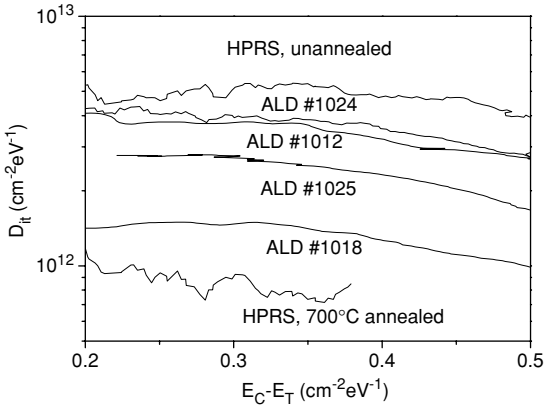

Figure 7. DLTS profiles for unannealed HPRS, 700 °C annealed HPRS and 750 °C annealed ALD TiO_2 film-based MIS devices.

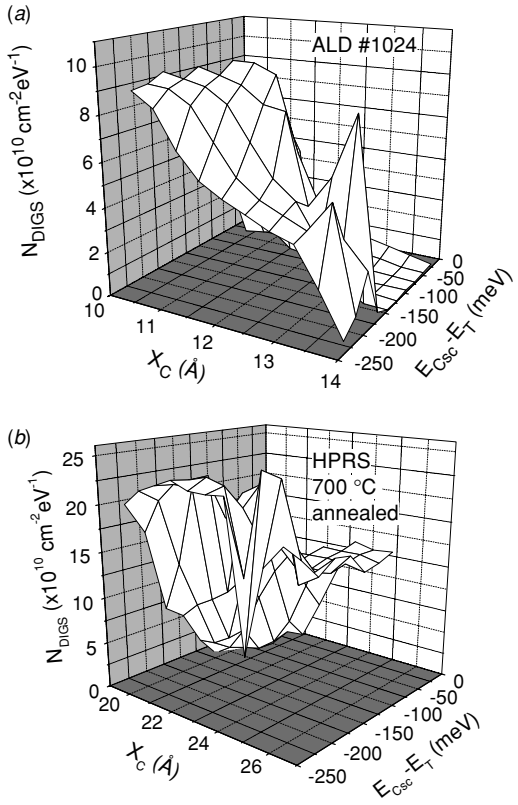

Figure 8. Three-dimensional DIGS profiles of 750 °C annealed ALD (1024 labelled sample in table 1) (a) and 700 °C annealed HPRS (b) TiO_2 film-based MIS devices.

Further, DIGS state density (N_{DIGS}) is obtained as a function of the spatial distance to the interface and of the energy position as it has been explained above. To evaluate the spatial coordinate, we must know the effective mass value. Differences of a factor of 3 have been obtained by using the values provided in [7–9], but they only affect the value of the spatial distance to the interface and not the DIGS density values. So, the intermediate value ($m_e = 3\ m_0$) has been considered through all this work.

Figure 8 shows three-dimensional DIGS profiles of one of the atomic layer deposited and the 750 °C annealed sample

($Ti(OC_2H_5)_4$ and H_2O_2 at 275 °C, table 1) (*a*), and the 700 °C annealed HPRS (*b*) TiO_2 films. In these figures, we can see that electrons reach different depth ranges for ALD than for HPRS samples. This fact is due to that the energy barrier between the semiconductor and the dielectric that determines the tunnelling decay length (see equations (2) and (3) in section 2.2) is different for HPRS samples that have a SiO_2 layer than for ALD samples where a TiO_2 film is directly grown on the silicon substrate. The energy barrier for the SiO_2/Si system (3.2 eV) is higher than that for the TiO_2/Si (1.5 eV) and, then, the tunnelling decay lengths are lower in the first case. Despite their low values of D_{it} obtained by DLTS, we clearly see that DIGS density is higher for 700 °C annealed HPRS films (2.0×10^{11} cm^{-2} eV^{-1}) than for the ALD sample (DIGS density is less than 1×10^{11} cm^{-2} eV^{-1}). As for the other 750 °C annealed ALD films, DIGS maxima values are 3×10^{11} cm^{-2} eV^{-1} ($Ti(OC_2H_5)_4$ and H_2O_2 at 225 °C), 1.6×10^{11} cm^{-2} eV^{-1} ($TiCl_4$ and H_2O at 225 °C) and 6×10^{10} cm^{-2} eV^{-1} ($Ti(OC_2H_5)_4$ and H_2O at 275 °C), as it is indicated in the sixth column of table 1.

All ALD samples in this work have been annealed at 750 °C, so differences in the interface quality must be due to differences in the growth temperature and chemical precursors. In comparing both samples corresponding to the highest growth temperature, 275 °C, our results indicate that values of D_{it} and DIGS are lower for 1018 sample for which chemical precursors used are $Ti(OC_2H_5)_4$ and H_2O, compared to the 1024 sample, for which chemical precursors $Ti(OC_2H_5)_4$ and H_2O_2 were used. So it seems that water is more adequate precursor than oxygen peroxide. On the other hand, 1012 and 1025 samples only differ on the nature of the precursors; in the former case little amount of chlorine may be present, whereas in the latter case carbon has been found and distributed uniformly in the film bulk. Regarding our electrical measurement results, it seems that if the chloride precursor was used, defects are preferentially located very near to the interface (high values of D_{it}), whereas if carbon atoms are present defects penetrate in the dielectric film (high values of DIGS). This conclusion seems to be reasonable, assuming that impurity concentrations can rise towards the oxide–substrate interface, where chlorine may diffuse due to the structural disorder naturally higher after growth of the incommensurate films in the very vicinity of the silicon surface. It is known that in the high-permittivity oxides (HfO_2 and ZrO_2 case studies) grown by ALD, chlorine accumulates near the interface and may not be easily outdiffused by annealing [19]. However, in the bulk of the film grown from $TiCl_4$, the defect density can be lower because the average concentration of impurities is lower than in the films grown from alkoxide [16]. Indeed, higher D_{it} and lower DIGS values correspond to films grown with $TiCl_4$ (sample 1012) than to the film grown from $Ti(OC_2H_5)_4$ (sample 1025).

In addition, the effect of the growth temperature can be seen by comparing 1025 and 1024 samples, both with the same chemical precursors. DIGS density is clearly higher in the case of $T_g = 225$ °C than in the 275 °C, whereas D_{it} value is slightly lower.

HPRS films annealed at 600, 800 and 900 °C exhibit lower DIGS densities than the 700 °C annealed HPRS films. As we can see in figure 9, we obtain 5×10^{10} cm^{-2} eV^{-1} in the case of 600 °C annealing (*a*) and about 1×10^{11} cm^{-2} eV^{-1} in the 800 °C case (*b*). Within our experimental resolution, conductance transients have not been detected for 900 °C annealed HPRS samples. However, at this point it is worth comparing DIGS and D_{it} densities. Figure 10 indicates that samples annealed at 600 °C and 800 °C exhibit higher interfacial state densities than those annealed at 700 °C. Also, the lowest value of D_{it} is obtained for 900 °C annealed HPRS films.

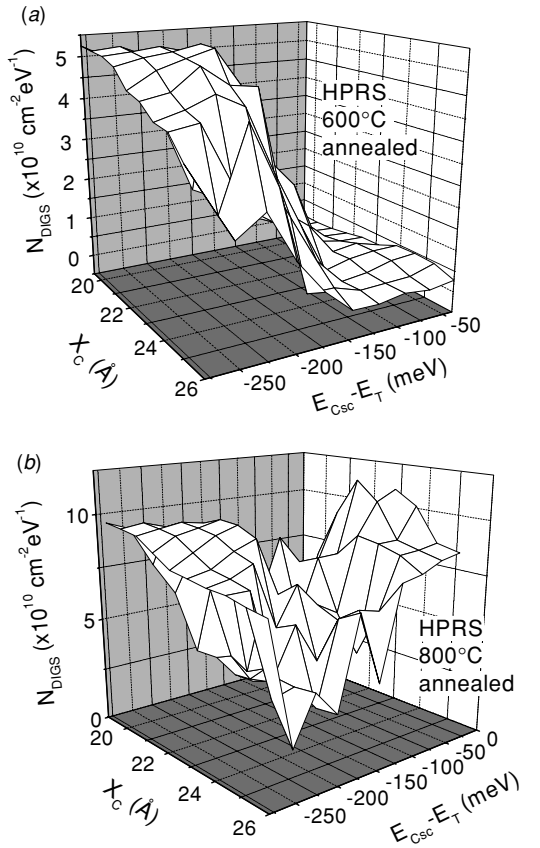

Figure 9. Three-dimensional DIGS profiles of 600 °C (*a*) and 800 °C (*b*) annealed HPRS TiO_2 film-based MIS devices.

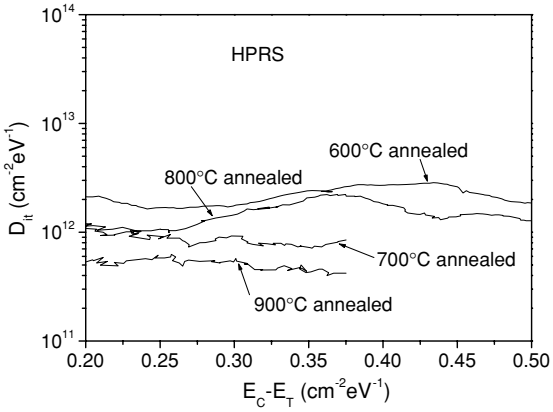

Figure 10. DLTS profiles for several temperatures oxygen annealed HPRS TiO_2 film-based MIS devices.

4. Conclusions

In summary, an electrical characterization of TiO_2-based MIS structures, with TiO_2 being fabricated by using two different methods: HPRS and ALD, has been carried out, by means of C–V, DLTS and G-t techniques. A comparison between several temperatures thermal annealed HPRS films has been established. Our results show that, in terms of interfacial state density, 700 °C annealed HPRS films exhibit better interface quality than 750 °C annealed ALD films. However, DIGS density is higher for 700 °C annealed HPRS films than for 750 °C annealed and 275 °C growth ALD TiO_2 films, whereas DIGS values corresponding to 700 °C annealed HPRS films are similar to those obtained for 750 °C annealed and 225 °C growth ALD TiO_2 films. 800 °C annealed HPRS films exhibit DIGS density values lower than those obtained for 700 °C cases, and the annealing temperature of 600 °C provides HPRS films with DIGS density as low as 5×10^{10} cm^{-2} eV^{-1}. However, both 800 and 600 °C annealing temperatures provide films with poorer interfacial properties in terms of D_{it} than in the 700 °C annealing temperature cases. Finally, 900 °C annealed HPRS films seem to be the best, with D_{it} density being the lowest value measured in this work ($5–6 \times 10^{11}$ cm^{-2} eV^{-1}), and undetectable conductance transients within our experimental limits. The good interface quality of 900 °C oxygen annealed HPRS films can be due to two contributions. First, oxygen present during the annealing oxidizes the silicon surface and increases the SiO_2 film thickness, as has been proved by TEM (table 2) and FTIR (figure 3). The increase with the annealing temperature of the crystalline phase (rutile) of HPRS samples (table 2 and figure 3) can also contribute to the observed interface improvement.

As for ALD TiO_2 films, all samples studied in this work have been annealed at 750 °C, and they are all more like anatase. However, the growth temperature and chemical precursors have been varied. We obtain the best result for the $Ti(OC_2H_5)_4$ and H_2O precursors and 275 °C growth temperature, both in terms of D_{it} ($1–2 \times 10^{12}$ cm^{-2} eV^{-1}) and DIGS (as low as 6×10^{10} cm^{-2} eV^{-1}). It seems that in the cases in which the main ALD precursor is $Ti(OC_2H_5)_4$, it is more adequate to use H_2O than H_2O_2 in order to obtain a better interface quality. On the other hand, chloride precursor leads to higher values of D_{it} but at the same time lower values of DIGS than measured in the films grown from alkoxide containing carbon. Finally, 225 °C growth temperature led to lower values of D_{it} but higher values of DIGS than 275 °C growth temperature.

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