A Comparison of Quantum-Mechanical Capacitance–Voltage Simulators

C. A. Richter, A. R. Hefner, and E. M. Vogel

***Abstract*—We have systematically compared the results of an extensive ensemble of the most advanced available quantum-mechanical capacitance–voltage (*C–V*) simulation and analysis packages for a range of metal-oxide-semiconductor device parameters. While all have similar trends accounting for polysilicon depletion and quantum-mechanical confinement, quantitatively, there is a difference of up to 20% in the calculated accumulation capacitance for devices with ultrathin gate dielectrics. This discrepancy leads to large inaccuracies in the values of dielectric thickness extracted from capacitance measurements and illustrates the importance of consistency during *C–V* analysis and the need to fully report how such analysis is done.**

***Index Terms*—Capacitance, effective oxide thickness, gate dielectric, inversion quantization, MOS devices, polysilicon depletion.**

I. Introduction

IN RECENT years, the continuing decrease of the gate dielectric thickness in conventional silicon MOS devices has made it increasingly difficult to predict capacitance–voltage (*C–V*) curves accurately. Thus, predictive TCAD is problematic and likely to be incorrect. Researchers have developed sophisticated methods to simulate *C–V* curves [1]–[8], [10], [11] in an effort to overcome this difficulty. However, there has been little work comparing the outputs from such simulators to check their agreement. In an effort to determine the variability between such simulators, we have acquired an ensemble of five advanced quantum-mechanical (QM) simulation and analysis packages and compared their results for a matrix of *C–V* curves produced for a range of device parameters.

Currently, one of the most prevalent uses of these QM *C–V* simulators is to determine the equivalent oxide thickness (EOT) of MOS devices made from alternate (high-k) dielectrics proposed to replace SiO_2 as the gate dielectric in future MOS technologies. Finding a replacement gate dielectric is necessary in order for traditional CMOS scaling to continue, and EOT is a primary criteria used to assess which materials are technologically most promising. Thus, it is critical that the interrelationship of QM CV simulators be well characterized to properly compare EOT extracted from experimental *C–V* curves.

Traditionally, the thickness, d, of the dielectric in an MOS capacitor was easily found by $d = \varepsilon A/C_{ox}$, where ε is the dielectric's permittivity, A is the device area, and C_{ox} is the device capacitance (in accumulation). However, this simple relationship does not hold for thin oxides, and extracting a accurate physical thickness from *C–V* curves is increasingly difficult for oxide thicknesses at and below 2 nm. Two primary effects, illustrated in Fig. 1, must be considered: quantum mechanical confinement, and the finite voltage drop across polysilicon gates (poly-Si depletion). To avoid the confusion often associated with *C–V*-derived film thickness, the following terminology will be used. EOT is the equivalent thickness of SiO_2 that would produce the same *C–V* curve as that obtained from the alternate dielectric system. The capacitive effective thickness (CET(V)) is simply the thickness that is derived directly from the relationship $\mathrm{CET(V)} = (\varepsilon_0 \varepsilon_{\mathrm{SiO_2}} A)/\mathrm{C(V)}$, where ε_0 is the permittivity of free space, $\varepsilon_{\mathrm{SiO_2}}$ is the relative permittivity of SiO_2, and C(V) is the capacitance at bias voltage V.

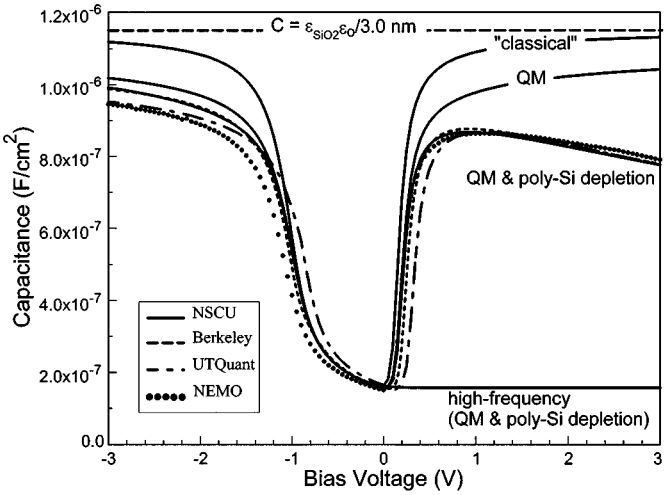

Fig. 1. Simulated *C–V* curves accounting for both QM confinement and poly-Si depletion. Simulated parameters are $d_{ox} = 3.0$ nm (2.987 nm for NEMO [10]), $\mathrm{N}_d = 3 \times 10^{17}$ cm^{-3}, and $\mathrm{N}_{poly} = 5 \times 10^{19}$ cm^{-3}. A classical *C–V* with no QM confinement or poly-Si depletion and a QM *C–V* which accounts for QM confinement only are also shown for illustrative purposes.

II. Simulators

An ensemble of five of the most advanced, one-dimensional (1-D) , quantum-mechanical *C–V* software packages was used in this comparison:

1) Quantum mechanical *C–V* simulator developed by the Device Group at UC Berkeley (Berkeley) [5];
2) Nanotechnology Engineering Modeling Program (NEMO) [2], [11];
3) CVC, a program developed by Hauser [1], [10] at NCSU (NCSU);

Manuscript received June 13, 2000. This work was funded in part by the NIST Office of Microelectronics Programs. The review of this letter was arranged by Editor K. De Meyer.

The authors are with Semiconductor Electronics Division, National Institute of Standards and Technology, Gaithersburg, MD 20899-8121 USA (e-mail: Curt.Richter@NIST.Gov).

Publisher Item Identifier S 0741-3106(01)00686-3.

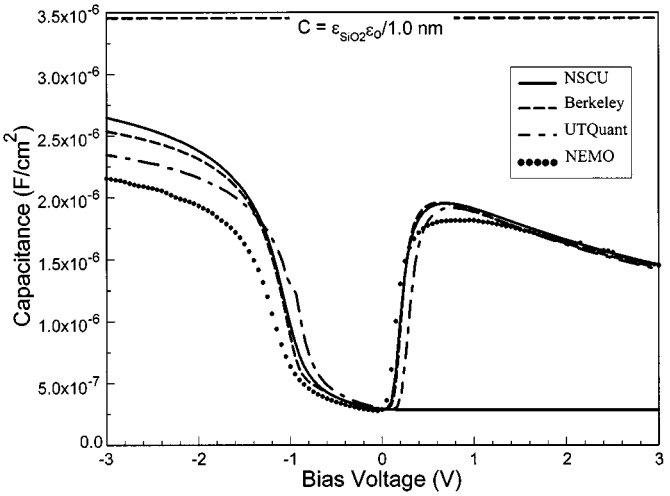

Fig. 2. Simulated *C–V* curves accounting for both QM confinement and poly-Si depletion. Simulated parameters are $d_{ox} = 1.0$ nm (1.086 nm for NEMO), $N_d = 1 \times 10^{18}$ cm^{-3}, and $N_{poly} = 1 \times 10^{20}$ cm^{-3}.

4) UTQuant developed at UT-Austin [4];
5) IBM's Tqm_v6 [3].

Three programs are purely simulation packages; Berkeley, NEMO, and UTQuant. NCSU is both a simulation and analysis package, while IBM's Tqm_v6 is only a *C–V* analysis program. The simulators all assume a source of minority carriers in the Si-substrate, and therefore produce ideal quasistatic *C–V* curves, or curves obtained in transistor measurements.

In simulating *C–V* curves, Berkeley calculates the electron/hole distributions in both inversion and accumulation derived by solving the Schrödinger and Poisson equations self-consistently with the Fermi–Dirac distribution [5]. NEMO, the most physically comprehensive of the ensemble, is a nonequilibrium Green's function simulator [2], [11]. In it, fundamental physics—such as multiband scattering, inelastic scattering, and interface roughness—can be simulated. NCSU is based upon a model containing first order physics approximations that can be rapidly calculated [1], [10]. UTQuant is another self-consistent, QM Poisson solver [4]. IBM's Tqm_v6 is a fast QM *C–V* analysis program that is based upon polynomial interpolation from the results of IBM's extensive QM simulations [3].

An n-channel MOS capacitor was chosen as the test structure to compare the various simulators. The MOS capacitor consists of a p-type silicon substrate, ideal SiO_2 gate dielectric, and n-type poly-Si as the gate material. This idealized structure was chosen in order to best compare the results of the simulators themselves. The parameters of the capacitor were varied to create a matrix of *C–V* curves: oxide thickness, $d_{ox} = 1.0$ nm, 2.0 nm, 3.0 nm, and 10.0 nm; silicon substrate doping, $N_d = 1 \times 10^{15}$ cm^{-3}, 1×10^{17} cm^{-3}, 3×10^{17} cm^{-3}, and 1×10^{18} cm^{-3}; and poly-Si doping, $N_{poly} = 1 \times 10^{19}$ cm^{-3}, 5×10^{19} cm^{-3}, and 1×10^{20} cm^{-3}. An effort was made to insure that comparable values were used for other parameters in the simulations such as work functions because their default values sometimes varied between simulators. Our simulations were done from -5 V to 5 V in nominally 50 mV steps [1]. It should be noted that this voltage range can lead to artificially large electric fields in the thinnest devices simulated.

TABLE I
PARAMETERS EXTRACTED BY USING Tqm_v6. SIMULATED PARAMETERS ARE: TOP, $d_{ox} = 1.0$ nm, $N_d = 1 \times 10^{18}$cm^{-3}, and $N_{poly} = 1 \times 10^{20}$cm^{-3}; BOTTOM, $d_{ox} = 3.0$ nm, $N_d = 3 \times 10^{17}$cm^{-3}, and $N_{poly} = 5 \times 10^{19}$cm^{-3}. CET IS DETERMINED AT -2.5 V

Simulator	CET (nm)	EOT (nm)	V_{fb} (V)	N_d (cm^{-3})
Berkeley	1.408	0.878	-1.141	1.12E18
NCSU	1.357	0.833	-1.133	1.12E18
NEMO (1.086 nm)	1.663	1.108	-1.281	1.12E18
UTQuant	1.520	0.979	-0.948	1.20E18

Simulator	CET (nm)	EOT (nm)	V_{fb} (V)	N_d (cm^{-3})
Berkeley	3.562	2.849	-1.087	3.44E17
NCSU	3.552	2.840	-1.076	3.44E17
NEMO (2.987 nm)	3.737	3.012	-1.153	3.19E17
UTQuant	3.695	2.973	-0.920	3.44E17

III. RESULTS AND DISCUSSION

Figs. 1 and 2 show typical *C–V* simulations for $d_{ox} = 3.0$ nm and for $d_{ox} = 1.0$ nm, respectively (with the exception of the thickness used in NEMO, which is nominally the same [2]). These figures illustrate that the simulators are in qualitative agreement; i.e., the overall shape of the *C–V* curves is the same for these four different simulators. More specifically, the capacitance value at the minimum is the same for the set. This agreement indicates that the simulators agree on how substrate doping affects the shape of the *C–V* curves. The flatband and threshold values of the *C–V* curves are also in good agreement with the exception that the default parameters used for UTQuant lead to a slight shift with respect to the others. This agreement between the simulators, where some are based on very different fundamentals (such as NSCU and NEMO) and others that have nominally the same basis (i.e., UTQuant and Berkeley), instills confidence in the overall capabilities of all these simulators.

However, there are systematic trends and important differences between the various simulators. The largest disparity is in the values of the accumulation region capacitance. The NCSU and Berkeley simulators tend to have the largest accumulation capacitance for a given set of parameters, while NEMO and UTQuant have a lower accumulation capacitance. This disagreement leads to *C–V* curves that appear to be from devices with different oxide thicknesses. On the other hand, there is surprisingly little difference in the simulated *C–V* curves in the inversion region. It should be noted that there is slightly greater variability (not shown) in the inversion capacitance when a metal gate is simulated (i.e., no poly-Si depletion).

[1]The Berkeley simulator simulates data in steps that are uniform in Si-surface potential, and are therefore not uniform in gate bias. A comparable number of data points (200) were simulated

[2]In NEMO, a minimum mesh of the silicon lattice constant (0.271 547 nm) is most physically realistic and gives consistent results. Therefore, the thicknesses simulated in NEMO are near, but not exactly, the same as the nominal thickness values

In order to quantitatively determine the relationships among the various simulators, we have used Tqm_v6, IBM's QM *C–V* analysis program, to extract a reduced set of parameters (or assessment criteria) for each simulated *C–V* curve. These extracted values are then used to compare the results for the simulators. This analysis also compares the simulators with the calculations utilized by Tqm_v6. Table I shows the extracted EOT, CET, and N_d for two different sets of parameters; one set at $d_{ox} = 3.0$ nm and the other set at $d_{ox} = 1.0$ nm. There is little variation in the extracted substrate doping values, as expected. In addition, the extracted flatband values are also in moderate agreement, as expected from the results shown in Figs. 1 and 2. The simulators are not in such strong agreement for EOT. There is a maximum difference [3] of 0.185 nm between the simulations for the $d_{ox} = 3.0$ nm parameter set, and a maximum difference of 0.189 nm for $d_{ox} = 1.0$ nm. This illustrates that the offset between simulators is not scaling with the thickness of the SiO_2, and thus becomes a larger problem for thinner gate dielectrics. The apparent thickness variability is a significant proportion of the total film thickness (up to 20%). This observed thickness variability is larger than the EOT thickness control value ($<\pm 0.08$ nm) required for the year 2001 by the 1999 ITRS [9]. We are currently investigating the possible physical assumptions leading to differences between the various simulators such as: the use of approximations for quantum effects versus a full solution of the Schrödinger equation, wave function boundary conditions at the Si/SiO_2 interface, type of carrier statistics, and models for handling highly doped poly-Si. In addition to a comprehensive understanding of the physical assumptions, a detailed knowledge of the computational methods used to solve the underlying physical equations is necessary to fully understand why this suite of programs is not in exact agreement in accumulation.

Although a significant discrepancy has been identified, it is difficult experimentally to determine which simulator is most "accurate." Typically, physical thickness measurements have minimum uncertainties on the order of 0.2 nm with regards to accuracy. In addition, the active doping concentration and profiles in the poly-Si gate affect the derived thickness and therefore also must be determined accurately. Thus, while there are systematic differences among the simulators they are in agreement to levels that are experimentally verifiable. Choosing the "most correct" one remains extremely challenging.

IV. Conclusions

While this extensive comparison of *C–V* simulator/analysis packages increases the confidence in the individual packages in this ensemble, important systematic differences in the resulting *C–V* curves have been observed. The most noticeable of these variations occurs in the accumulation capacitance region and leads to variations in extracted EOT on the order of 0.2 nm for total SiO_2 film thicknesses in the range 1.0 nm to 3.0 nm. This thickness variation is a significant proportion of the total film thickness—up to 20% of the total film thickness. The demonstrated discrepancy illustrates that when reporting experimentally derived electrical thickness results, it is important to describe fully how these values were obtained. The same experimental curve can lead to different extracted EOT values depending upon which QM software is used for the analysis. Therefore, it is essential that EOT results be presented consistently and with sufficient detail to allow the technical community to reliably compare *C–V* results.

[3]The maximum difference is determined from comparing $d_{ox}^{\text{simulated}}$-EOT(Tqm_v6) for the various simulators.

Acknowledgment

The authors would like to acknowledge R. Lake (Raytheon), J. Hauser (NCSU), D. Buchanan, E. Gusev (IBM), A. Tasch (UT Austin), the Device Group at UC Berkeley, S. Satterfeld, D. Blackburn, and J. Ehrstein (NIST) for their help during this comparison.

References

[1] J. R. Hauser and K. Ahmed, "Characterization of ultra-thin oxides using electrical C-V and I–V measurements," in *Characterization and Metrology for ULSI Technology*, Seiler *et al.*, Eds. Woodbury, NY: AIP, 1998, pp. 235–239.

[2] R. Lake *et al.*, "Single and multiband modeling of quantum electron transport through layered semiconductor devices," *J. Appl. Phys.*, vol. 81, pp. 7845–7869, 1997.

[3] S.-H. Lo, D. A. Buchanan, and Y. Taur, "Modeling and characterization of quantization, polysilicon depletion and direct tunneling effects in MOSFET's with ultrathin oxides," *IBM J. Res. Develop.*, vol. 43, pp. 327–337, 1999.

[4] W.-K. Shih *et al.*, *UTQUANT 2.0 User's Guide*. Austin, TX: Univ. Texas Press, Oct. 1997.

[5] Berkeley Device Group.. [Online].. Available: www.device.eecs.berkeley.edu/qmcv/html

[6] K. S. Krisch, J. D. Bude, and L. Manchanda, "Gate capacitance attenuation in MOS devices with thin gate dielectrics," *IEEE Electron Device Lett.*, vol. 17, pp. 521–524, 1996.

[7] C. Bowen *et al.*, "Physical oxide thickness extraction using quantum mechanical simulation," in *IEDM Tech. Dig.*, 1997, pp. 869–872.

[8] S. V. Walstra and C.-T. Sah, "Thin oxide thickness extrapolation from capacitance-voltage measurements," *IEEE Trans. Electron Devices*, vol. 44, pp. 1136–1142, 1997.

[9] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors: 1999*. Austin, TX: SEMATECH, 1999.

[10] W. K. Henson *et al.*, "Estimating oxide thickness of tunnel oxides down to 1.4 nm using conventional capacitance-voltage measurements on MOS capacitors," *IEEE Electron Device Lett.*, vol. 20, pp. 179–181, 1999.

[11] D. K. Blanks *et al.*, "NEMO: General release of a new comprehensive quantum device simulator," in *Proc. IEEE 24th Int. Symp. Compound Semiconductors*, 1998, pp. 639–642.