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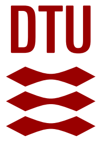

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A Comparison Review of the Resonant Gate Driver in the Silicon MOSFET and the GaN Transistor Application

Bainan Sun, *Student Member, IEEE,* Zhe Zhang, *Senior Member, IEEE*
and Michael A.E. Andersen, *Member, IEEE.*

***Abstract*—The increasing transistor power loss brought by the high switching frequency places a limit to the future high power density converter design. A review of resonant gate drivers is given in this paper to provide a vision for its future application. Various resonant gate driver topologies from the prior-art research is categorized and thoroughly compared in terms of the implementation frequency and the percentage gate driver loss reduction. Moreover, a case study of two representative resonant gate driver topologies is given. The conventional gate drive and two resonant gate drivers are implemented to driver Silicon MOSFETs and Gallium Nitride (GaN) transistors respectively. The feasibility and effectiveness of implementing resonant gate drivers in wide band-gap semiconductor transistors is discussed according to a detailed comparison of loss decomposition.**

***Index Terms*—Resonant gate driver, gate driver loss, high frequency, GaN transistor, Silicon MOSFET.**

I. Introduction

HIGH power density is one critical consideration for the future power converter design. High switching frequency is generally viewed as the solution, which largely shrinks the volume of the passive component [1]. However, the transistor power loss is proportional to the switching frequency, which poses challenges to the thermal management and efficient power conversion. Minimization of transistor power loss in high frequency switching is important.

The general model of a field effect transistor is shown in Fig. 1 [2]. The transistor power loss is composed by conduction loss, switching loss and gating loss. The conduction loss is related to the transistor on-state resistance. Reduction of the conduction loss is considered in the converter operating at high conduction current. Especially in the high-step-up ratio DC-DC converter, high conduction current in the low side transistor can lead to severe efficiency degradation and thermal dissipation challenge [3]. Therefore, the interleaved converter topology is widely adopted as one of the solutions to reduce the conduction loss [4], [5]. On the other hand, the switching loss is related to the transistor output capacitor ($C_{oss} = C_{ds} + C_{gs}$) and proportional to the switching frequency. Reduction of the switching loss is considered within a wide range of applications, such as the low-power chip-scale power converter (33 MHz, 10.5 W) [6], the medium-power DC-DC converter (100 kHz, 1 kW) [7] and the high-power grid-connected inverter (16 kHz, 30 kW) [8]. Soft-switching technique is generally used as the solution for switching loss reduction [9]–[11]. The gating loss is related to the transistor input capacitor ($C_{iss} = C_{gs} + C_{gd}$) and also proportional to the switching frequency. Reduction of the gating loss is considered in the low to medium power range converters ($\leq$ 1 kW). Especially in the high frequency soft-switching converter applications, the transistor gating loss can have significant impact on the power conversion efficiency. As an example, a loss decomposition of the power MOSFET in a synchronous buck converter is given in Fig. 2. The conduction loss at 10 V, 1 A output is 0.77 W, while the gating loss can be up to 1.82 W at 1 MHz. Considering the 10 W converter output power, the gating loss can degrade the total efficiency by 2 - 18% depending on the switching frequency. Reduction of the gating loss is important for the low power range voltage regulator modules. Resonant gate driver is widely adopted to achieve low gating loss.

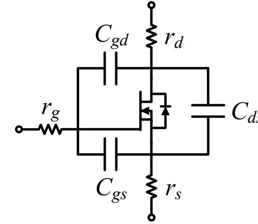


Fig. 1. Equivalent circuit of the field effect transistor.

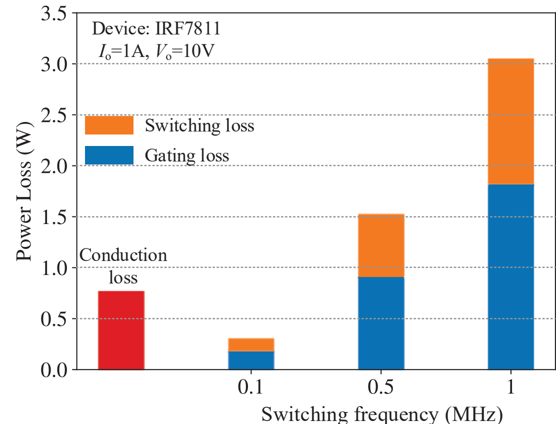


Fig. 2. MOSFET power loss decomposition in a synchronous buck converter.

Besides the above mentioned techniques, the implementation of wide band-gap semiconductor material in the transistor fabrication sheds new light on the high frequency high

power density converter design. GaN transistor is widely considered as a promising candidate for the next generation of power transistor [12]. Compared with Silicon MOSFET, GaN transistors have smaller on-resistance, smaller parasitic capacitance, higher operating temperature and more compact package size. For the GaN transistor, the slew rate of the drain-source voltage can be as high as 100 V/ns during the switching transient [13]. All these salient features enable the GaN transistor's application in high frequency power conversion [14]–[16]. However, the transistor over-heating and efficiency degradation brought by the increasing power loss during the high frequency switching is still the major concern. This problem is even more challenging when considering the limited heat dissipation capacity resulted from the chip scale packaging technique adopted by the majority of GaN transistor manufacturers. The soft-switching technique is dependent on the transistor C_{oss} and the converter topology, which has been widely adopted and proved valid for the GaN transistor application [17]–[19]. The effectiveness of the resonant gate driver is dependent on the transistor C_{iss}. Implementation of the resonant gate driver in the GaN based converter can be found in very few prior-art research [20]–[22]. Moreover, the detailed gate driver loss decomposition is rarely mentioned. Therefore, the review, comparison and analysis of different resonant gate driver topologies is important for the topology selection, transistor selection and efficiency estimation of the future high frequency power converter design.

This paper is dedicated to discuss the implementation of resonant gate driver in the high frequency power conversion. A thorough comparison of the resonant gate driver topologies is given. Prior-art research from the literature review is summarized, categorized, analyzed in section II. Intuitive comparison results are given as a reference to the gate driver selection for the high frequency power converter design. In section III, a case study of two representative resonant gate driver topologies is carried out. The detailed gate driver loss decomposition is given in the comparison of Silicon MOSFET and GaN transistor application. Section IV concludes the paper.

II. Literature Review of the Resonant Gate Driver

A. Basic Principle of the Resonant Gate Driver

Conventional gate driver adopts the totem pole topology and shown in Fig. 3. PMOS and NMOS are in series configured as the totem pole to generate the square wave gate signal [23]. Gating process is achieved by charging and discharging the C_{iss} of transistor Q, which is shown in Fig. 4(a). Duration

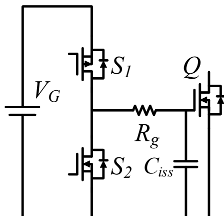


Fig. 3. Conventional totem pole gate driver.

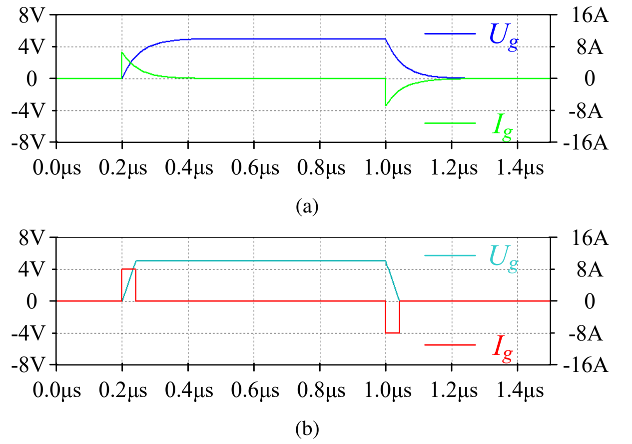


Fig. 4. Comparison of voltage source and current source gate driver: (a) voltage source gate driver (b) current source gate driver.

of the gating transient is dominant by the time constant of the gate resistor R_g and the transistor input capacitor C_{iss}. A fast switching transient can be achieved by a smaller gate resistor, which helps to reduce the switching loss of transistor Q. Selection of the gate resistor is the trade-off between the switching loss and the gate voltage over-shoot. Gating loss, also known as CV^2 loss, is defined as the power loss on the gate resistor during the switching transient.

For the conventional gate driver, the well-known equation for gating loss calculation is shown as

$$P_{gate} = V_G \cdot Q_G \cdot f_s = {V_G}^2 \cdot C_{iss} \cdot f_s, \tag{1}$$

where Q_G is the gate charge and f_s is the switching frequency. V_G is the gate voltage, which equals to the electric potential difference between the gate-on voltage and the gate-off voltage ($V_G = V_{g_on} - V_{g_off}$). The gating loss is dissipated on the gate loop resistance. For the conventional gate driver, the gating loss can be hardly reduced for the application with a certain switching frequency and limited options in transistor selection.The basic idea of the resonant gate driver is to compose a current source to drive the transistor Q. As a result, the resonant gate driver is also referred as the current source gate driver in some research [24]–[27]. The power loss of the resonant gate driver is composed by the loss on the transistor gate resistor, the ancillary transistor/diode bridge and the resonant tank. Another benefit of implementing the resonant gate driver is the fast charging/discharging capability. As shown in Fig. 4(b), with a large and rather constant gate current, the gating transient is shortened and the switching loss of transistor Q can thus be reduced.

Although different resonant gate drivers vary in topology, application scenario and control scheme, majority of them origins from the same totem pole topology and differs in the resonant tank design. One criterion to categorize all the resonant gate driver designs is the initial inductor current. For the zero initial inductor current topologies, the gate charging process is simultaneous with the charging process of the resonant inductor. For the non-zero initial inductor current topologies, gate charging is initialed with a start-up current, which further helps to shorten the switching transient. Review

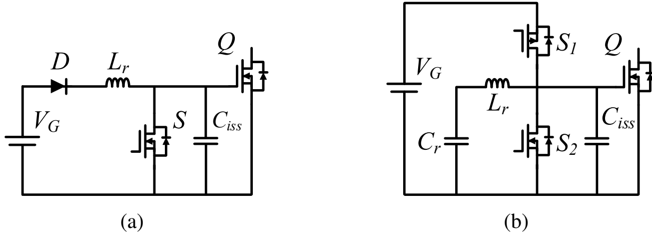


Fig. 5. The basic resonant gate driver topology: (a) resonance during the gate-on transient [28] (b) resonance in both the gate-on and the gate-off transient [29].

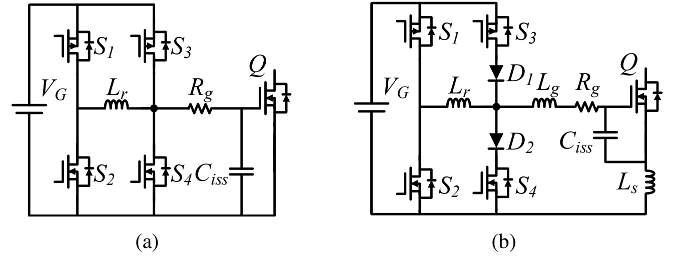


Fig. 7. Power recovery resonant gate driver: (a) the basic topology [31] (b) parasitic impedance insensitive topology with blocking diode [24].

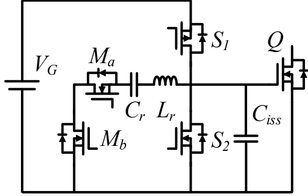


Fig. 6. Pulse resonant gate driver [30].

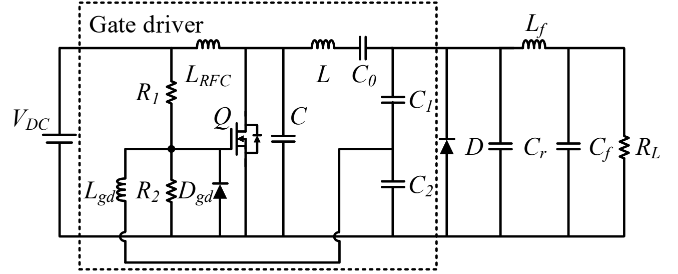


Fig. 8. Self-oscillating resonant gate driver [33].

and comparison of the resonant gate driver will be carried out in the two major groups of topologies categorized by this criterion.

B. Non-zero Initial Inductor Current Resonant Gate Driver

The idea of resonant gate driver was first proposed in [28] and applied quasi-resonant buck converter to reduce the considerate power loss from the conventional gate driver at 10 MHz switching frequency. The first resonant gate driver topology was inspired by the phenomenon that the MOSFET switching characteristics could be improved by a series connected inductor within the gate loop. As shown in Fig. 5(a), during the gate transistor S is conducting, the transistor Q is off and current is formed in the inductor L_r. When S is switched off, the transistor Q is gated on by the resonance of the inductor and the input capacitor of Q. The conventional gating loss is reduced to the loss within the resonant tank. The total gate driver loss is reported to be 1.5 W at 10 MHz switching frequency. Further research into this idea is given in [29], as shown in Fig. 5(b). The input capacitor of Q is both charged and discharged in a resonant circuit. The proposed resonant gate drive is applied to a high-frequency low-power multi-resonant buck converter. From the SPICE simulation, the gate driver loss at 2 MHz switching frequency is estimated to be 0.23 W, which is much lower than the 0.8 W power dissipation in the conventional gate driver.

Further research into the resonant gate driver is accompanied with extra gate transistors and more control flexibility. The pulse resonant gate driver with online controllable slew rate is proposed in [30] and shown in Fig. 6. M_a and M_b are the ancillary switches, which are in reverse series connected to provide separate charging and discharging path for the LC resonant tank. The gate current is thus on-line controllable and modulated by the phase shift control between the two transistor pairs in the gate driver. The PSPICE simulation result is given at 12 V, 1 MHz switching condition. The gate driver loss is reported to be 0.33 W when rise/fall time is 25 ns and 0.42 W when rise/fall time is 20 ns.

For the resonant gate driver, only partial energy stored in the resonant tank is used to gate on the transistor. Power recovery of the residue energy within the resonant tank is another popular research topic. The resonant gate driver designed for the gate energy recovery is researched shown in Fig. 7(a) [31], [32]. A small resonant inductor is installed between the two totem pole bridges. Four gate transistors are modulated to provide six individual states for inductor current forming, gate charge/discharge and power recovery. Excessive inductor stored energy is returned to the gate voltage source V_G. This topology is demonstrated in a 1 MHz 12 V Boost converter. The gate driver loss is reported to be 0.20 W, compared with 0.34 W from the conventional gate driver. The similar idea is studied in [26] to provide dual-channel output, which is reported to reduce the gating loss by 67 % compared with the conventional gate driver. Further research into this topology is given in [24], as shown in Fig. 7(b). Schottkey diodes D_1 and D_2 are installed to block the voltage ringing and the gate voltage is clamped during the conduction state of transistor Q, which helps the resonant tank design less sensitive to the parasitic component on the gate path.

Self-oscillating gate driver is one special category of the resonant gate driver. Different from the totem pole based topologies, gate transistors are no longer needed. Drain source voltage of the transistor Q is fed back to the resonant tank and a close loop is formed to maintain the self-oscillating. As a result, the switching frequency is no longer limited by the conventional gate transistors, which can be increased to the very high frequency (VHF) range [34]–[36]. A self-oscillating gate driver applied for the full VHF band DC-DC converter is given in [33]. The Class E DC-DC converter is designed to operate at the switching frequency from 30 MHz to 300 MHz.

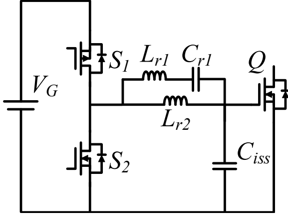


Fig. 9. Multi-resonant gate driver [39].

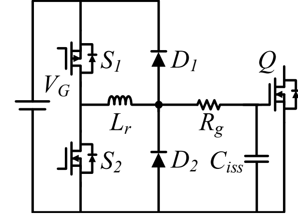


Fig. 10. Efficient power recovery topology [41].

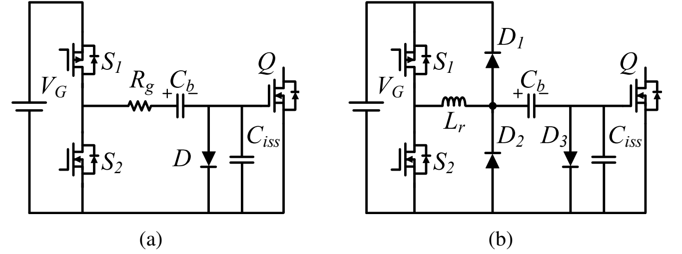


Fig. 11. Resonant gate driver with negative driving voltage: (a) resonant tank topology [42] (b) power recovery topology [43].

Self-oscillating gate driver is utilized in the Class-E inverter part, which is shown as Fig. 8. At the switching frequency of 100 MHz, the gating loss is reported to be 0.29 W according to the simulation result. Other applications of self-oscillating resonant gate driver can be found in [37] for the Class Φ2 inverter and [38] for the flyback converter application. The drawback of the self-oscillating gate driver is that impedance matching must be guaranteed to maintain the oscillation. The inverter stage have to be followed by a rectifier stage designed accordingly to generate the desired self-oscillating gate signal. As a result, application of the self-oscillating gate driver is limited to the resonant converter topologies, which is widely adopted in the power amplifier applications.

C. Zero Initial Inductor Current Resonant Gate Driver

This category of resonant gate drivers share the similar idea as the self-oscillating gate drivers. Instead of the oscillation maintained by the transistor drain-source voltage, the resonant tank is generally connected to the conventional totem pole gate driver and the square-wave voltage is applied to trigger the resonance. As a result, the impedance matching is no longer needed and the resonant gate driver can be easily applied in different topologies for high frequency PWM modulation.

A multi-resonant gate driver designed for Class E power amplifier is proposed in [39], which is shown as Fig. 9. The resonant tank composed by L_{r1}, L_{r2} and C_r, which is designed to pass through the 1st and the 3rd harmonic component. A quasi-square gate signal is generated, which helps to reduce the switching transient and the transistor switching loss. The gate transistors S_1 and S_2 both operate at soft switching condition, which further helps to minimize the gate driver loss. The resonant gate driver is implemented to a Silicon MOSFET (FDMC86248) switching at 20 MHz and the gating loss is reported to be lowered from 1.8 W to 0.72 W compared with the commercial gate driver (LM5114). Further research into this idea for GaN transistor application is demonstrated in [40]. The input capacitor of the GaN transistor is also considered as part of the resonant tank. The proposed gate driver is tested to drive a GaN based 13.56 MHz Class-E inverter (TPH3066PS). The gating loss is reported to be lowered from 0.88 W to 0.80 W compared with the conventional totem pole gate driver.

The resonant gate driver topology with efficient power recovery was first proposed in [41], which is shown as Fig. 10. Resonant inductor L_r is connected between the totem pole bridge and the diode bridge. The freewheeling diodes D_1 and D_2 provide the power recovery path for the excessive inductor energy. For the 500 kHz MOSFET application, the gating loss is reported to be 0.21 W, which is reduced by 55% compared with the conventional gate driver loss. This topology is further researched in [20] to be applied for the integrated circuit (IC) application and the GaN transistor drive. Gating loss is reported to be 0.20 W at 10 MHz from the simulation.

The low power loss of the resonant gate driver has once inspired the research of its application in the GaN based converter. At the early stage of the GaN transistor commercialization, depletion-mode GaN transistor dominates the market, which is the normally-on transistor and requires for negative gate-on voltage [44]. Accordingly, research of resonant gate driver with negative driving voltage was once a popular topic. The resonant gate driver with negative driving voltage shown in Fig. 11(a) is proposed in [42]. C_b and D_3 are installed in the gating path to provide the negative drive voltage. This topology is researched in [45] and applied to drive the normally-on GaN transistor for a 13.56 MHz Class E power amplifier. Based on the similar idea, the energy recovery resonant gate driver with negative gate voltage is given in [43], [46], which is shown as Fig. 11(b). In [46], gating loss is reported to be lowered from 0.11 W to 0.10 W for 1 MHz normally-on GaN transistor application.

The slew rate of the transistor switching must be well designed to guarantee the gating efficiency and reliability. For the conventional gate driver, two gate resistors with different resistance are respectively installed to the gate-on and gate-off path to protect the transistor from over-shoot breakdown, which is especially important for GaN transistor application as the lack of avalanche breakdown and the limited voltage tolerance [16], [48], [49]. The resonant gate driver with controllable slew rate is proposed in [47] for Silicon MOSFET application and further explored in [50] to be applied in GaN transistor application. As shown in Fig. 12, the totem pole output is separated into the charging path and the discharging path, where different resonant inductor are installed to provide

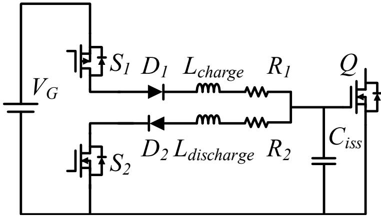


Fig. 12. Separate gate path topology [47].

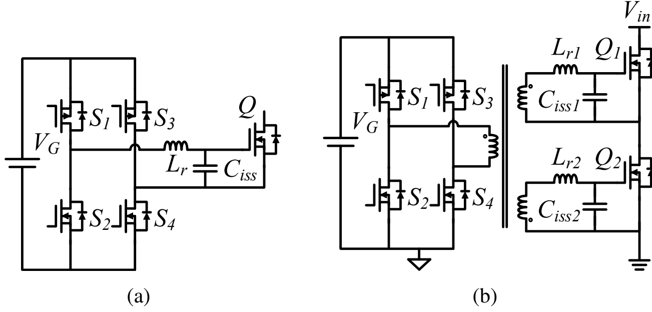


Fig. 13. Full-bridge resonant gate driver: (a) topology for low-side transistor [51] (b) isolated gate driver [52].

asymmetric output. For the Silicon MOSFET application, the resonant gate driver loss is reported to be reduced to less than half of the conventional gate driver loss at 1 MHz switching frequency. For the 600 V commercial GaN transistor application, the gate driver loss is reported be be 0.92 W at 1 MHz switching frequency.

The resonant gate driver in full bridge configuration is capable of providing negative gate voltage and generally applied to drive the MOSFET in high voltage applications. The full-bridge topology proposed in [51] is shown as Fig. 13(a). Compared with the conventional gate driver, the gating loss is reported to be lowered from 9.30 W to 0.90 W at 360 kHz switching frequency. Benefit from this considerate loss reduction, the overall power conversion efficiency is improved from 98.2 % to 99.1 % for the 1 kW half-bridge inverter application. Further research of this topology is carried out in [52], which is shown as Fig. 13(b). A transformer with two secondary windings is integrated in the gate driver to provide isolated and dual-channel gate signal. The gating loss is reduced by 76 % for the 500 kHz MOSFET application.

III. Literature Analysis

A. Prior-art Research Comparison

A thorough review of the resonant gate driver topologies is given in the previous section. Several conclusions can be made to summarize the prior-art research:

- For all the resonant gate drivers, the gating loss is reduced by the same mechanism – the current source is more efficient than the voltage source when charging and discharging the capacitor.
- Majority of the resonant gate drivers are applied in switching frequency around 1 MHz. Self-oscillating gate driver, as a special category, is generally applied in 30 to 300 MHz switching frequency.
- Implementation of the non-zero initial inductor current topology focus on the design of individual current conduction path and power flow path provided by the modulation of gate transistors.
- Implementation of the zero initial inductor current topology focus on the design of resonant tank and gate voltage shaping.
- Recovery of the residue energy within the resonant tank is widely researched in both categories.
- Compared with the conventional gate driver, the resonant gate driver is more efficient in the higher gate voltage applications [25], [32], [53].
- Different from the conventional gate driver, the gating loss is affected by the gate loop resistance. A larger gate loop resistance, resulted from either the gate resistor or the transistor parasitic gate resistance, will lead to extra gating loss [24], [30], [31].

TABLE I
Literature Comparison

Ref.	f_{sw}/MHz	P_{out}/W	GaN transistor	Silicon MOSFET	Switches count
[51]	0.36	1000		✓	4
[41]	0.5	*		✓	2
[52]	0.5	960		✓	4
[30]	1	*		✓	4
[31]	1	50		✓	4
[26]	1	*		✓	4
[46]	1	56	✓		2
[47]	1	*		✓	2
[32]	1	50		✓	4
[29]	2	20		✓	2
[28]	10	5		✓	1
[40]	13.56	*	✓		2
[42]	13.56	4.7	✓		2
[39]	20	32		✓	2
[37]	30	200		✓	0
[33]	100	1.7		✓	0
[35]	110	23		✓	0

To provide an intuitive comparison, the prior-art researched resonant gate driver topologies are summarized in TABLE I and arranged in a descending order of the switching frequency. All collected data is obtained from the literature review and unspecified output power in some research is marked with $''*''$. It shows that the resonant gate drivers have been applied to a wide range of switching frequency, covering the medium frequency range (300 - 3000 kHz), the high frequency range (3 - 30 MHz) and the very high frequency range (30 - 300 MHz). For the medium to high frequency applications, the resonant gate driver is used to maximize the power conversion efficiency. Topologies including extra switches and diodes bridge are all within this range of switching frequency, which helps in the power recovery and further reduces the gate driver loss. For the very high frequency applications, the resonant gate driver is used to overcome the switching frequency limitation from the commercial gate driver. All the resonant gate drivers at very high frequency range adopt the

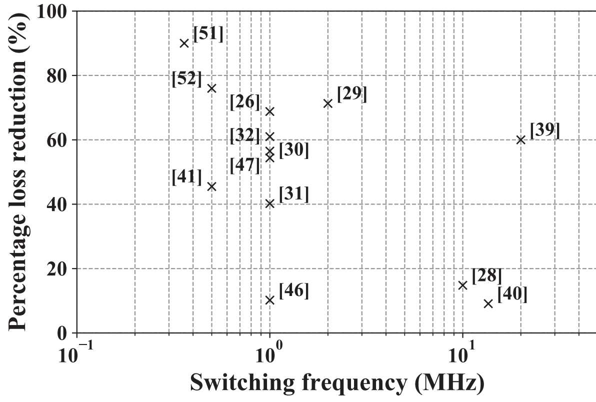
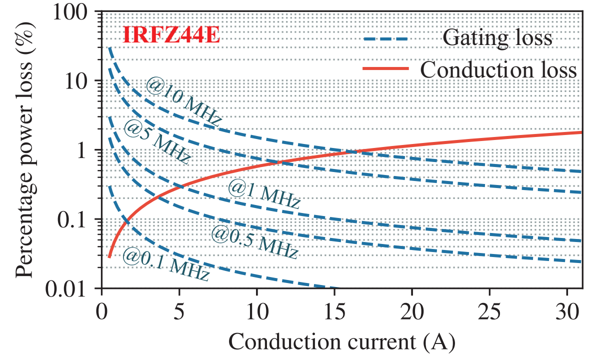
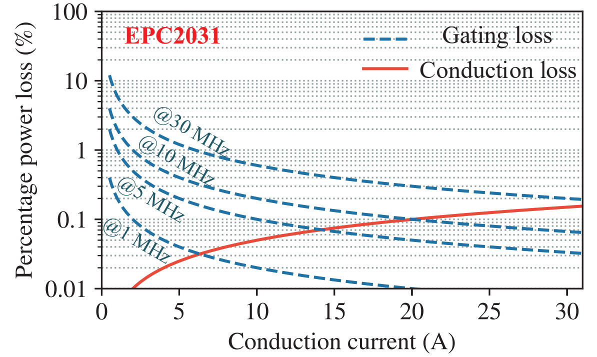


Fig. 14. Percentage loss reduction data collected from the literature review.



(a)



(b)

Fig. 15. Comparison of percentage power loss between gating loss and conduction loss at 40 V drain-source voltage: (a) IRFZ44E Silicon MOSFET (b) EPC2031 GaN transistor.

self oscillating topologies, which completely get rid of the gate transistors and capable of generating the gate signal up to several hundred MHz. From the switches count point of view, less transistors are used in the higher frequency resonant gate driver design. This is resulted from the increasing loss in the gate transistors at higher frequency compared with the gating loss reduction which is irrelevant to the switching frequency. Another limitation is the increasing control complexity for the multiple transistor topologies in higher frequency range.

B. Future Research Topics

The gating loss saving is the major consideration for the resonant gate driver design. To provide an equal comparison between various resonant gate driver topologies, the percentage loss reduction compared with the conventional gate driver is plotted against the switching frequency, which is shown in Fig. 14. The self-oscillating gate driver category is excluded in this plot for the difficulty in separating the gating loss from the converter loss. Although the obtained data is rather scattered in the vertical axis, it can be concluded that the majority of the prior-art research has claimed a percentage loss reduction around 40 - 70 %. The gating loss and the gate driver transistor loss both contribute to the overall gate driver loss, while not all of the prior-art research provides the detailed loss breakdown [31], [54].

It should be emphasized that the application of the resonant gate driver in the GaN based converter is not widely researched. For the very high frequency power conversion, all the researched self-oscillating gate drivers are used to drive the conventional Silicon MOSFET. For the medium to high frequency power converter, only two sets of data from the literature review can be included in Fig. 14, and both of them shows a rather low loss reduction percentage of around 10 % [40], [46]. In [24], the resonant gate driver even shows a higher loss compared with the conventional gate driver, while the advantage of the proposed topology is given as the reduced transistor switching loss. From the prior-art research, necessity of the resonant gate driver in the GaN transistor application is yet not clear. To provide a vision for applying resonant gate driver in the GaN transistor, percentage power loss is compared between the Silicone MOSFET and the GaN transistor. Since transistor switching loss is highly dependent on the switching condition (hard switching or soft switching, modulation scheme and load current), gating loss and conduction loss are included for intuitive comparison. According to the manufacturer data sheet, the gating loss is calculated according to (1) and the conduction loss is calculated as the transistor on-state resistance ohmic loss. Both two calculated loss is then divided by the transistor apparent power to obtain the percentage power loss, which are plotted against conduction current and different switching frequency as shown in Fig. 15.

From the comparison, it shows that the proportion of transistor gating loss is significant at high frequency and low power range. Implementation of the GaN transistor can effectively reduce both the gating loss and the conduction loss, which enables higher frequency applications. For the GaN transistor, gating loss is still comparable to the conduction loss within large range of conduction current and dominant in the high frequency applications. Furthermore, the limited heat dissipation capability of the GaN transistor package should be considered. For example, 0.1 % percentage power loss at 40 V, 5 A switching condition can lead to 9 °C rise on the EPC2031 junction temperature (estimated according to junction-ambient thermal resistance specified in the transistor data sheet). Furthermore, reduced switching loss brought by the resonant gate driver will further helps to improve the GaN

transistor switching efficiency and thermal performance. As a result, research of the resonant gate drive in the GaN transistor application is essential.

IV. Case Study

A. Case Analysis

According to the analysis from the previous section, further research into the resonant gate driver shall focus on the following two topics:

- Comparison of the resonant gate driver topologies with a detailed loss breakdown.
- The effectiveness of applying the resonant gate driver to the GaN based converter.

A case study is carried out in this section to discuss these two problems. Two typical topologies each from one of the major category are compared in details to investigate their application in the Silicon MOSFET and the GaN transistor respectively. Case A is the zero initial inductor topology proposed in [41] and Case B is the non-zero initial inductor current topology proposed in [31], which are shown in Fig. 16. Both of them are representative topologies, which are widely cited and investigated in other prior-art research. Furthermore, these two resonant gate drivers resemble in topology and both designs implement the idea of energy recovery, which makes them ideal for comparison.

The ideal operation waveform of two resonant gate drivers is shown in Fig. 17. Case A topology is composed by a conventional totem pole bridge, a resonant inductor and a schottkey diodes bridge. The input capacitor of Q, along with the resonant inductor is charged during t_0-t_1. Energy recovery takes place during $t_2 - t_3$ and the residue energy within the resonant inductor is returned to the gate voltage source via the path of S_2 body diode, L_r and D_1. In Case B topology, the schottkey diodes bridge is replaced by another totem pole bridge. During $t_0 - t_1$, two totem pole bridges are modulated to charge the resonant inductor via the path of S_2, L_r and S_3. The input capacitor of Q is then charged by the pre-formed inductor current during $t_1 - t_2$. Energy recovery takes place during $t_2 - t_3$ via the path of S_4 body diode, L_r and S_1.

B. Test Benchmark Specification

Test circuit shown in Fig. 18 is implemented for the gate driver comparison. The topology is revised from the conventional double pulse test circuit, which is a general test method for the semiconductor characterization [55]–[57].

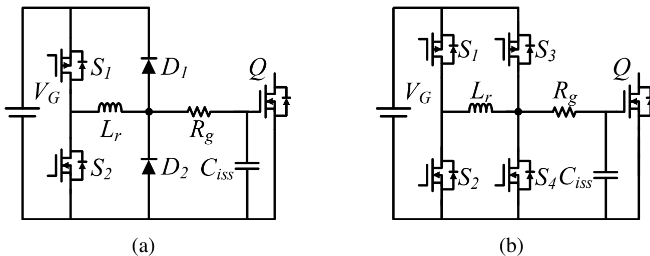


Fig. 16. The resonant gate drivers in comparison: (a) Case A (b) Case B.

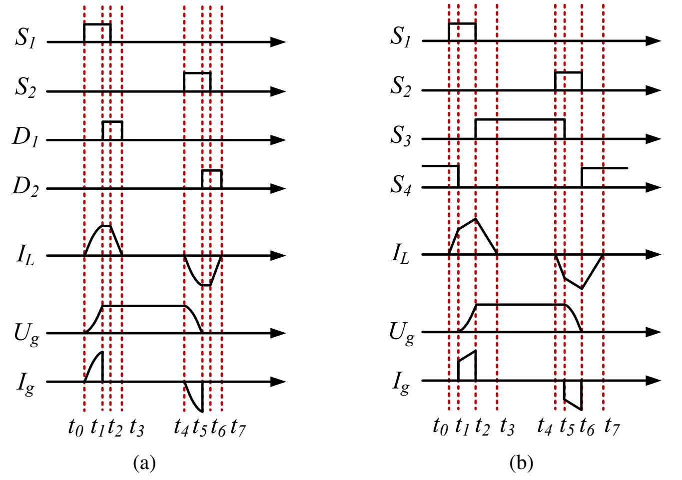


Fig. 17. The idea operation waveform: (a) Case A (b) Case B.

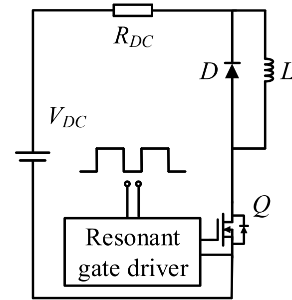


Fig. 18. Topology of the test circuit for the resonant gate driver comparison.

The resistor R_{DC} is installed within the power loop to limit the transistor switching current and guarantees the identical switching condition between different gate driver implementation. The resonant gate driver is each applied with a 50 % duty cycle, 1 MHz square wave digital signal. The inductor L and the schottkey diode D provide the current circuiting path during the transistor Q is switched off. The conventional gate driver, the resonant gate driver from Case A and Case B are implemented respectively to drive the transistor Q.

The transistor Q is picked as the Silicon MOSFET and the GaN transistor respectively for the gate driver loss comparison. The implemented transistor specification is summarized in TABLE II. Two transistors are of the same power rate. Benefit from the wide band-gap semiconductor characteristics, GS66516B has a lower gate charge Q_g and requires for lower gate voltage V_G, which leads to a much lower gating loss compared with the Silicon MOSFET IPW60R045CP. IRF6617 is used as the gate driver transistor in both cases. The resonant inductor is chosen according to the design rules specified in each paper and the equations for inductance calculation are shown as (2) and (3) respectively

$$L_{r_A} \leq \frac{1}{C_G}\left(\frac{2t_{rise}}{\pi}\right)^2, \tag{2}$$

$$L_{r_B} = \frac{t_{rise}}{C_G}\left(\frac{t_{rise}}{4} + t_d\right), \tag{3}$$

TABLE II
COMPARISON OF THE IMPLEMENTED TRANSISTOR

	IPW60R045CP	GS66516B
Semiconductor material	Silicon	Gallium Nitride
V_{DS}	650 V	650 V
I_D	60 A	60 A
Q_g	150 nC	12.1 nC
V_G	+15 V, -12 V	+6 V, 0

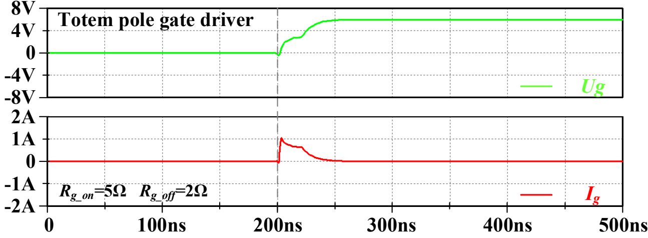
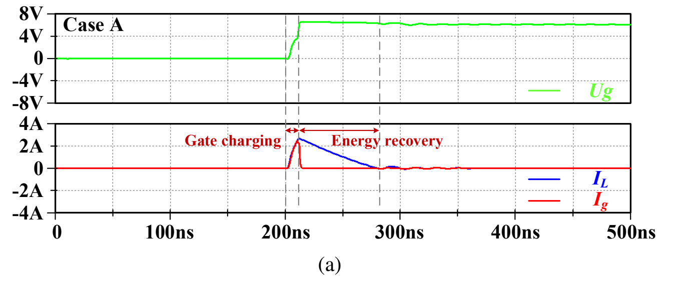


Fig. 19. Simulation waveform of the totem pole gate driver.



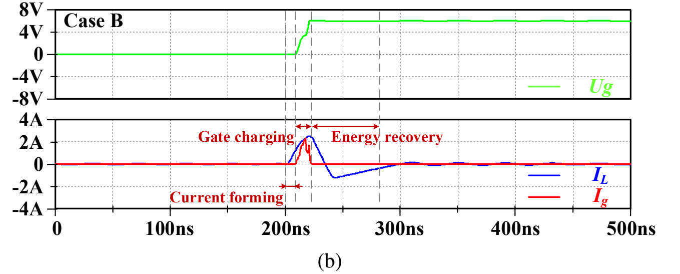


Fig. 20. Simulation waveform: (a) Case A (b) Case B.

where t_{rise} is the gate voltage rising duration ($t_0 - t_1$ in Case A and $t_1 - t_2$ in Case B) and t_d is the inductor pre-charging duration ($t_0 - t_1$ in Case B). Comparison of results is given in the LTSpice simulation, which is ideal for topology comparison in order to provide the highly identical operation condition between different cases. Furthermore, the power loss on each circuit component can thus be obtained individually, which are used to provide a thorough analysis of the gate driver loss decomposition.

C. Comparison of Results

1) gate waveform comparison: Both topologies in Case A and Case B were originally proposed for the Silicon MOSFET application. The gate waveform is given for comparison in the GaN transistor application at 1 MHz switching frequency. The gate wave form of the conventional gate driver and the resonant gate driver is given in Fig. 19 and Fig. 20 respectively, where U_g is the gate voltage, I_g is the gate current and I_L is the inductor current. For the conventional totem pole gate driver, the switching transient is rather slow. The peak gate current reaches 1 A and decreases rapidly during the gating process. The resonant gate drivers in both cases provide a larger gate current with the peak value of 2 A and thus the switching transient is shortened. The gate energy recovery process can be observed in both two cases. In the Case B, the current forming stage can be seen before the gate charging stage. Also, there's a noticeable current ringing in the resonant inductor during the energy recovery stage in Case B, which is resulted from the oscillation of resonant inductor and the parasitic capacitor of the gate transistors. From the simulation results, it can be concluded that resonant gate drivers in both Case A and Case B show well feasibility in GaN transistor application.

2) switching loss comparison: A larger gate current provided by the resonant gate driver helps to reduce the switching transient, and thus reduces the switching loss of Q. For the conventional gate driver, the gate current is regulated by the gate resistor. For the resonant gate driver, the gate current is regulated by the charging duration of the resonant inductor, which can be increased in modulation control or a smaller inductor selection. The switching loss characterization of GS66516B is obtained by adopting the conventional gate driver and two resonant gate drivers respectively, as shown in Fig. 21.

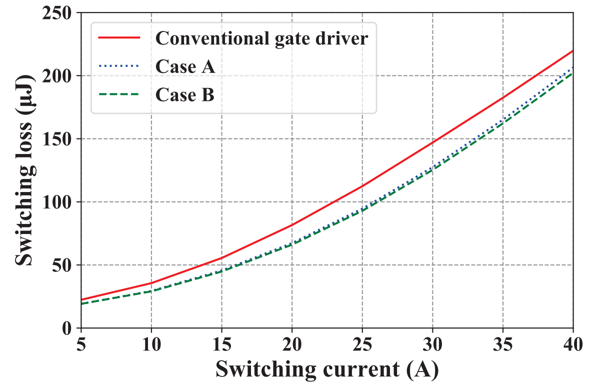


Fig. 21. The switching loss characterization of GS66516B.

At 400 V drain-source voltage, the switching loss of GS66516B is obtained with the source current ranging from 5 A to 40 A. The switching loss characterization obtained from Case A and Case B resembles each other, which is resulted from the similar gate current in two cases. Compared with the conventional totem pole gate driver, there's a noticeable reduction of the switching loss. At the 40 A source current condition, the switching loss of GS66516B can be reduced by 7.7 % when using the resonant gate driver.

3) gate driver loss comparison: To provide a thorough comparison of the gate driver loss, a detailed loss breakdown is given. The total gate driver loss is composed by:

- The internal CV^2 loss, which is defined as the power loss on the parasitic gate resistance of Q.

TABLE III
GATE DRIVER LOSS FOR SILICON MOSFET APPLICATION

	totem pole	Case A	Case B
internal CV^2 loss	0.78 W	0.84 W	0.77 W
external CV^2 loss	3.65 W	*	*
gate transistor loss	0.45 W	0.79 W	1.29 W
total	4.88 W	1.63 W	2.07 W

TABLE IV
GATE DRIVER LOSS FOR GAN TRANSISTOR APPLICATION

	totem pole	Case A	Case B
internal CV^2 loss	0.01 W	0.04 W	0.03 W
external CV^2 loss	0.12 W	*	*
gate transistor loss	0.02 W	0.10 W	0.12 W
total	0.15 W	0.14 W	0.15 W

- The external CV^2 loss, which is defined as the power loss on the gate resistor
- The gate transistor loss, which is defined as the power loss on the transistor S. The loss on the diode bridge in Case A is also included in this part for simplicity.
- The logic loss, which is defined as the power loss on the signal generation provided to the gate transistor.
- The core loss and copper loss, which is defined as the power loss on the resonant tank.

The gating loss is generally considered as the sum of the internal CV^2 loss and the external CV^2 loss. For the conventional gate driver, sum of the internal and external gate resistance only matters in controlling the slew rate of the transistor Q. A lower gate resistor selection will not help in the gate driver loss reduction, which has been proved in [41]. For the resonant gate driver, the resonant tank replaces the conventional gate resistor and the gating loss equals to the internal CV^2 loss. Extra parasitic gate resistance from the transistor Q will lead to higher internal CV^2 loss. As a result, the transistor with a lower gate resistance is preferred in the resonant gate driver application. The gate transistor loss can be reduced by adopting the gate transistor with low on-resistance and small output capacitance. In the case study, IRF6617 from International Rectifier is used as the gate transistor for all three topologies and RBR10NS30A from Rohm is used to compose the Schottky diodes bridge in Case A. The logic loss and, the core loss and copper loss of the inductor are much smaller than the other loss sources and also difficult to be generally quantified for various application scenarios, which are omitted in the loss comparison.

The gate driver loss breakdown for the Silicon MOSFET application is shown in TABLE III. Compared with the conventional totem pole gate driver, the gating loss is largely reduced by 81.0 % and 82.6 % in Case A and Case B respectively. This comes with the price of extra gate transistor loss and the total gate driver loss is reduced by 66.6 % and 57.6 % in Case A and Case B respectively. In some prior art research, the percentage loss reduction is not clearly defined as the total gate driver loss or the gating loss, which explains the scattered data points collected in the Fig. 14.

The gate driver loss breakdown for the GaN transistor application is shown in TABLE IV. The gating loss is reduced by 71.9 % and 77.3 % in Case A and Case B respectively. However, the gating loss of the GaN transistor is much lower and comparable to the gate transistor. Extra gate transistor loss in Case A and Case B contributes to the majority of the total gate driver loss. Percentage reduction of the total gate driver loss is negligible.

Furthermore, it should be noted that the internal CV^2 loss of the resonant gate driver is 3 to 4 times higher than the conventional gate driver, which is resulted from the increased gate charge/discharge current. The internal CV^2 loss will result in heating within the GaN transistor package, which should not be neglected considering the limited heat dissipation capacity resulted from the chip scale package. Case A and Case B are similar in percentage loss reduction for both Silicon MOSFET and GaN transistor application.

In comparison of the two resonant gate drivers, the gate charge current in Case A is decided by the resonant inductor, while in Case B is on-line changeable according to the phase shift modulation. For the resonant gate driver, design of the gate charge current is trade-off between the transistor gating loss and switching loss. Thus, Case B topology brings more flexibility in the varioius applications, especially considering the PCB inductor technique widely adopted in the Case A topology. On the other hand, implementation of Case B topology comes with the price of extra gate transistor loss, extra effort in inductor selection and more control complexity.

V. CONCLUSIONS

A thorough review of the resonant gate driver is given in this paper. Topology comparison is given between the two general groups of the resonant gate driver categorized by the initial inductor current. For the medium to high frequency application, topologies with extra transistor or diode bridge are widely used, which introduces more control flexibility to further minimize the gating loss. For the very high frequency application, the self-oscillating topologies are generally used to get rid of the gate transistor and maximize the switching frequency. A case study is carried out to investigate the application of two typical resonant gate driver topologies. For the Silicon MOSFET application, the CV^2 loss contributes to the majority of the total gate driver loss. The resonant gate driver is effective in both CV^2 loss reduction and the total gate driver loss reduction. For the GaN transistor application, the gating loss is comparable to the gate transistor loss. The resonant gate drivers are effective in the CV^2 loss reduction, but lead to much more loss in the gate transistors. As a result, the total loss of resonant gate driver is not evidently reduced and potentially higher than the conventional gate driver if the extra inductor loss and digital loss are taken into account. Benefit of the resonant gate driver in the GaN based converter application is validated in the switching loss reduction, which is resulted from its fast charging/discharging capability.

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