A Compensation Way for A Differential Pair to Achieve A High Performance Single-ended to Differential Converter

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***Abstract*— An improved technique is presented for a differential pair operating as a single-ended to differential converter. Common source stages are used to compensate the output amplitude difference, and a resistor in series with a dummy transistor is in parallel with only one common source stage to compensate the output phase difference. The simulation results show that for the output differential signal, HD2 < -48.5 dBc, HD3 < -50.5 dBc, the amplitude difference < 4.5% and the absolute phase difference < 3° with 0.18 μm-CMOS technology, over the frequency range from 1.6 GHz to 2.4 GHz. The simulation results agree with the improved technique well.**

I. INTRODUCTION

Differential signals are widely used in high-speed signal processing today, but single-ended to differential converters (SDCs) are rarely reported, especially CMOS wideband and high linearity ones. A linear tunable SDC using bipolar technology has achieved a bandwidth of 120 MHz and the phase difference smaller than 25° [1]**.** A rat-race circuit SDC using InP-based HEMT technology has achieved 80 GHz operation frequency, but it consumes a big die area. A SDC using MBE-grown-metamorphic-InGaAs/InAlAs technology through inserting a delay-line asymmetrically in one output signal path to compensate the phase difference has achieved less spread group-delay over operation bandwidth of 42 GHz [3]. [2] and [3] are used for digital signals and the linearity is not very important.

For simple application, people usually use a differential pair followed by another differential pair as a SDC, this can compensate for the amplitude difference, but cannot effectively improve the difference of phase. In this paper a compensation way is presented, and a high linearity low phase difference SDC is achieved.

II. MECHANISM OF THE OUTPUT DIFFERENCE IN A TRADITIONAL SDC

The conventional SDC is shown in Fig. 1(a). It is a differential pair with an input terminal biased at a reference of constant DC voltage V_{ref}. Fig. 1(b) shows the output waveforms of the traditional SDC. There are differences in both phase and amplitude. This is mainly because of the parasitic capacitance at node A in Fig. 1(a) and the finite output impedance of the current mirror transistor M3.

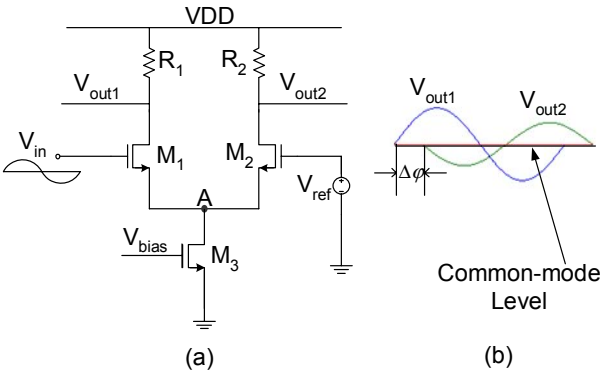

Fig. 1 A simple differential pair SDC (a) circuit, (b) the output waveform, Δφ is the phase difference between V_{out1} and V_{out2}.

The mechanism of the output difference is analyzed as follows. For simplicity, here the second and higher order effects (e.g. channel length modulation and body effect) of M1 and M2 are neglected. As explained in [4], M1 operates as a common source stage with a degeneration resistance R_S shown in Fig. 2(a), R_S is equal to the impedance seen

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looking into the source of M2 $1/g_{m2}$ in parallel with $1/sC_A$ and $ro3$,

$$R_S = 1/g_{m2} \,||\, 1/sC_A \,||\, ro3 \tag{1}$$

where ,

C_A = the total parasitic capacitance at node A

$ro3$ = the output resistance of M3

g_{m2} = the transconductance of M2

Then V_{out1} is obtained as,

$$V_{out1} = \frac{-R_1 g_{m1}}{1 + g_{m1} R_S} V_{in} \tag{2}$$

where,

g_{m1} = the transconductance of M1.

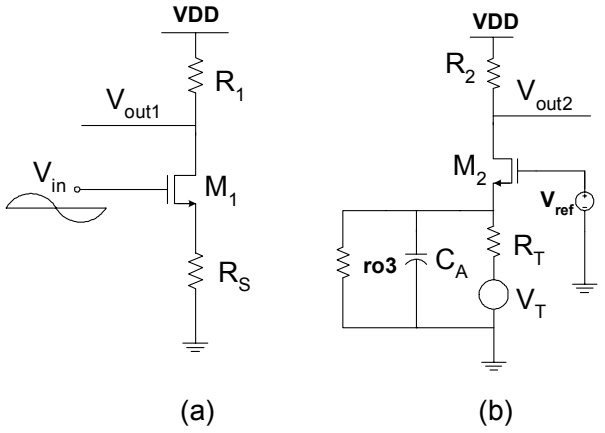

Fig. 2 (a) Equivalent circuit of M1 viewed as a common source stage degenerated by M2. (b) Equivalent circuit of M2 viewed as a common gate stage with replacing M1 by a Thevenin equivalent circuit

In Fig. 1(a), M2 operates as a common-gate circuit and M1 drives M2 as a source follower. To obtain V_{out2}, the equivalent circuit is shown in Fig. 2(b), where V_{in} and M1 are replaced by a Thevenin equivalent circuit: the Thevenin voltage $V_T = V_{in}$ and the resistance $R_T = 1/g_{m1}$. Then V_{out2} is,

$$V_{out2} = \left(1 - \frac{1}{1 + g_{m1}(1/g_{m2} \,||\, 1/sC_A \,||\, ro3)}\right) R_2 g_{m2} V_{in}$$

$$= \left(1 - \frac{1}{1 + g_{m1} R_S}\right) R_2 g_{m2} V_{in}. \tag{3}$$

Because V_{out1} and V_{out2} have the opposite polarity, so the difference ΔV_{out} between them is the addition of these two values,

$$\Delta V_{out} = V_{out1} + V_{out2} = \frac{R_2(g_{m2} R_S) - R_1}{1 + g_{m1} R_S} g_{m1}. \tag{4}$$

Since (1), if M3 is replaced by an ideal current mirror which means $C_A = 0$ and $ro3 = \infty$, then for $R_1 = R_2$, $\Delta V_{out} = V_{out1} + V_{out2} = 0$. This explains that in ideal conditions, a simple differential pair can be a perfect SDC. In (4), R_S is a complex variable, consequently ΔV_{out} is also a complex variable including the difference of both amplitude and phase. Because M1 drives M2, owing to C_A, V_{out2} lags behind V_{out1}.

III. CIRCUIT DESIGN

Based on (4) and the above analysis, the proposed topology of SDC is shown in Fig. 3. To gain high performance, the following aspects have been considered.

a) Small dimentions of M1, M2 and M4 are used to decrease C_A, this increases R_S in (1).

b) Increasing the length of M3 will increase $ro3$. Both a) and b) increase R_S in (1) and make R_S much close to $1/g_{m2}$, Since $R_1 = R_2$, then $\Delta V_{out} = V_{out1} + V_{out2} \to 0$. M4 is a small dimention transistor which makes the capacitance at point A small and due to its operating in triode region , it affects the headroom slightly.

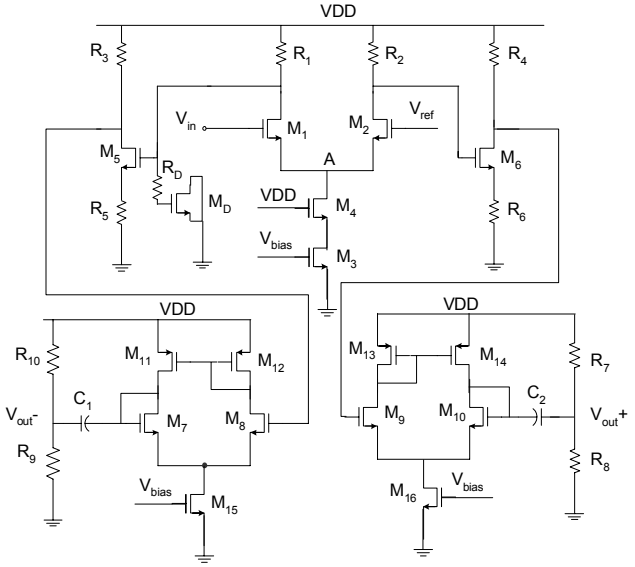

Fig. 3 Proposed SDC circuit.

c) Since $R_S = 1/g_{m2} \,||\, 1/sC_A \,||\, ro3 < 1/g_{m2}$, then $g_{m2}R_S < 1$, $R_2(g_{m2}R_S) < R_2$. So in order to make ΔV_{out} close to zero, the simple way is to modify the value of load resistors, e.g. to increase R_2 or decrease R_1, but this makes the input common-mode noise corrupt the amplified differential signal[4] and directly introduces a systematic offset, so $R_1 \neq R_2$ is not a choice.

d) Common source stages M5 and M6 are used to adjust the amplitude difference. Keeping the resistors $R_3 + R_5 = R_4 + R_6$ makes the amplitude difference less sensitive to the variation of supply voltage.

e) M_D is a dummy transistor providing extra parasitic gate capacitance to delay V_{out1} then decrease the phase difference between $V_{out}-$ and $V_{out}+$. The gate capacitance of M_D and resistor R_D also will decrease the load of M1, it affects the output amplitude slightly due to the small gate capcitance of M_D.

f) M7~M16 constitute two unity gain buffers, which make the outputs of the common source stages less sensitive to the variation of their loads. C_1, C_2, and $R_7 \sim R_{10}$ are simply used to rebuild the common mode level.

IV. SIMULATION RESULTS

Spectre is used to simulate the proposed SDC circuit using 0.18-μm CMOS technology. The component dimensions and circuit parameters are given in TABLE I.

TABLE I. COMPONENT DIMENSIONS AND CIRCUIT PARAMETERS

M1 M2	1.2/0.2 μm/μm
M3	30.0/1.0 μm/μm
M4	0.6/0.5 μm/μm
M5	0.7/0.2 μm/μm
M6	0.95/0.2 μm/μm
M7~M10	1.0/0.2 μm/μm
M11~M14	5.0/0.2 μm/μm
M15 M16	30.0/1.0 μm/μm
M_D	0.85/0.2 μm/μm
R_D	2.2 KΩ
R_1 R_2	9.0 KΩ
R_3 R_4	2.5 KΩ
R_5 R_6	500 Ω
VDD	1.8 V
I_{D3}	107 μA
I_{D5}	195 μA
I_{D6}	240 μA
I_{D15} I_{D16}	148 μA

The circuit is simulated with applying 200 mV_{pp} input, common-mode level 1.3 V and over the frequency range from 1.6 GHz to 2.4 GHz. Fig. 4 shows an example waveform of the input and output at 2 GHz. Fig. 5 shows the relation between phase difference and different variables including: frequency, variation ration of resistor, variation ratio of (W/L) of M_D and variation ratio of (W/L) of M5. In simulation, the variations of all the resistors are assumed to increase or decrease with the same ratio simultaneously. The variation ratio of (W/L) is assumed that both width and length of a transistor vary by the same ratio simultaneously. With careful layout, the above two assumptions can be realized. In Fig. 5, (b), (c) and (d) are simulated at 2 GHz. (c) and (d) show the worst performance of phase difference, but with careful layout the effect of M5 can be partly compensated by M6, only if the dimension of M5 and M6 vary synchronously. Fig. 6 shows the second and third order harmonic distortion of the output differential signal with frequency, variation ratio of resistor, variation ratio of (W/L) of M_D and variation ratio of (W/L) of M5.

TABLE II. CIRCUIT PERFORMANCE SUMMARY

Parameter	Frequency (1.6 GHz ~2.4 GHz)	Variation ratio of resistors (-0.2 ~ 0.2)	Variation ratio of (W/L) of M_D (-0.1 ~ 0.1)	Variation ratio of (W/L) of M5 (-0.1 ~ 0.1)	Variton of input (50~300 mVpp)
HD2 of Differential (dBc)	< -51.5	< - 48.5	< -50.5	< -49.0	<-48.0
HD3 of Differential (dBc)	< -53.5	< -50.5	< -54	< -53.5	< -47.0
Phase Difference (deg)	0.5 ~ -0.3	0.6 ~ 0	1.8 ~ - 1.5	1.2 ~ - 1.5	-1.0 ~ 1.0
Amplitude difference	<4.5%				

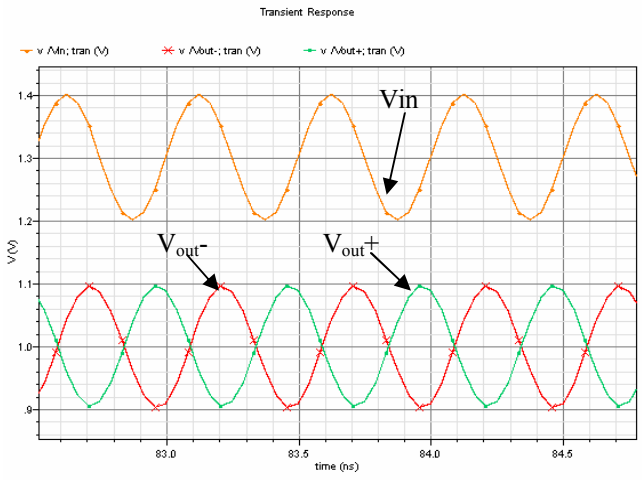

Fig. 4 An example waveform of input output @ 2 GHz

Fig. 7 shows the phase difference and harmonic distortion with the variation of input amplitude.

The amplitude difference is smaller than 4.5%, in all the above conditions. The simulation results of the proposed SDC in Fig. 3 are summarized in TABLE II.

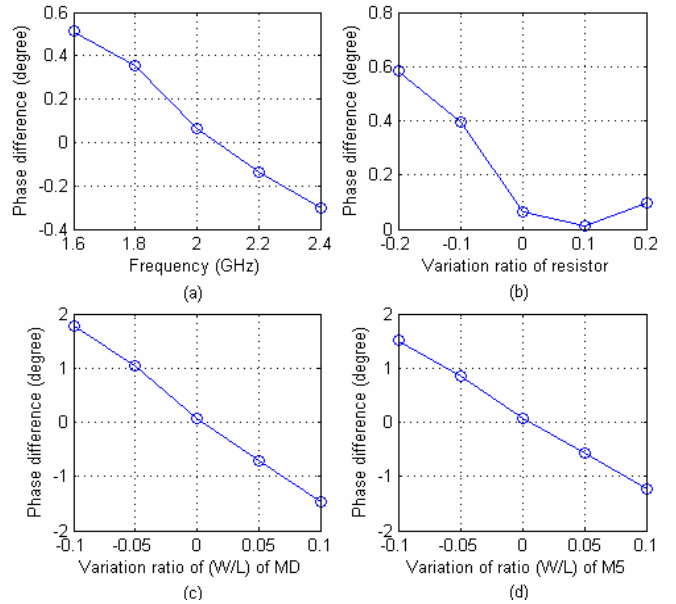

Fig. 5 Phase difference with (a) frequency, (b) variation ratio of resistor, (c) variation ratio of (W/L) of M_D, (d) variation ratio of (W/L) of M5.

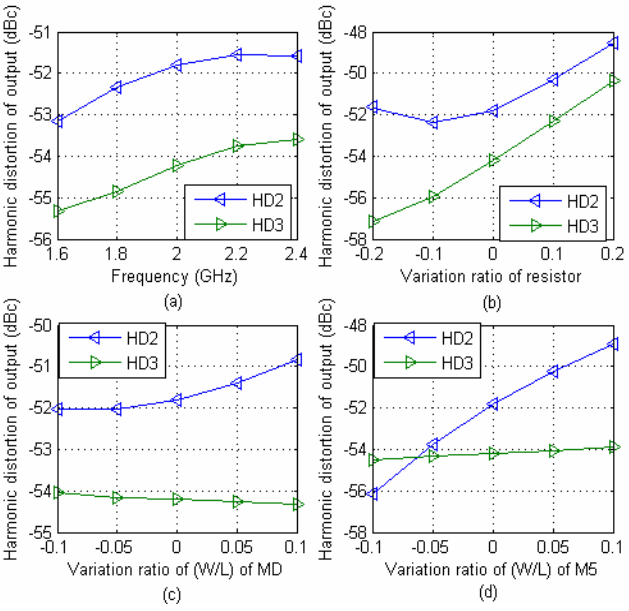

Fig. 6 The second and third order harmonic distortion with (a) frequency, (b) variation ratio of resistor, (c) variation ratio of (W/L) of M_D, (d) variation ratio of (W/L) of M5.

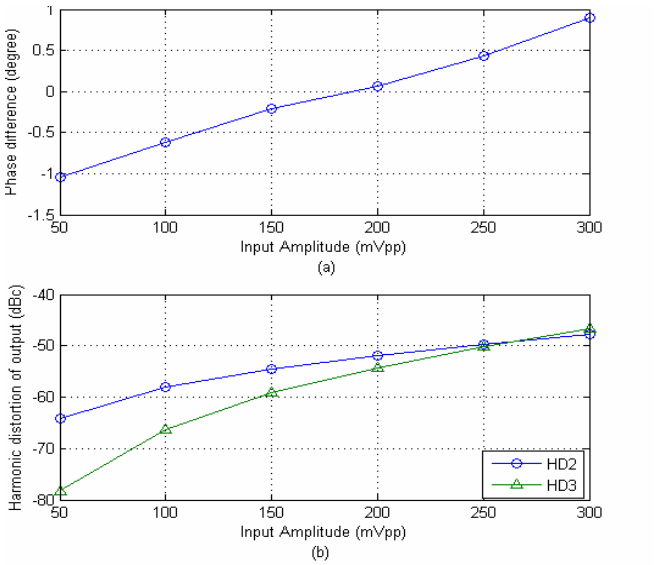

Fig. 7(a) Phase difference with the variation of input amplitude, (b) the second and third harmonic distortion with the variation of input amplitude.

V. CONCLUSION

The mechanism of the output difference in phase and amplitude in a simple differential pair SDC is analyzed, the compensation technique is proposed. The simulation results show with a careful layout an absolute phase difference smaller than 3° and amplitude difference smaller than 4.5% can be expected. The simulation results demonstrate the feasibility of the proposed circuit. This circuit is designed for testing chip in library and the center frequency can be set at the interest frequency according to application. The frequency arrange from 1.6 GHz to 2.4 GHz in this design is only to show this compensation technique can achieve a relatively wide bandwidth.

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