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A Complete Small-Signal MOSFET Model and Parameter Extraction Technique for Millimeter Wave Applications

YANG CAO [1], WEI ZHANG [1], JUN FU [2], QUAN WANG [3], LINLIN LIU [3], AND AO GUO [3]

1 School of Microelectronics, Tianjin University, Tianjin 300072, China
2 Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, Beijing 100084, China
3 Application Development Department, Shanghai Integrated Circuit Research and Development Center, Shanghai 201210, China

CORRESPONDING AUTHOR: Y. CAO (e-mail: yangcaoa5977@126.com)

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ABSTRACT In this paper, we propose a parameter extraction method for a complete MOSFET small signal equivalent circuit model addressing nearly all the parasitic and non-quasi-static (NQS) effects. Extraction and de-embedding of drain/source/gate series resistances and the substrate network are found to be necessary for obtaining the intrinsic elements of the small-signal equivalent circuit. We demonstrate for the first time, a step-by-step procedure for the extraction and de-embedding of the extrinsic model parameters directly from measurements. As a result, a precise intrinsic parameters derivation in the saturation region is presented. Moreover, for the intrinsic small signal equivalent circuit, a gate drain branch is supplemented in parallel to describe parasitic gate-drain coupling under high frequency up to 60 GHz together with the NQS effects. Finally, the presented parameter extraction method is verified by comparing with the corresponding measurement data from the 40-nm RF CMOS process of Shanghai Huali Microelectronics Corporation.

INDEX TERMS MOSFET, millimeter wave, parameter extraction, small-signal model.

I. INTRODUCTION

As MOSFETs are scaled down to improve the integration density and electrical performance for millimeter wave (MMW) applications, the parasitics become increasingly complicated in integrated circuits [1]–[3]. Accurate modeling of MMW MOSFETs requires proper characterization of both intrinsic and extrinsic parts. The extrinsic parasitics at gate, drain, source and substrate may play a more crucial role than intrinsic ones in very high frequency. Once the extrinsic parasitics are accurately extracted and de-embedded, intrinsic components could be achieved.

A lot of effort has already been put into characterizing and extracting extrinsic parasitics. For instance, the technique took the intrinsic elements into account under different bias conditions is applied in some works for extracting the series impedances [4], [5]. However, the method is made possible by approximating the equivalent circuit until it is simple enough.

The cold extraction method (Vds=Vgs=0V) [6] assumes that the intrinsic part is purely capacitive and therefore bias-independent series parasitics are easily extracted. However, the resistances extraction when substrate loss and gate-substrate coupling effect are considered is still not fully discussed when the cold strategy is used in previous work [4], [6].

In this paper, a parameter extraction method that suffers from none of the above limitations is proposed for a complete MMW MOSFET small signal equivalent circuit model addressing nearly all the parasitic and NQS effects. We have fully considered the layout-dependent resistive/capacitive parasitics and substrate loss of the HLMC 40nm MOSFETs. In the next section, complete small-signal NMOS equivalent circuit models on zero-bias (Vds=Vgs=0V) and saturation region are presented. The extraction of extrinsic parasitics and intrinsic elements are solved in Sections III and IV, respectively. In Section V, the presented parameter extraction method is verified by comparing with the corresponding

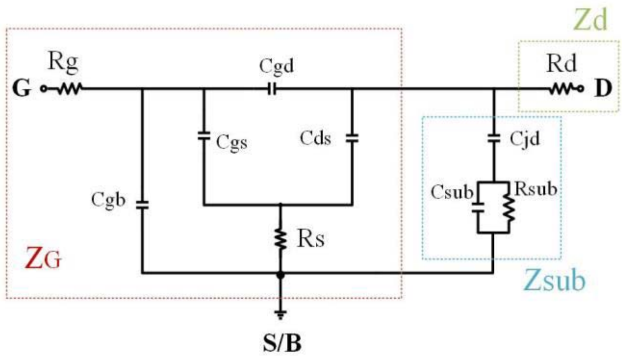

FIGURE 1. A MOSFET small-signal equivalent circuit model under zero-bias.

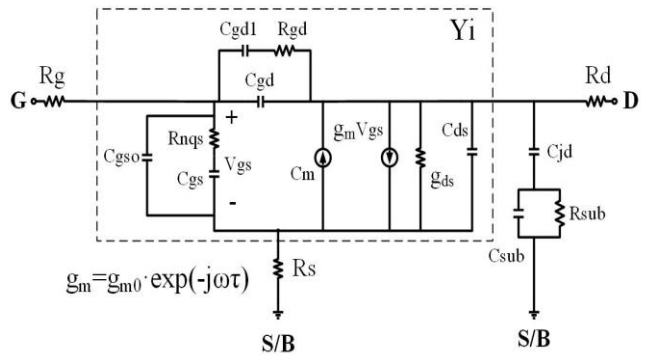

FIGURE 2. A complete MOSFET small-signal equivalent circuit model in saturation region.

measurement data. Concluding remarks are given in Section VII.

II. COMPLETE SMALL-SIGNAL MOSFET EQUIVALENT CIRCUIT MODELS

A set of NMOS transistor test structures fabricated on the 40nm RF CMOS process of Shanghai Huali Microelectronics Corporation (HLMC) are measured up to 60GHz for investigating the small-signal MOSFET modeling and parameter extraction. Standard open-short de-embedding is performed on the measured S-parameters since this method is thought to be still effective below 60GHz [7]. The MOSFET is designed as a two-port network with source and bulk connected to ground, gate as input and drain as output respectively.

Under zero-bias, the MOSFET equivalent circuit model with the intrinsic part consisting of three capacitances is shown in Fig. 1. R_g, R_s, and R_d are gate/source/drain series resistances, respectively. The substrate effect is modeled as a RC network different from the only-resistive substrate model [8] and C_{jd} is the drain-to-bulk junction capacitance. In addition, the C_{gb} for characterizing gate-bulk coupling effect is added in the equivalent circuit. In extrinsic parasitics extraction, series resistance and substrate effect are assumed to be bias independent or at least have weak bias dependence.

Fig. 2 shows a complete small-signal model addressing nearly all the parasitic and NQS effects in the saturation region. C_{gs} is the inversion-charge capacitance and the resistance R_{nqs} represents the effective channel resistance seen by the signal flowing via C_{gs} from gate to source [9]. C_{gso} represents the gate-to-source overlap and fringing capacitances. Since the inversion channel acts as a conductive shield, C_{gb} becomes much less than the other capacitances and then, it can be neglected [8], [10]. Note that, the controlling voltage is the total voltage V_{gs} across the R_{nqs} and C_{gs}. $C_m = C_{dg} - C_{gd}$ is a trans-capacitance taking care of the different effects of the gate and drain on each other in terms of charging currents [11]–[13]. The gate-to-drain overlap and fringing capacitances are merged with the corresponding intrinsic capacitance C_{gd}. In addition, a gate-drain branch consisting of C_{gd1} and R_{gd} paralleled with C_{gd} is added to accurately model the frequency dependence of coupling effects arising from non-ideality parasitics in high frequency region in this work [6]. C_{ds} is the drain-to-source intrinsic capacitance. This paper gives a complete extraction procedure for extracting all the above parameters.

III. EXTRACTION OF EXTRINSIC ELEMENTS

The conventional T-type equivalent circuit model [4], [6] in fact does not fully consider the layout-dependent gate and substrate parasitics under zero-bias. Therefore, we propose a step-by-step procedure for the extraction and de-embedding of the extrinsic elements for a more complete model as shown in Fig. 1 in this section.

We first give an extraction of R_d parameter. To extract R_d from the measured data, the following equations derived from Fig. 1 are used.

$$Z_{11} = Z_{G,11} - \frac{Z_{G,12} \cdot Z_{G,21}}{Z_{sub} + Z_{G,22}} \tag{1}$$

$$Z_{12} = \frac{Z_{G,12} \cdot Z_{sub}}{Z_{sub} + Z_{G,22}} \tag{2}$$

$$Z_{21} = \frac{Z_{G,21} \cdot Z_{sub}}{Z_{sub} + Z_{G,22}} \tag{3}$$

$$Z_{22} = \frac{Z_{G,22} \cdot Z_{sub}}{Z_{sub} + Z_{G,22}} + Z_d \tag{4}$$

In the high-frequency region (40GHz-60GHz), equation (5) is reasonable for Mag ($Z_{G,22}$) becomes much less than Mag (Z_{sub}) with increasing frequency [14]. Then, the value of R_d can be extracted by equation (6), where A_d is expressed as a function of other parameters under zero-bias and the detail of A_d in (6) is listed in the Appendix (1).

$$Real(Z_{22} - Z_{12})\_HF \approx R_d + Real\big(Z_{G,22} - Z_{G,12}\big) \tag{5}$$

$$Real(Z_{22} - Z_{12})\_HF \approx R_d + A_d/\omega^2 \tag{6}$$

The linear regression is performed to the measured high-frequency data of Real$(Z_{22} - Z_{12})$ with regard to ω^{-2} for a HLMC 40nm NMOS transistor, which has 32 fingers and a gate width of 5μm for each finger as shown in Fig. 3. The intercept with the Real$(Z_{22} - Z_{12})$ axis is used as an initial guess of $R_d = 1.98\Omega$. Before the substrate parameter extraction, the extracted R_d has to be subtracted for obtaining Y^d parameters.

The substrate network may affect the extraction of the model parameters, including source and gate resistances at high frequencies. Therefore, the substrate network should be de-embedded for R_g extraction. Cold extraction technique [15] is used in this letter to extract substrate parameters of the model (i.e., R_{sub}, C_{sub}, and C_{jd}). The details are shown in the following equations,

$$Real\left(Y_{22}{}^{d}+Y_{12}{}^{d}\right)=\left(a_1\omega^2\right)/\left(1+a_2\omega^2\right) \tag{7}$$

$$Imag\left(Y_{22}{}^{d}+Y_{12}{}^{d}\right)/\omega=C_{jd}\cdot\left(\left(1+b_1\omega^2\right)/\left(1+a_2\omega^2\right)\right) \tag{8}$$

where $a_1 = R_{sub}C_{jd}{}^2$, $a_2 = R_{sub}{}^2(C_{sub}+C_{jd})^2$, and $b_1 = R_{sub}{}^2C_{sub}(C_{sub}+C_{jd})$. We can solve for R_{sub} and C_{sub} as: $R_{sub} = a_1/C_{jd}{}^2$ and $C_{sub} = ((C_{jd}{}^2\cdot\sqrt{a_2})/a_1) - C_{jd}$.

The a_1, a_2, and C_{jd} can be extracted using the frequency response at zero-bias. At lower frequencies, (7) and (8) are approximated as $\mathrm{Real}(Y_{22}{}^{d}+Y_{12}{}^{d}) \approx a_1\omega^2$ and $Imag(Y_{22}{}^{d}+Y_{12}{}^{d})/\omega \approx C_{jd}$, respectively. At high frequencies, (7) is approximated as $\mathrm{Real}(Y_{22}{}^{d}+Y_{12}{}^{d}) \approx a_1/a_2$. Then a_1, C_{jd}, a_2, and thus R_{sub} and C_{sub} are obtained. Using extracted values at zero-bias, it is determined that $C_{jd} = 72$fF, $R_{sub} = 55\Omega$ and $C_{sub} = 414$fF.

Next, R_g can be extracted from Z_G-parameters after de-embedding the Z_d and Z_{sub} as defined in Fig. 1. In the high-frequency region (40GHz-60GHz), equation (9) gives the extracted $R_g = 4.6\Omega$ as shown in Fig. 3. Here A_g is analogous to A_d and the detail of A_g is shown in the Appendix (2). So far, R_d, R_g, and substrate parameters have been extracted.

$$Real\left(Z_{G,11}-Z_{G,12}\right)\_HF \approx R_g + A_g/\omega^2. \tag{9}$$

IV. INTRINSIC PARAMETER EXTRACTION

After de-embedding of R_d, R_g, and substrate parameters, the Z_{in}-parameters of the T-type equivalent circuit with R_s in the saturation region are obtained. Before the intrinsic parameters extraction, R_s can be accurately extracted by using equation (10) in the high-frequency region (40GHz-60GHz), where A_s is expressed as a function of intrinsic parameters in saturation region and its detail is listed in the Appendix (3). The linear regression giving the extracted $R_s = 2.36\Omega$ for $V_{ds} = 1.1$V and $V_{gs} = 837.5$mV as shown in Fig. 3.

$$Real\left(Z_{in,12}\right)\_HF \approx R_s + A_s/\omega^2 \tag{10}$$

Using Y^i-parameters analysis of the intrinsic part as defined in Fig. 2, a parameter extraction procedure is developed and included in the Appendix (4)-(16). The directly extracted capacitances C_{ds}, C_{gd}, C_m and C_{gso} versus frequency are plotted in Fig. 4. The result that directly extracted capacitances from measurement are almost constant across broad frequency band confirms the validity of the complete model and extraction procedure in this work.

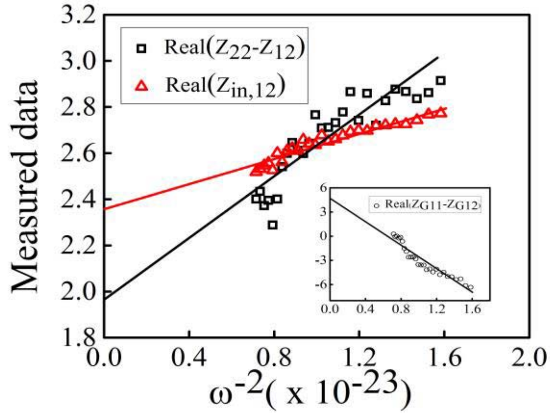

FIGURE 3. **Measured data and corresponding linear fitting lines in the high-frequency region (40G-60GHz) as a function of ω^{-2} gives the extracted values of $R_d = 1.98\Omega$, $R_s = 2.36\Omega$ and $R_g = 4.6\Omega$.**

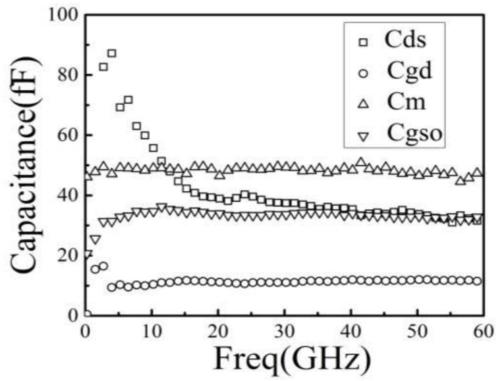

FIGURE 4. **Frequency dependence of directly extracted capacitance parameters for a HLMC 40nm NMOS having 5µm×32 width and biased to $V_{gs} = 837.5$mV and $V_{ds} = 1.1$V.**

Other intrinsic elements are formulated and extracted from simple linear fitting as defined in the Appendix.

The extracted intrinsic element values of the model in saturation region are listed in Table 1. The R_s decreases with increasing gate bias for constant $V_{ds} = 1.1$V, which is consistent with the description in [10] and [16]. The extracted key intrinsic parameters (e.g., C_{gs}, R_{nqs}, C_{gd}, C_{ds} and gm) are nearly constant in saturation region ($V_{gs} = 0.575$V-1.1 V) [6], [11].

V. EXPERIMENTAL VALIDATION

Using the presented parameter extraction method, we compare the simulation results of Y_{12} parameter with and without the gate-drain branch consisting of C_{gd1} and R_{gd} in Fig. 5. It shows that the presented model in this work with the gate-drain branch can yield a more accurate fit of the measured data in high frequency region than the conventional model. This phenomenon also exists in devices for $N_f = 8$ and $N_f = 16$. However, only a 32 finger NMOS transistor, which has a gate length of 0.04µm and a gate width of 5µm for each finger is shown as an example.

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TABLE 1. The extracted model parameters of HLMC N-MOSFET in saturation region (W5L0.04NF32, Vds=1.1V).

Parameters	V_{gs}=575mV	V_{gs}=837.5mV	V_{gs}=1.1V
Rs	3.1Ω	2.36Ω	2.1Ω
Cgs	38.5 fF	38.6 fF	38.3 fF
Rnqs	33Ω	32Ω	34Ω
Cgso	33.6 fF	34 fF	34.3 fF
Cgd	11.7 fF	11.6 fF	13.4 fF
Rgd	6.3Ω	6Ω	6.7Ω
Cgd1	16.8 fF	17.3 fF	17.4 fF
Cds	33 fF	35 fF	34.7 fF
Cm	51 fF	50 fF	53 fF
gm0	449mS	455mS	467mS
τ	0.71ps	0.65ps	0.34ps
rds	10.4Ω	10Ω	9.5Ω

In Fig. 5, real and imaginary parts of the simulated Y parameters using the extracted small-signal equivalent circuit model in this paper are found to agree well with the measured ones for frequency range from 0.25GHz to 60 GHz, thus verifying the effectiveness and accuracy of the complete small-signal model and its extraction method proposed in this work.

VI. CONCLUSION

A complete MOSFET small-signal model and the parameter extraction procedure are proposed. The values of the substrate parameters and the gate/drain series resistances are extracted by using their Y/Z-parameter equations derived from the model in zero-bias. For the coldfet model, we add a gate-substrate coupling capacitance to the equivalent circuit and a step-to-step extraction and de-embedding procedure for extrinsic elements is presented. In saturation region, a complete MOSFET small-signal equivalent circuit model addressing nearly all the parasitic and NQS effects is proposed. After removing the extrinsic parasitics, the intrinsic elements are formulated and extracted from the measurements and linear fitting. Moreover, we show that the frequency dependence of Y_{12} in high frequency region can be well explained by considering the gate-drain branch consisting of C_{gd1} and R_{gd}. The effectiveness and the accuracy of the complete model and its extraction technique is verified by achieving excellent agreement of the modeled Y parameters with the measured data from 0.25GHz to 60 GHz.

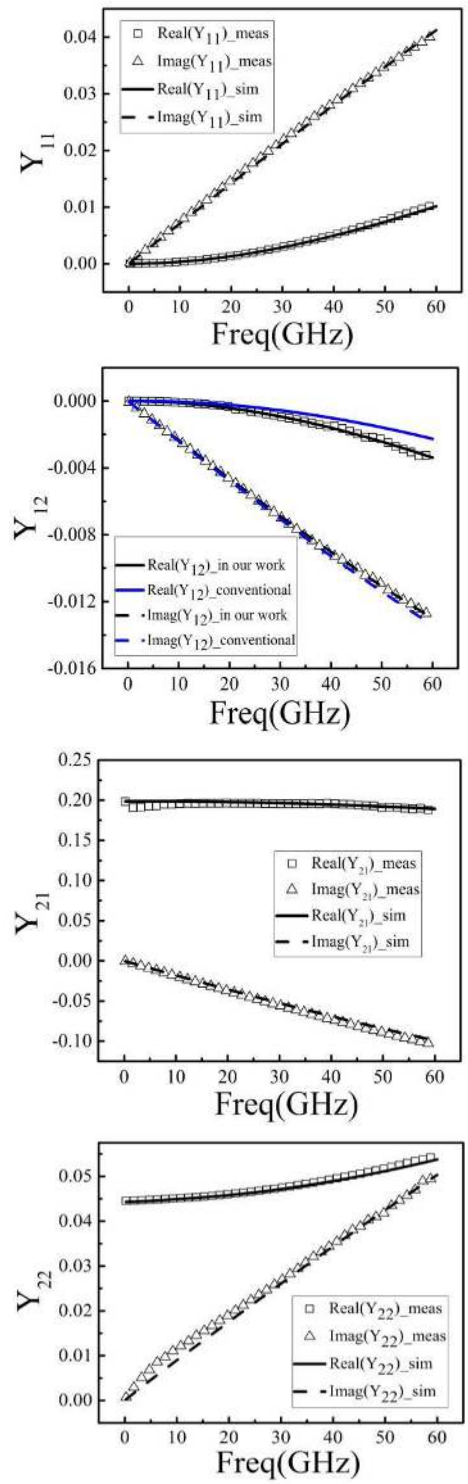

FIGURE 5. Real and imaginary parts of the Y-parameters versus frequency for the 40nm NMOS device for V_{ds} = 1.1V and V_{gs} = 837.5mV. W=5μm, N_f = 32. Symbols are the measured data, and curves are the modeling results.

APPENDIX

$$A_d = \frac{AC_{ds} + C_{gb}{C_{ds}}^2}{R_s C_{gb} A^2} \tag{1}$$

$$A_g = -\frac{C_{ds}}{R_s C_{gb} A} \tag{2}$$

With

$$\mathrm{A} = C_{gd}C_{ds} + C_{gs}C_{gd} + C_{gs}C_{ds}$$

$$A_s = \frac{1}{a \cdot R_{gd}} + \frac{b \cdot C_{gd}}{a^2} \tag{3}$$

With

$$\mathrm{a} = C_{gd}C_m - C_{ds}\left(C_{gd} + C_{gso}\right) - C_{gd}C_{gso}$$

$$\mathrm{b} = \left(C_{gd} + C_{gso}\right)g_{ds} + C_{ds}\left(\frac{1}{R_{gd}} + \frac{1}{R_{nqs}}\right) + C_{gd}\frac{1}{R_{nqs}} + C_{gso}\frac{1}{R_{gd}} + g_m C_{gd} - C_m\frac{1}{R_{gd}}$$

$$C_m = \frac{imag\left(Y^i{}_{12}\right) - imag\left(Y^i{}_{21}\right)}{\omega} \tag{4}$$

$$g_{m0} = \left|Y^i{}_{21} - Y^i{}_{12}\right| \tag{5}$$

$$\tau = -(1/\omega)phase\left(Y^i{}_{21} - Y^i{}_{12}\right) \tag{6}$$

$$r_{ds} = 1/real\left(Y^i{}_{12} + Y^i{}_{22}\right) \tag{7}$$

$$C_{ds} = \frac{imag\left(Y^i{}_{12} + Y^i{}_{22}\right)}{\omega} \tag{8}$$

$$\frac{\omega^2}{real\left(-Y^i{}_{12}\right)} = R_{gd}\cdot\omega^2 + \frac{1}{C_{gd1}{}^2\cdot R_{gd}} = \alpha_1\cdot\omega^2 + \beta_1 \tag{9}$$

$$R_{gd} = \alpha_1 \tag{10}$$

$$C_{gd1} = \frac{1}{\sqrt{\alpha_1\cdot\beta_1}} \tag{11}$$

$$C_{gd} = \frac{imag\left(-Y^i{}_{12}\right)}{\omega} - \frac{1}{\sqrt{\alpha_1\cdot\beta_1}\left(1+\omega^2\frac{\alpha_1}{\beta_1}\right)} \tag{12}$$

$$\frac{\omega^2}{real\left(Y^i{}_{11} + Y^i{}_{12}\right)} = R_{nqs}\cdot\omega^2 + \frac{1}{C_{gs}{}^2\cdot R_{nqs}} = \alpha_2\cdot\omega^2 + \beta_2 \tag{13}$$

$$R_{nqs} = \alpha_2 \tag{14}$$

$$C_{gs} = \frac{1}{\sqrt{\alpha_2\cdot\beta_2}} \tag{15}$$

$$C_{gso} = \frac{imag\left(Y^i{}_{11} + Y^i{}_{12}\right)}{\omega} - \frac{1}{\sqrt{\alpha_2\cdot\beta_2}\left(1+\omega^2\frac{\alpha_2}{\beta_2}\right)}. \tag{16}$$

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YANG CAO received the B.S. degree in electrical engineering from the Tianjin University of Technology and Education, Tianjin, China, in 2010, and the M.S. degree in microelectronics and solid state electronics from the Tianjin University of Technology, Tianjin, in 2015. She is currently pursuing the Ph.D. degree with the School of Microelectronics, Tianjin University. She is exploring device characterization, modeling, parameters extraction, and IC design based on RF CMOS technology.

WEI ZHANG received the B.S., M.S., and Ph.D. degrees in electrical engineering from Tianjin University, Tianjin, China, in 1997, 2000, and 2002, respectively. Since then, he has been with Tianjin University, where he is currently a Professor with the School of Electronic and Information Engineering. His research interests include very large scale integration implementations for signal processing systems and RFIC design.

JUN FU received the B.E. degree in semiconductor physics and devices and the M.E. and Engineering Ph.D. degrees in semiconductor devices and microelectronics from Tsinghua University, Beijing, China, in 1992 and 1998, respectively. From 1999 to 2001, he was a Post-Doctoral Research Fellow with the Laboratory of Electronic Components, Technology and Materials, Delft Institute of Microelectronics and Submicron Technology, Delft University of Technology, Delft, The Netherlands. From 2001 to 2006, he was with X-FAB Semiconductor Foundries AG, Erfurt, Germany, as a Process Development Project Manager. Since 2006, he has been an Associate Professor with the Institute of Microelectronics, Tsinghua University. His current research interests include device characterization, modeling, and IC design based on SiGe HBT, SiGe BiCMOS, RF CMOS, and RF LDMOS technologies.

QUAN WANG received the B.S. and M.S. degrees in material physics and chemistry from Nanjing University, Nanjing, China, in 1998 and 2001, respectively. He is currently with Shanghai IC Research and Development Center for RF device developing and manufacturing. From 2003 to 2004, he joined the co-project with HUAHONG and IMEC developing the 0.13 um logic technology. His current main research interest concerns advanced logic devices and its RF/mmW applications.

LINLIN LIU received the B.S. and M.S. degrees in microelectronics and solid-state electronics from Xi'an Jiaotong University, Xi'an, China, in 2009 and 2012, respectively. In 2012, he joined Shanghai IC Research and Development Center, where he is a Senior Modeling Engineer with the main focus on SPICE model developing for CMOS devices. His research interests include millimeter wave devices modeling and circuit design.

AO GUO received the B.S. degree from Nanjing University in 2002 and the Ph.D. degree in microelectronics and solid-state electronics from Peking University in 2007. He is currently a Senior Device Modeling Engineer with Shanghai IC Research and Development Center, with the main focus on SPICE model developing for CMOS logic devices and RF devices. His current research interests are more about novel modeling technology for advanced CMOS devices, and its applications in RF/mmWave designs.