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A Comprehensive Investigation on the Short Circuit Performance of MW-level IGBT Power Modules

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Keywords

«Insulated-Gate Bipolar Transistor (IGBT)», «Power Modules», «Short Circuit», «Current Distribution».

Abstract

This paper investigates the short circuit performance of commercial 1.7 kV / 1 kA IGBT power modules by means of a 6 kA Non-Destructive-Tester. A mismatched current distribution among the parallel chips has been observed, which can reduce the short circuit capability of the IGBT power module under short circuit conditions. Further Spice simulations reveal that the stray parameters inside the module play an important role in contributing to such a phenomenon.

1. Introduction

Nowadays, there are increasingly demands to improve the durability and reliability of modern power electronic systems while reducing the manufacturing and maintenance costs. In order to fulfill these requirements, it becomes more and more important to improve the performance of power semiconductor modules in terms of reduced failure under abnormal conditions [1]. According to the questionnaires surveyed in [2-3], 34% of the manufacturers consider power semiconductor discrete devices or modules as the most fragile components in power electronic systems. Insulated Gate Bipolar Transistors (IGBTs) are the most widely used reliability-critical power devices in industrial power electronic systems in the range above 1 kV and tens of kW, for instance wind turbine systems [4-5]. In medium- and high-power applications with IGBTs, the power module is the most used semiconductor packaging, which usually contains multiple chips connected in parallel to increase its current ratings [6]. IGBT modules usually come with a specified short circuit operation capability of a few μs (e.g., typically 10 μs). However, this allowable short circuit operation duration might be reduced if imbalanced current distribution exists among the multiple chips in IGBT modules. The aim of this paper is to comprehensively investigate the current distribution of IGBT chips of MW-level power modules during short circuit operation.

Because of the variations in chip characteristics and the layout design of each section in the power modules [6], it is difficult to ensure that the currents among the paralleled IGBT chips are identical. This challenge becomes even more critical for the MW-scale IGBT modules, due to the high current ratings (typically kA-level) and the asymmetric geometry. Several researchers have investigated the current sharing under normal operations: in [7-8], the Partial Element Equivalent Circuit (PEEC) method has been applied to analyze the current imbalance of IGBT modules with 2 or 4 chips connected in parallel, while convincing experimental validations are still missing; in [9], the field analysis has been applied to investigate the current imbalance among 6 chips based on the detailed structure. A study on medium power modules (e.g., with a rating of 600 V/300 A) shows that the stray parameters can affect the power loss and temperature distribution among IGBT chips [10], which leads to mismatched lifetimes. This effect becomes even more critical for the short circuit operations, since the current is several times higher than the normal operation values. Some of the chips may withstand higher stresses during short circuits, and therefore fail faster than others in the same power module.

This paper investigates the current imbalance among parallel chips during turn-on short circuit of MW-level IGBT power modules by means of a 6 kA Non-Destructive-Tester (NDT). Based on the experiments on the 1.7 kV / 1 kA IGBT power modules, the most stressed IGBT chips are identified according to the power loss distribution. Moreover, the impact of stray resistances and stray inductances of the IGBT module layouts is studied by Q3D and Spice simulations. This presented findings could be helpful for both the packaging designers and application engineers to optimize the internal layout design, to improve the thermal performance, and finally to enhance the reliability level of IGBT power modules.

2. Specifications of the Device under Test

The experimental study has been carried on a commercial 1.7 kV/1 kA IGBT module. This MW-level module is widely used in wind turbine systems, motor drives and other high power converters. The maximum operating junction temperature is 150 °C. The rated short circuit current is 4 kA for a gate pulse duration no longer than 10 μ s under a maximum DC voltage of 1 kV and an external circuit stray inductance of 30 nH. The main specifications are summarized in Table I.

An outline picture of the Device under Test (DUT) is shown in Fig. 1(a). The package size of the module is 234 mm by 89 mm by 38 mm. There are two power terminals for the DC+ connections (upper IGBT collector), two power terminals for the DC- connection (lower IGBT emitter), and one terminal with two screw connections for the output phase. The upper IGBT gate terminals are on the right side in Fig. 1(a), and the lower IGBT gate terminals are on the left side, which are also aligned with the Negative Temperature Coefficient (NTC) thermistor connections. There are six sections connected in parallel to achieve the rated current of 1 kA. For the sake of clarification, the definition of section numbers is shown in Fig. 1(b): the nearest section to the gate terminals is defined as section 1 and the farthest one is defined as section 6. Each section contains two IGBT chips and two freewheeling diode chips, which are configured as a phase leg.

Table I: The main specifications of the DUT.

Specifications	Values
Collector-emitter voltage, V_{CES}	1.7 kV
Continuous DC collector current, $I_{C,nom}$	1 kA
Maximum operation temperature, $T_{vj,op}$	150 °C
Rated short circuit current, I_{SC}	4 kA
Gate-emitter maximum voltage, V_{GEs}	+/- 20V
Number of parallel sections	6

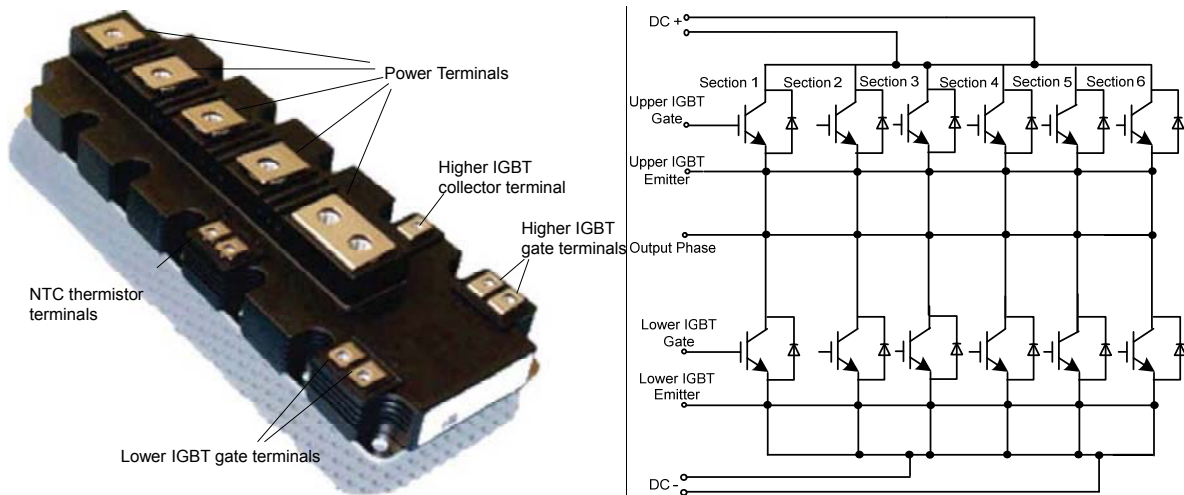


Fig. 1: The IGBT power module under test: (a) the photo of the packaging outline, (b) internal structure of the power module with section definitions.

3. Short Circuit Tests

3.1 Description of the testing setup

During a short circuit, the IGBT module is working in the gate voltage controlled active region, withstanding both high voltage and high current. The corresponding huge power shock (in the range of megawatts) can damage the power module in short transients (i.e., μs -level), and even cause explosions. In order to prevent the potential damages, a state-of-the-art Non-Destructive Tester (NDT) is built up with the current and voltage limits of 6 kA and 1.1 kV, respectively. It can perform repetitive overcurrent and short circuit tests of IGBTs under protected conditions.

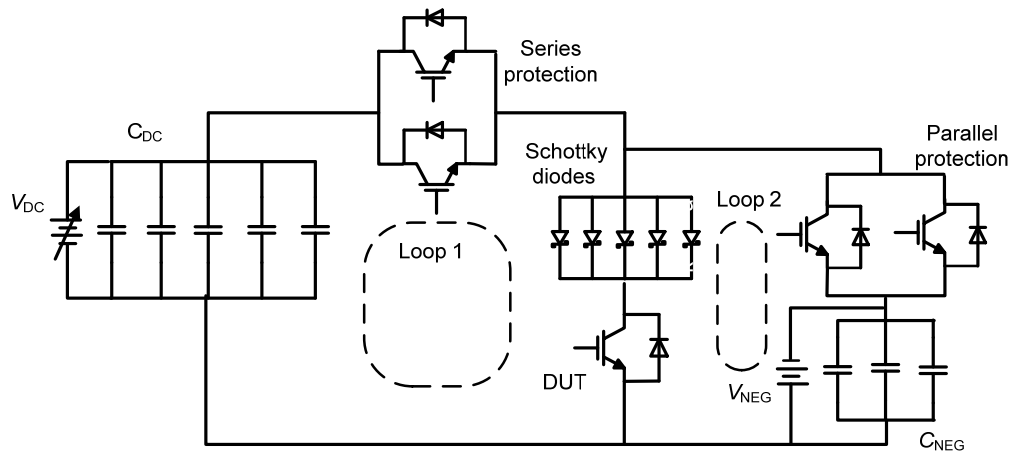


Fig. 2: Circuit schematic of the non-destructive tester.

The basic principle of the non-destructive testing technique is to perform repetitive tests up to the physical limits of the DUT while avoiding device destructions. This characteristic is achieved by some additional protection switches, typically set in series to the DUT. These protection switches are usually IGBT power modules that have higher voltage and current ratings. Fig. 2 shows the principle schematic of the constructed NDT. The NDT structure is described as follows. A high-voltage power supply charges up preliminarily a capacitor bank C_{DC} to a given testing voltage. This capacitor bank supplies all the energy required for the test. A series protection is connected between the capacitor bank and the DUT. It is turned on before the short circuit is activated and switched off right after the short circuit test in order to prevent the DUT from potential explosions. The additional leg in parallel to the DUT contains the parallel protection, a capacitor bank C_{NEG} , and a battery V_{NEG} . The parallel protection has two functions: 1) to assist the series protection during its turn off by diverting the tail current of IGBTs; 2) to act as a crow-bar in case of any instability occurs. The capacitor bank C_{NEG}

and the battery V_{NEG} are used to accelerate the transients. Five Schottky diodes are used to avoid any negative voltage that might be supplied to the DUT. A FPGA supervising unit provides the time control signals for the DUT and protection driving signals with a resolution of 10 ns.

The series protection switch is implemented by 3.3 kV/ 3 kA IGBT modules with a larger physical size compared to that of the DUT, which introduce a considerable stray inductance into the circuit. Two countermeasures are adopted to minimize the overall circuit inductance. First of all, two devices are connected in parallel with optimized placement locations by means of a three-dimensional Computer-Aid Design (CAD) tool. Secondly, the mutual coupling effects are taken into account for the bus bar design. With these considerations, the overall circuit inductance of the Loop 1 shown in Fig. 2 is 37 nH. More details about the NDT can be found in [11].

The short circuit operations can be classified as Type I and Type II [12]: Type I happens at the turn-on of the IGBT. Before turn-on, the gate voltage is negative and the collector-emitter voltage (V_{CE}) is at high level. Immediately after turn-on into short circuit, the collector current increases to several times of the rated current, which is the value of the saturated current at V_{GE} . The IGBT withstands both high voltage and high current, and it should be turned-off within a short duration (i.e., typically less than 10 μ s). Type II happens during the IGBT conducting mode. The main difference with Type I is the addition of a transient desaturation phase, which may increase the V_{GE} due to the Miller capacitance and therefore result in a higher short circuit current peak. After the desaturation phase, short circuit current drops to its static value I_{SC} , and the subsequent behavior is the same as Type I. It should be mentioned that Type II short circuit is harsher in converter operations due to the potential oscillations and collector overvoltage. Because Type I short circuit can reflect the semiconductor's performance more directly, this study focuses on the Type I short circuit.

3.2 Experimental results

First of all, a new 1.7 kV/1 kA IGBT module is tested under a 700 V DC voltage for a 10 μ s short circuit operation at a room temperature of 25°C. Fig. 3 shows the waveforms of the lower IGBTs collector current I_C , the gate-emitter voltage V_{GE} , and the collector-emitter voltage V_{CE} . It is noted that the peak short circuit current reaches 4.2 kA. The collector voltage drop during short circuit turn-on and voltage peak during short circuit turn-off are related to the effect of the stray inductance and the high current slopes di/dt .

It is worth mentioning that the collector current I_C presents an overshoot and then it decreases with time. This phenomenon is caused by the junction temperature rising during the short circuit [6]. This dynamic electro-thermal coupling phenomenon is well known and has also been simulated for this class of devices by means of a physics-based PSpice-Icepak co-simulation method recently presented in [13].

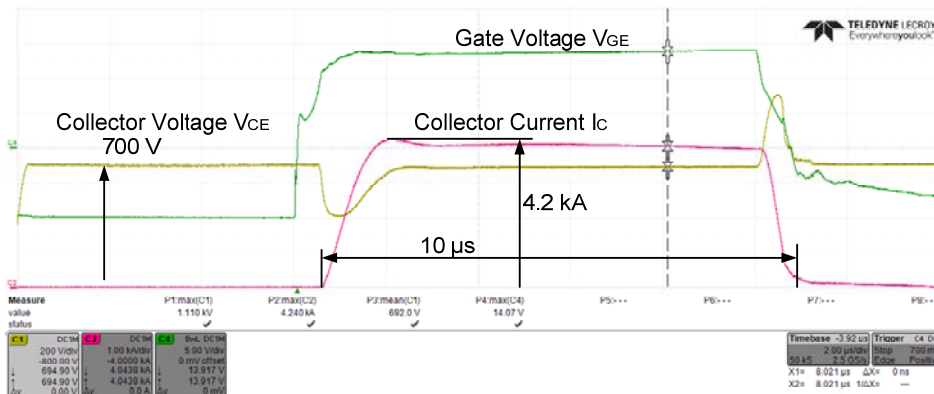


Fig. 3. Experimental waveforms during a 700 V/10 μ s short circuit: time 2 μ s/div, collector voltage 200 V/div, collector current 1 kA/div, gate voltage 5 V/div.

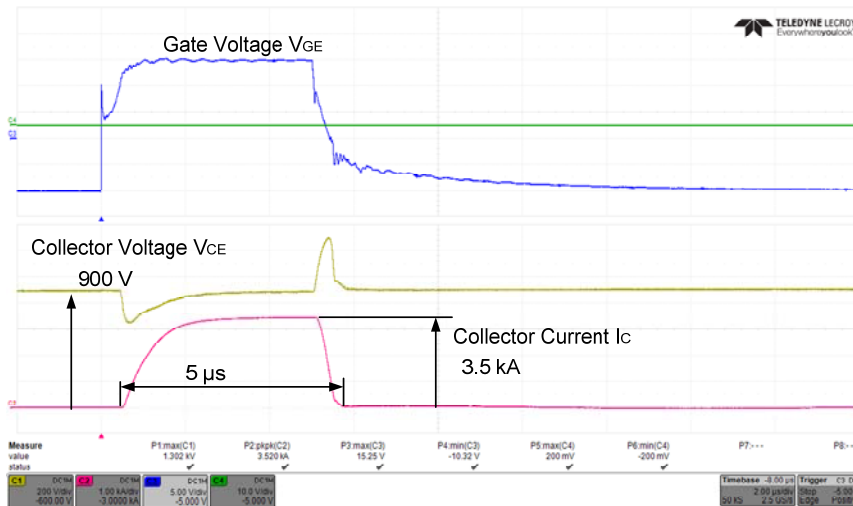


Fig. 4. Experimental waveforms during a 900 V / 5 μ s short circuit: time 2 μ s/div, collector voltage 200 V/div, collector current 1 kA/div, gate voltage 5 V/div.

Another power module in which the plastic frame and silicone gel have been removed is tested at 900 V DC for a 5 μ s short circuit operation. The experimental waveforms of I_C , V_{GE} , and V_{CE} during the short circuit test are shown in Fig. 4. It is worth mentioning that the waveforms refer to the upper IGBTs of the leg. It can be seen that I_C is not obviously decreasing within the 5 μ s, which cannot be simply explained by the shorter testing duration. Therefore, further tests on internal current distributions are desirable to study the root-cause mechanism.

The cross-section information of the IGBT module is illustrated in Fig. 5: each IGBT section is connected to the power terminals through copper bus bars. Rogowski coils have been inserted into the bus bars to measure the collector current of each section as shown in Fig. 5. An ultra mini CWT Rogowski probe with a current range up to several kA and a parasitic inductance in the range of a few pH is used for the current measurements [14].

In Fig. 6, the measured short circuit current distribution among the six sections is plotted for the same test of Fig. 4. A mismatched current distribution among the six sections can be observed. It is worth noting that Section 5 and Section 6 have lower di/dt during the turn-on transient and the current through them increase with time. On the other hand, Section 2 and Section 3 show an obvious overshoot and their currents decrease with time (same behavior as the I_C in Fig. 3). What above proves that, even though the total current is almost constant during the test, a strong transient imbalance occurs. The above observations imply that the parallel sections may have different stray parameters at the short circuit frequency, which are further studied by detailed simulations in the following section.

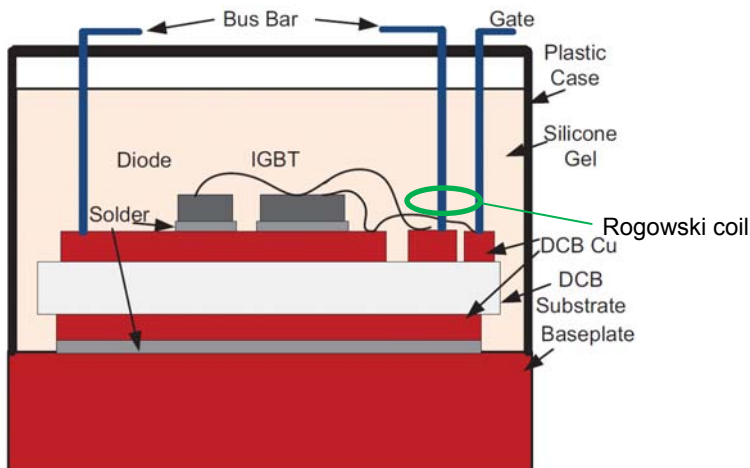


Fig. 5. The cross-section structure of the power module and the Rogowski coil measurement location.

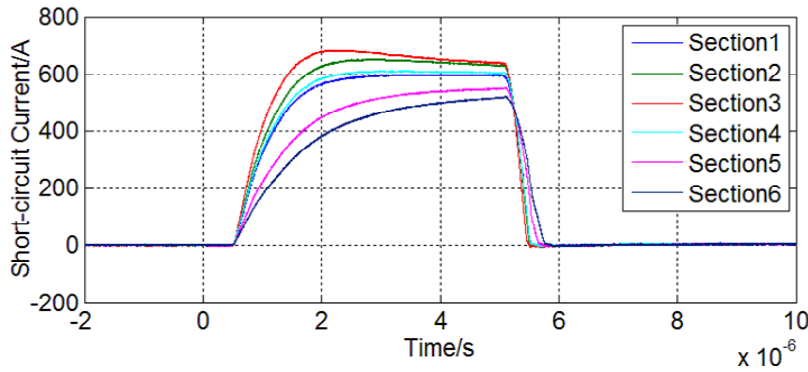


Fig. 6. The experimental waveforms of the collector currents of the six sections under the same condition of the test in Fig. 4.

4. Simulations

PSpice simulations have been performed in this study to further investigate the above observed phenomenon. The procedure is as follows: firstly, the parameters in the PSpice IGBT model are calibrated with the provided information in the DUT datasheet; secondly, an electro-magnetic simulation is performed to extract the stray parameters inside the DUT; thirdly, a circuit profile is defined, which is identical to the executed experiment. The procedure is illustrated in Fig. 7.

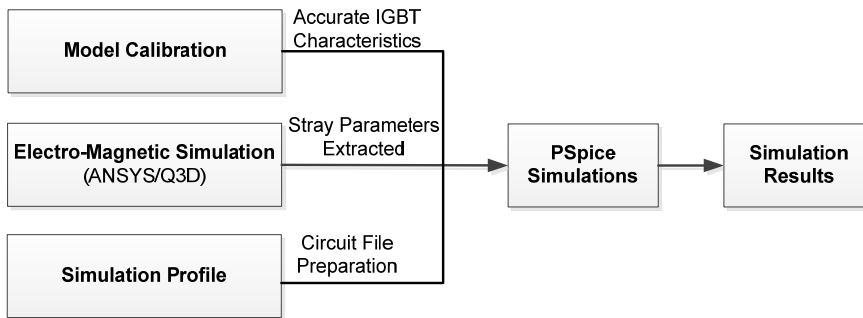


Fig. 7. A schematic of the simulation procedure.

4.1 Model calibration

A physics-based lumped-charge IGBT Spice model [15] is used, which has been proved to have a higher accuracy for high voltage IGBTs with respect to the embedded PSpice IGBT model. Based on the datasheet information, the IGBT model has been calibrated at different conditions. The IGBT model output characteristics at different V_{GE} (i.e., 8 V, 10 V, and 15V) are plotted in Fig. 8, which are also compared with the curves in the datasheet of the DUT.

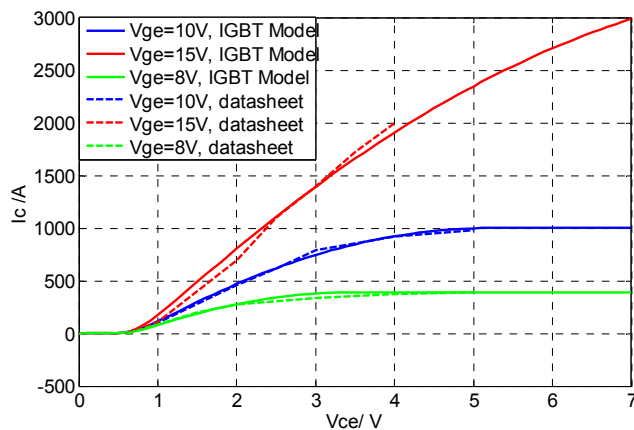


Fig. 8. The output characteristics based on the obtained PSpice IGBT model and the datasheet.

4.2 Electro-magnetic simulation

A detailed discussion on the stray parameters extraction of the DUT has been presented in a recent study [15]. A brief introduction is given as follows. First, a detailed geometry is created in a CAD program and further imported to the software ANSYS/Q3D. Then, Q3D applies Finite-Element Method (FEM) to extract the matrices of resistance, inductance, and capacitance. Simulations are performed in Q3D at a specific frequency. The corresponding stray inductances and stray resistances of the six sections (from the power terminals to each section) are extracted. The simulations are done in such a way that, when extracting the inductance and resistance of a certain section, only the IGBT chip of this section conducts. It is worth noting that simulations should be performed at each specific frequency individually instead of by using the “frequency sweep” available in Q3D. It is because that the finite element mesh for the adaptive solution is optimized for the simulated frequency only, and the accuracy of the results could vary significantly at frequencies different from the specified frequency. The simulated stray inductances and stray resistances of different sections at 100 kHz (i.e., corresponding to a 10 μ s transient) are listed in Table II. The results show that the middle sections (Sections 2-4) have lower stray inductances and stray resistances than the other sections.

Table II: The stray parameters of each section at 100 kHz.

	Section 1	Section 2	Section 3	Section 4	Section 5	Section 6
Stray resistance ($\mu\Omega$)	1449	850	469	665	931	1559
Stray inductance (nH)	70	43	33	44	62	82

4.3 Simulation results

With the calibrated IGBT model and the extracted stray parameters, PSpice simulations are performed under the same conditions as the experiments: a DC voltage of 900 V DC, a short circuit duration of 5 μ s, and at the room temperature of 25°C. The PSpice simulation circuit is plotted in Fig. 9. L_{circuit} represents the circuit stray inductance, while R_{x_m} , L_{x_m} ($m = 1, 2, \dots, 6$) represent the stray parameters of the six sections. The simulation results of the I_C and V_{CE} are plotted as dashed lines in Fig.10 (a), which are compared with the experimental waveforms of Fig. 4 (shown in solid lines). The simulation results of the short circuit currents in each section is shown in Fig. 10(b) in dashed lines, compared with the corresponding experimental results in solid lines.

In Fig. 10(a), the PSpice simulated waveforms coincide with the experimental ones: I_C behaves similar rising slopes, and V_{CE} have same voltage undershoot/overshoot transients during short circuits. It is noted that the simulated short circuit current is slightly higher than the experimental one in Fig. 10(a). This is because the PSpice simulations are performed at a constant temperature of 25°C. While in the experiments, the IGBT chip temperature increases to a much higher temperature during the short circuit operation. The short circuit current is reduced with the increase of the chip temperature. It suggests that further simulations dealing with the IGBT dynamic electro-thermal coupling effects at μ s-level is demanded to achieve a more accurate prediction of the short circuit performance.

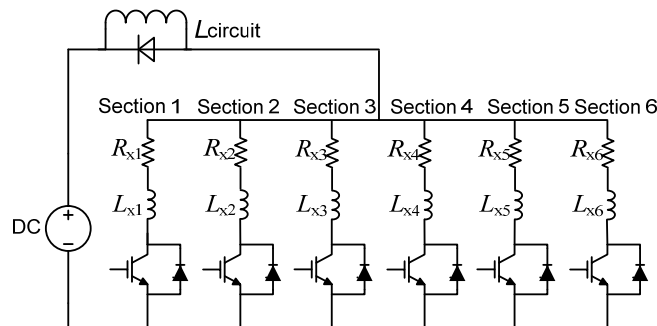


Fig. 9. The PSpice circuit for simulating the current distributions during short circuits.

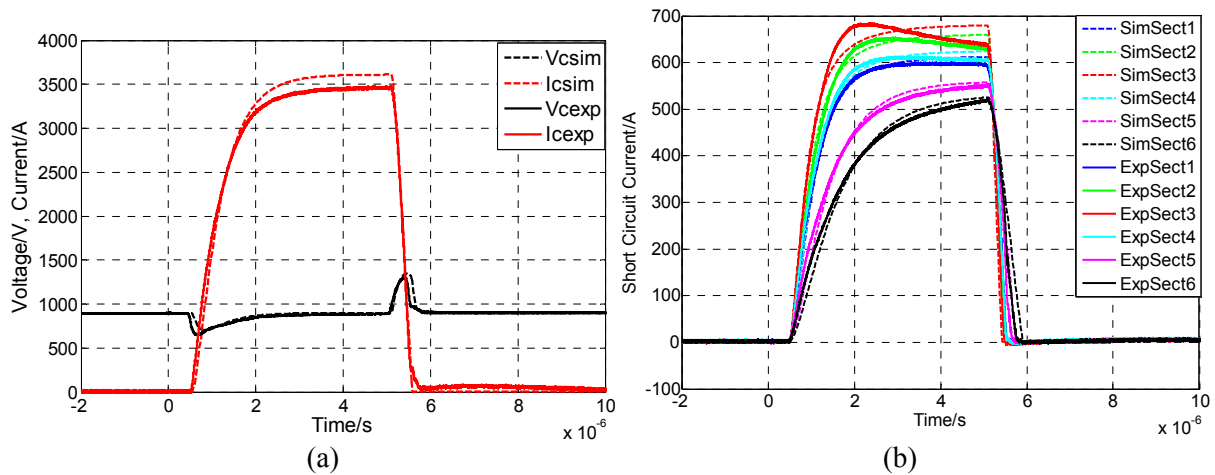


Fig. 10. The PSpice simulation results: (a) the whole module short circuit waveforms, comparing with experimental waveforms in Fig. 4; (b) simulated section currents, comparing with waveforms in Fig.6.

In Fig. 10(b), the PSpice simulated di/dt coincides with the experiments. This comparison confirms the differences in stray parameters among the parallel sections. The middle sections (Sections 2 and 3) have higher di/dt and carry higher currents, while the farthest sections (Sections 5 and 6) have lower di/dt and conduct lower current. Meanwhile, due to the aforementioned dynamic electro-thermal coupling effects, the currents of Sections 2 and 3 visibly show overshoots and decrease with the operation time. Because of the higher inductances, the Sections 5 and 6 currents increase during the entire operation time. It is worth noting, though, that the current differences tend to reduce at the end of the short circuit, evidencing a dominating effect of the inductance in the imbalance phenomenon. From Fig. 6 and 10(b), it is observed that Sections 2 and 3 have higher current stresses which may fail faster than other sections.

In order to study the impact of the stray parameters on the internal current distribution, a further PSpice simulation is performed with a set of assumed stray parameters with reduced differences among the six sections. The stray parameters of Sections 5 and 6 are within 1.5 times the values of Sections 2 and 3. The simulation is done under the same conditions as simulation presented above. The simulated short circuit current waveforms are plotted in Fig. 11. The current imbalance is within 50 A (i.e., less than 10%) among the six sections. This suggests the current imbalance phenomenon can be minimized by decreasing the stray parameters imbalance.

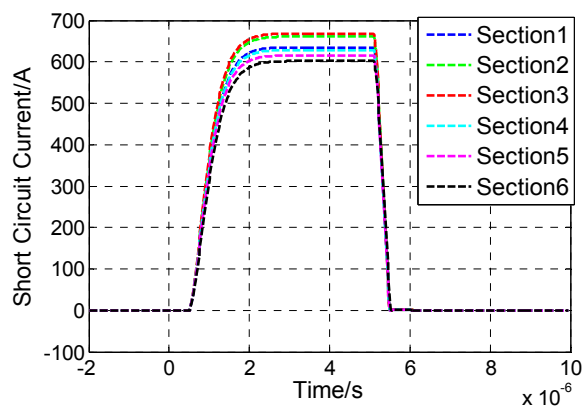


Fig. 11. The simulation results of the short circuit section currents under a set of assumed stray parameters with reduced differences among different sections.

5. Conclusion

This paper investigates the short circuit performance of the MW-level IGBT power module by means of experiments and simulations. It has been shown that the stray parameters imbalance lead eventually to a non-equal current distribution among the parallel chips. Both simulations and experiments show that some chips are more stressed than others during short circuits, as well as suggest a dominating effect of the inductance in the imbalance phenomenon. The proposed study can provide a feedback to module designers on optimizing module's internal structure and geometry, as well as give suggestions for application engineers to improve the thermal management and/or cooling system design.

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