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A Comprehensive Review on Space Vector Modulation Techniques for Neutral Point Clamped Multi-Level Inverters

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ABSTRACT The Neutral Point Clamped (NPC) Multi-Level Inverters (MLI) have been ruling the power electronics industries for the past two decades. The Multi-Carrier Pulse Width Modulation (MCPWM) is common PWM techniques which are widely used in NPC-MLI applications. However, MCPWM is not having a good impact on the balancing of DC-link voltages, Common Mode Voltage (CMV) and limiting the Total Harmonics Distortion (THD). The Selective Harmonic Elimination (SHE) technique is introduced for reducing the THD, however all the switching angles should be maintained less than $\pi/2$ to keep the eliminated harmonics at constant level which narrows down the modulation index range. Hence, in recent days Space Vector Modulation (SVM) technique is widely used in NPC-MLI, which gives better DC-link voltage balancing, self-neutral point balancing, near-zero CMV reduction, better-quality harmonics profile and switching loss minimization. Hence, it is a preferred solution for the majority of electrical conversion applications such as electric traction, high power industrial drives, renewable power generation, and grid-connected inverters, etc. The paper gives a comprehensive review of the SVM for NPC-MLI. First, this paper deliberates the state of art for two-level SVM and extends it to three-level (3L) SVM. Also compares the 3L SVM performance with other MCPWM techniques. Followed by the various modified MLI SVM techniques in terms of their implementations, DC-link capacitor balancing, and reduction of CMV. Further, the review of MLI SVM is widened to open-end winding Inverters and multiphase MLIs. The final part of this paper discussed the future trends and research directions on MLI SVM techniques and its applications.

INDEX TERMS Space Vector Modulation, Multi carrier Pulse Width Modulation, 3-Phase Neutral Point Clamped Inverters, 5-Phase Neutral Point Clamped Inverters, DC-link voltage balancing, Total Harmonics Distortion, Common Mode Voltage, Open-End Winding Inverter.

ABBREVIATION

MLI	Multi-Level Inverter
VSI	Voltage Source Inverter
THD	Total Harmonic Distortion
PWM	Pulse Width Modulation
MCPWM	Multi carrier Pulse Width Modulation
NPC	Neutral Point Clamped
CMV	Common Mode Voltage
CHB	Cascaded H-Bridge
FC	Flying Capacitor
SHE PWM	Selective Harmonic Elimination PWM
SVM	Space Vector Modulation
SVD	Space Vector Diagram
PD PWM	Phase Disposition PWM
POD PWM	Phase Opposition and Disposition PWM
APOD PWM	Alternate POD PWM
PSC PWM	Phase Shifting Carrier PWM
IC PWM	Interleaved Carrier PWM
VFC PWM	Variable Frequency Carrier PWM
VSVM	Virtual Space Vector Modulation
NTV	Nearest Three Vector
STV	Selected Three Vector
OFV	Optimized Five Vectors
2L	2 Level
3L	3 Level
NPF	Neutral Point Fluctuation
DC	Direct Current
3D	3 Dimensional
OVM	Over Modulation
M^2ZV	One Zero Vector and Two Medium Switching Vectors
M^3V	Three Medium Switching Vectors

FPGA	Field Programmable Gate Array
PE	Partial Elimination
FE	Full Elimination
EMI	Electromagnetic Interference
OFV	Optimized Five Vectors
OEW	Open-End Winding
FLI	Five leg Inverter
NSI	Nine Switch Inverter
FOC	Field Oriented Control
DTC	Direct Torque Control

I. INTRODUCTION

The two-level (2L) VSI has been ruling the industrial world before the development of MLI. The 2L VSI is widely used in transportation and industrial automation [1], [2]. The output voltage of the 2L VSI will be of two levels such as $+V_{dc}$ and $-V_{dc}$. The PWM generation plays an important role in controlling the connected load. The generation of PWM for two-level (2L) VSI is discussed. The limitation of using 2L inverter is that it is not possible to operate high power and high frequency applications. To overcome this issue the three-level (3L) inverter is developed in 1981 by A.Nabae, et.al., The output voltage of the 3L inverter will be in three level like $+V_{dc}/2$, 0 and $-V_{dc}/2$. Since the development of 3L inverter, the controlling of motor drive in high voltage applications is preferred using MLIs [3]-[6].

The MLIs are most commonly categorized into NPC inverter [7]-[10], cascaded H-bridge inverter [11]-[14] and flying capacitor inverter [15]-[18]. Among these three types, NPC which is also called as diode clamped multi-level inverter attracts the industries as they have lower Electromagnetic Interference (EMI) and the efficiency is considerably high. The controlling of drives is done by PWM strategies which are basically classified as Multi-carrier PWM (MC PWM) [19]-[21], Selective Harmonic Elimination (SHE) PWM [22]-[24] and Space Vector Modulation (SVM) [25]-[28]. The PWM signal generated using multiple carrier signals by shifting the level and phase angle of carrier signals is named as Multi carrier PWM signals. The Phase Disposition (PO) [29], Phase Opposition and Disposition (POD) and Alternative Phase Opposition and Disposition (APOD) [30] techniques are grouped as level shifted PWM. In Phase Shifting Carrier (PSC) PWM [31], the power loss is evenly distributed when compared to level shifted PWM. The Interleaved Carrier (IC) PWM [32] and Variable Frequency Carrier (VFC) PWM [33] are also the types of MCPWM techniques. These MCPWM techniques are not able to reduce the harmonics in output which induces the researcher to move on to SHE PWM technique. The SHE PWM is used to eliminate the harmonics selectively [22]. The harmonics which are needed to be removed is included in the carrier signal which helps to eliminate the corresponding harmonic elements from PWM pulse. Though SHE PWM eliminates the harmonics, it has few drawbacks like slower reaction during transient conditions, switching angle needs to be maintained below $\pi/2$, pre-defined calculations are required etc., [216-219]. To overcome all these issues, the SVM technique [34] is introduced which also provides the balancing of DC-link voltages and reduction of common mode voltages along with harmonic reduction [35]-[38]. The output voltage and harmonic elimination of SVM is better over the sine PWM techniques [220-221]. The reduction of CMV can be done easily in SVM by neglecting the switching states that generates high CMV. As the pulses in SVM technique is digital, the DC-link utilization can be done easily in SVM.

Though SVM has few advantages, the medium vectors present in space vector are responsible for the fluctuation in DC-link voltages. This problem can be reduced by removing the medium vectors and it is named as Virtual Space Vector Modulation (VSVM) [39]-[41]. Due to the absence of medium vectors in VSVM, the fluctuation in the neutral point is tends to be reduced which provides the better output. Another challenge in the NPC MLI is faced when the unbalanced dc source (PV input) is used [42]-[44]. The location of vectors in SVM of unbalanced dc source will be displaced from its original position due to the variation of dc sources. The performance of multi-level inverter when unbalanced dc source is supplied to the inverter is discussed. The minimum time period is involved along with original time period to overcome the unbalancing issues caused by asymmetrical dc sources. The operation of the MLI at over modulation region is discussed and its performance is compared with the normal modulation region. [45]- [46].

Then the research is moved towards 3D SVM technique which provides the faster and accurate response than 2D SVM. The 3D SVM techniques for three-leg and four-leg inverter are studied [47]. The CMV and dc-link balancing is minimized because of non-availability of redundant vectors (vectors at same point is said as redundant vectors). The other advantages of 3D SVM is low switching loss and conduction loss. The research is very less in 3D SVM due to its complex structure and calculation. Though many PWM and SVM techniques are available for the 3-phase inverters to reduce the DC-link voltage, switching loss, CMV etc., The development of Open-End Winding (OEW) inverter gives the solution for the above-mentioned limitations. OEW inverter is introduced to overcome all these issues without any changes in the modulation techniques [48], [49]. The OEW inverter has two inverters with separate windings connected to a common load. No additional modification needed for this topology to reduce the CMV as the inverters are connected to separate DC voltages and switching loss is less because the supply voltage is half when compared to the conventional NPC MLI. The SVM of the 2L and 3L OEW inverter is discussed.

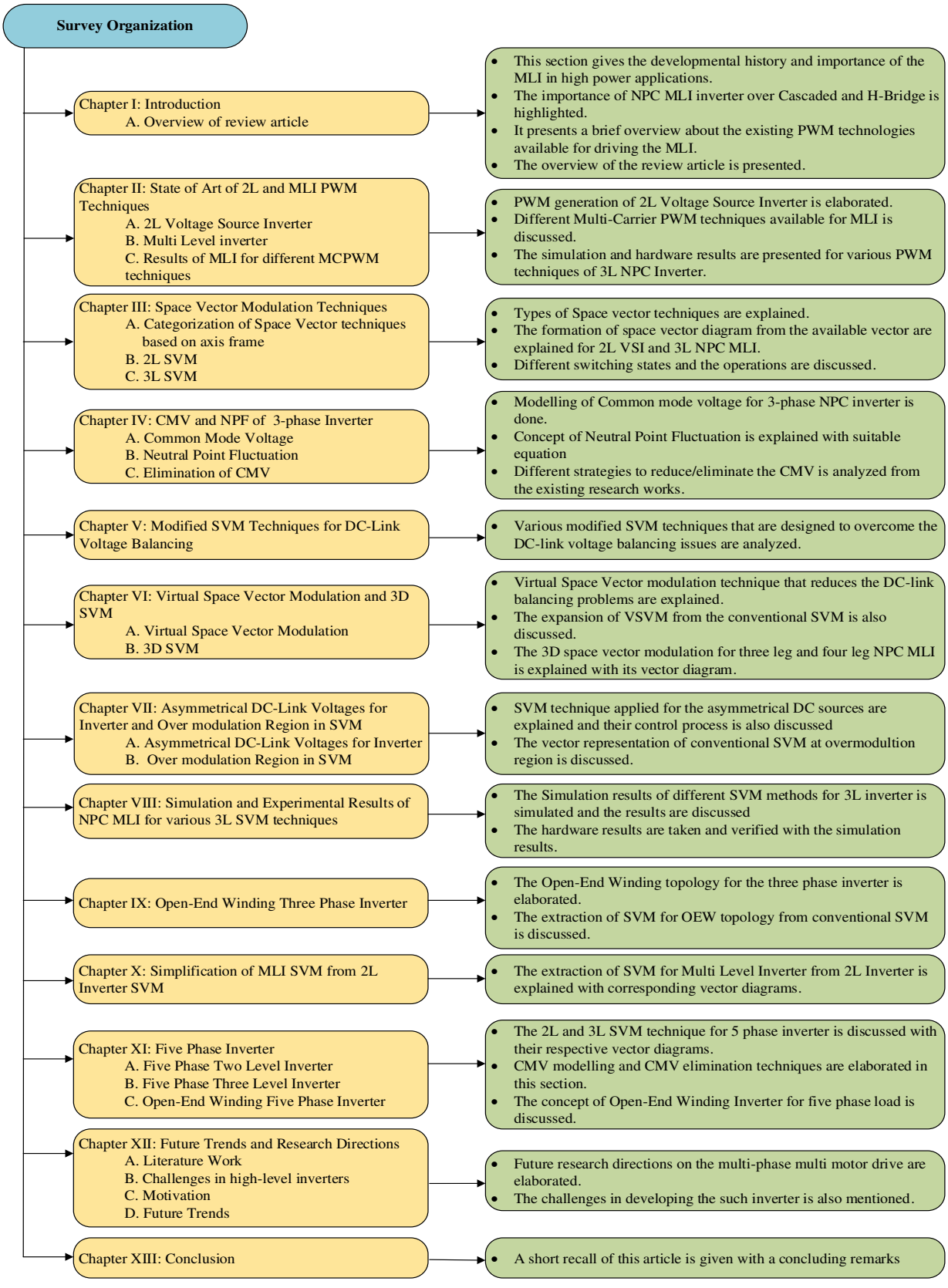

FIGURE 1. Organization of the review article

In recent years, the researchers are slowly concentrating on 5-phase inverters which decrease the switching loss and CMV when compared to the 3-phase inverters [50]. Also, it provides the optimum DC-link voltage for inverter. The multi-phase system reduces the per-phase power stress as power gets divided by five [51]. The MCPWM techniques of 5-phase inverter will be similar to 3- phase inverter [52]-[54]. The SVM for 5-phase 2L NPC inverter [55] is

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discussed followed by 3L SVM technique where Optimized Five Vector (OFV) method is used for the selection of vectors [56], [57]. The OFV is carefully chosen so that the desired voltage is generated at main subspace (α-β subspace) and the average voltage at auxiliary subspace (x-y subspace) is made zero.

The OFV consists of reduced switching vectors (113 vectors) of the 5-phase SVM which is further reduced to 51 vectors that has zero CMV which eliminates the CMV completely. The OEW topology for 5-phase inverter is also discussed. The review on different PWM techniques is made to realize that a SVM technique provides better performances than the MCPWM techniques.

A. Overview of review article:

The overview of the presented review article is illustrated in flowchart Fig. 1. This article is organized as described in the flowchart. The aim of this article is to find the suitable PWM generation technique for the NPC MLI which overcomes the issues of CMV, DC-Link balancing, etc. This review article discusses about the following for 3-phase and 5-phase loads.

- This paper gives the basic knowledge about different PWM techniques available for 2L VSI and NPC MLI.
- The mathematical analysis of CMV and NPF is carried out.
- Various modified SVM techniques to reduce CMV and DC-link capacitor voltage are discussed.
- OEW inverter topology are discussed.
- SVM techniques for asymmetrical DC source MLI, SVM at Over-modulation region, VSVM and 3D SVM techniques are also explained for 3-phase loads.

The section II in this paper discusses about the PWM techniques involved in 3-phase inverter. The Space Vector Modulation technique for 2L and 3L three-phase Inverter has been discussed in the section III. The CMV and NPF for 3-phase inverter has been explained in section IV. The modified SVM techniques are compared and discussed in section V. The section VI explains about Virtual Space Vector Modulation and 3D SVM techniques. The SVM techniques for asymmetrical DC-link voltages and SVM in over-modulation region has been explained in section VII. The simulation results are validated with experiments results of 3-phase NPC MLI for different 3L SVM techniques in section VIII. The OEW topology of 3-phase inverter is discussed in section IX. Simplification of MLI from 2L Inverters is discussed in section X. The section XI discussed about SVM of 5-phase 2L and 3L inverters along with OEW topology. The future trends and research directions are discussed in section XII. The inference obtained from this review article is summarized in section XIII as conclusion.

II. STATE OF ART OF 2L AND MLI PWM TECHNIQUES

The power electronics switches are controlled by switching on and off. This switching process is done by PWM techniques. The triangular carrier signal is compared with sinusoidal reference signal for generation of pulse which controls the switching process of power electronic switches and it is named as carrier based PWM techniques. The number of carrier signals used in PWM technique is based on the number of levels required. Number of carrier signals = N-1, where N is number of levels. The various PWM techniques for 2L and 3L inverter are discussed in this section.

B. 2 Level Inverter:

The circuit for 2L VSI is shown in Fig. 2. The inverter has 6 switches with 2 switches in each leg. The upper switch and lower switch in each leg are complementary to each other.

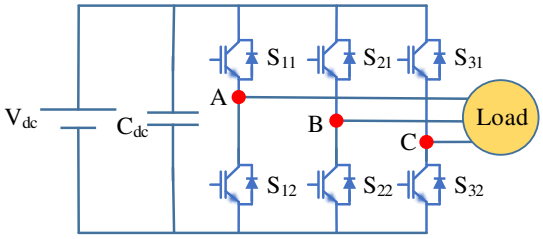
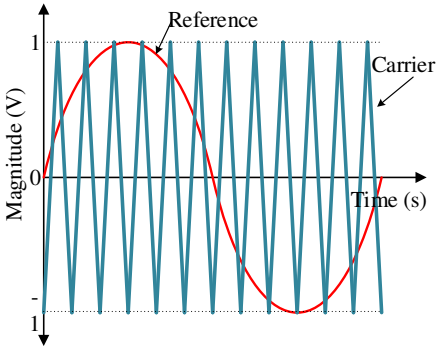


FIGURE 2. Schematic representation of 2-L VSI

The number of carrier signal required for the 2L VSI is 1 (N-1). The switching table for 2L VSI considering phase A is given in Table 1. The arrangement of reference and carrier signal for 2L VSI is shown in Fig. 3. Whenever the carrier signal is higher than reference signal, the pulse is generated and given to switches. The output voltage of this



arrangement has two level such as $+V_{dc}$ and $-V_{dc}$.

FIGURE 3. Pulse Generation for 2L inverter

Table 1. Switching Table for 2L inverter

States	S_{11}	S_{12}	Output Voltage
p	1	0	V_{dc}
n	0	1	$-V_{dc}$

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C. Multi-Level Inverter:

Multi-Level Inverter Topologies are widely used in High Voltage AC Drives. On comparing to 2L VSI, MLIs has many advantages such as reduction in voltage stress across switching devices, lower dv/dt, lesser switching loss at high switching frequency, lesser harmonic contents and lower CMV. Due to these advantages, the MLI is widely preferred in high power and high frequency applications. The circuit for 3L NPC inverter is shown in Fig. 4.

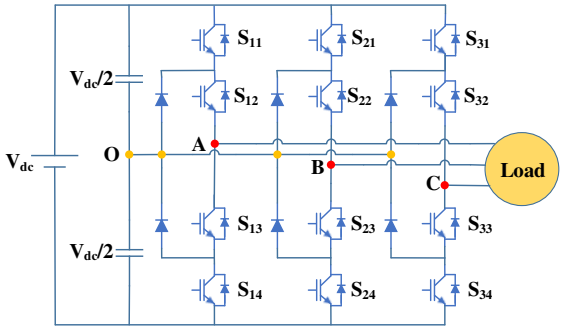


FIGURE 4. Three level Neutral Point Clamped Inverter

The number of active switches in 3L inverter is more when compare to 2L VSI. The 3L inverter has 12 switches and 6 diodes. Each leg consists of 4 switches with 2 switches in upper leg and 2 switches in lower leg. Also 2 diodes are used in each leg, with one junction is connected to neutral point of DC-link capacitor and the other junction is connected in between two switches in the upper and lower leg correspondingly. The pulse for multi-level inverter is generated by various PWM techniques. The Multicarrier PWM technique is classified as Phase Disposition (PO) PWM, Phase Opposition Disposition (POD) PWM, Alternate Phase Opposition Disposition (APOD) PWM, Phase Shifting Carrier (PSC) PWM, Interleaved Carrier (IC) PWM and Variable Frequency Carrier (VFC) PWM. The arrangements of carrier and reference signal for 3L PWM is shown in Fig. 4. The carrier signals required for 3L inverter is 2 (N-1) [212],[213].

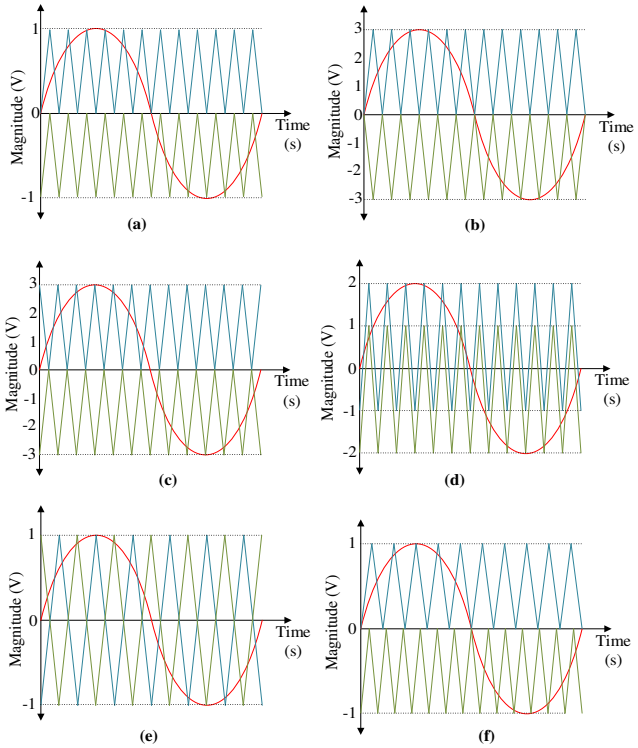
Table 2. Switching States of Phase A

States	S_{11}	S_{12}	S_{13}	S_{14}	Pole voltage
p (Positive)	0	0	1	1	$V_{dc}/2$
o (Zero)	0	1	1	0	0
n (Negative)	1	1	0	0	$-V_{dc}/2$
Invalid	1	0	0	1	-

The switching states and phase voltage of A phase is shown in Table 2. In switching states, 1 is denoted when the switch is in ON condition and 0 is denoted when the switch is in OFF condition. The pole voltage of each state will be obtained as $V_{dc}/2$, 0 or $-V_{dc}/2$. If S_{11} and S_{14} switches are turned on, then such state is not valid for the NPC inverter. The remaining 3 states will be denoted as p, o and n respectively.

In PD PWM technique [58], the carrier signals are placed at different position in above and below of the zero reference as shown in Fig.5 (a). While in POD PWM technique [59], the carrier signals are not only placed in different positions but also the phase angles are shifted by 180° for the signals placed below zero reference when compared to the signals placed above zero reference as shown in Fig.5 (b).

FIGURE 5. Arrangements of Reference and Carrier signal waveforms of phase A for 3-level NPC inverter for (a) PD, (b) POD, (c) APOD, (d) IC, (e) PSC, (f) VFC PWM techniques



In APOD PWM technique [60], the alternative carrier signals are shifted by 180° to each other as given in Fig..5 (c). The carrier signals will not overlap each and also the amplitude and frequency remain same in above three methods [213]. In IC PWM technique [61], the amplitude and frequency will be same for all carrier signals but one carrier signal will overlap with the other carrier signal in some parts as shown in Fig.5 (d). In PSC PWM technique [62], all the carrier signals will be at same amplitude level and frequency will also be same, but each carrier signal will be shifted by certain degrees based on the number of levels is shown in Fig.5 (e). The phase angle of carrier signals shifted is calculated as 180°/N. The frequency of all carrier signal will not be same for VFC PWM technique [63] as shown in Fig.5 (f).

In case of 3L inverter both POD and APOD technique will be similar to each other. However, in higher level inverter they both will be different as shown below. The seven level PWM generation using POD and APOD technique is shown in Fig. 6. The following section discusses about the Space Vector Modulation Techniques [212].

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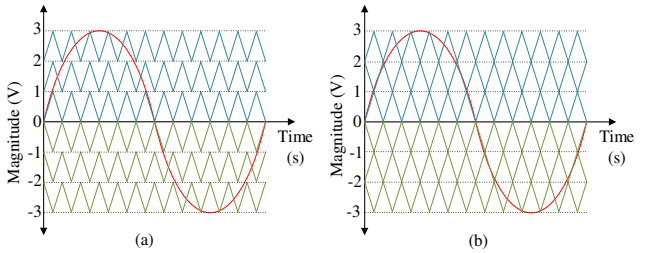

FIGURE 6. Arrangements of Reference and Carrier signal waveforms of phase A for 7 level NPC inverter for (a) POD, (b) APOD PWM techniques

D. Results of MLI for different MCPWM techniques:

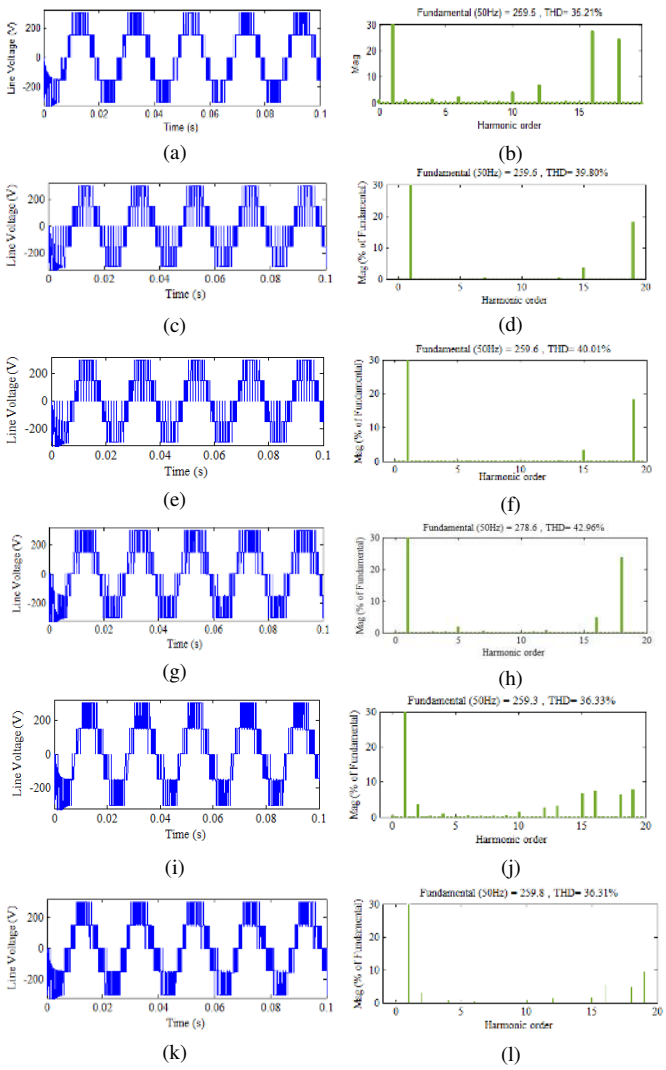

FIGURE 7. Line-to-Line Voltage of (a) PO, (c) POD, (e) APOD, (g) IC, (i) PSC and (k) VFC PWM. Voltage THD of (b) PO, (d) POD, (f) APOD, (h) IC, (j) PSC and (l) VFC PWM

The input dc voltage is considered as 300V to perform the simulation with 10kHz switching frequency. The line voltage waveforms and THD chart upto 20 harmonics are captured for PO, POD, APOD, IC, PSC and VFC PWM techniques and shown in Fig. 7 (a-l).

The MATLAB simulation is carried out for various PWM techniques of 3L inverter at different modulation indices and the results are noted in Table 3. From the obtained results, it is observed that IC PWM technique provides high line voltage but the THD% is very poor when compared to other PWM techniques. While, the PO PWM technique has considerable lesser THD% among MC PWM techniques and the line voltage is almost similar to line voltage obtained from other PWM techniques.

Table 3. Line Voltage and THD for various PWM Techniques

M_i	PD		POD		APOD	
	V	THD%	V	THD%	V	THD%
1	259.5	35.21	259.6	39.80	259.6	40.01
0.9	233.6	33.82	233.4	37.67	233.8	38.01
0.8	207.68	31.78	207.5	36.58	207.8	36.88
0.7	181.72	34.67	181.5	38.31	181.8	35.85
0.6	155.76	39.56	155.6	42.14	155.8	40.31
M_i	IC		PSC		VFC	
	V	THD%	V	THD%	V	THD%
1	278.6	42.96	259.3	36.33	259.8	36.31
0.9	250.7	41.13	233.6	34.76	236.2	35.06
0.8	222.8	39.58	207.6	32.91	210.6	33.81
0.7	195.1	40.15	181.7	35.81	187.8	34.95
0.6	167.1	41.26	155.7	37.26	162.3	36.03

The output harmonics in MC PWM techniques are high. To reduce the harmonics, SVM technique is introduced. Also, DC-link voltage balancing can be done in SVM which is difficult in MCPWM technique. The voltage stress at switches can be reduced while using SVM technique. The next section deals with SVM technique for 2L and 3L inverter.

III. SPACE VECTOR MODULATION:

The SVM technique is a digital modulating technique which generates PWM based on the vector representation. These digital signals are given directly to switches which are controlled as per vector representation. The vectors are placed in hexagonal structure for representing magnitudes and phases of each vector. The SVM which is represented in α-β frame is the conventional technique. The SVM can also be represented in g-h coordinate system and K-L coordinate system.

A. Space Vector Techniques Based on Axis Frame:

1) CONVENTIONAL (α-β frame) SVPWM TECHNIQUE

In [64], various space vector PWM techniques are discussed. The SVM shown in Fig. 6 is conventional (α-β frame) SVM technique. The axis of α is along 0^0 and β is along 90^0. The reference voltage is given in below equation:

$$V_{ref} = \frac{2}{3}[V_a + \alpha V_b + \alpha^2 V_c] \quad (1)$$

where $\alpha = e^{j2\pi/3}$

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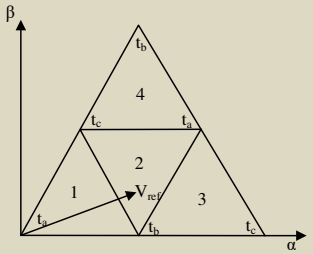
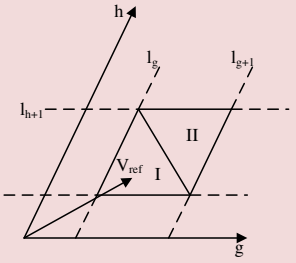
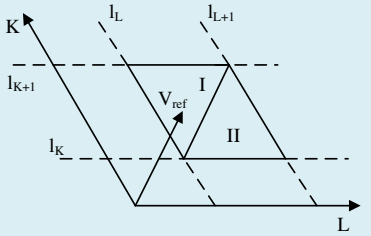
Table 4. Relation between abc frame with different coordinate systems

	α-β frame	g-h Coordinate system	K-L Coordinate system
Vector Representation			
Relation with abc frame	$\begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$	$\begin{bmatrix} V_{rg} \\ V_{rh} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$	$\begin{bmatrix} V_{rL} \\ V_{rK} \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$
Volt Sec Balance	$V_{ref}T_s = V_8t_a + V_1t_b + V_7t_c$ $T_s = t_a + t_b + t_c$	$V_{rg}T_s = V_{ag}t_{g,h} + V_{bg}t_{g+1,h} + V_{cg}t_{g,h+1}$ $V_{rh}T_s = V_{ah}t_{g,h} + V_{bh}t_{g+1,h} + V_{ch}t_{g,h+1}$ $T_s = t_{g,h} + t_{g+1,h} + t_{g,h+1}$	$V_{rL}T_s = V_{aL}t_{L,K} + V_{cL}t_{L,K+1} + V_{dL}t_{L+1,K+1}$ $V_{rK}T_s = V_{aK}t_{L,K} + V_{cK}t_{L,K+1} + V_{dK}t_{L+1,K+1}$ $T_s = t_{L,K} + t_{L,K+1} + t_{L+1,K+1}$

2) SVPWM BASED ON g-h COORDINATE SYSTEM

In g-h coordinate system, the g axis is placed along 0^0 which overlaps α axis and h axis is shifted by 60^0 from g axis.

3) SVPWM BASED ON K-L COORDINATE SYSTEM

The K-L coordinate system is also referred as 120^0 coordinate system. In this system, the L axis is overlapped with α axis at 0^0 and the K axis is shifted by 120^0 from L axis in clockwise direction. The volt-sec balance and the relation between abc frame and the corresponding frames are shown in Table 4.

B. 2 Level SVM:

The 2L SVM for 3-phase inverter has 8 switching states ($x^n = 2^3 = 8$) and it contains 6 active vectors and 2 zero vectors [65]-[71]. In the switching sequence, "n" is denoted when the lower switch is active whose corresponding voltage is $-V_{dc}$ and "p" is denoted when the upper switch is active whose corresponding voltage is $+V_{dc}$. The space vector diagram for 2L inverter is shown in Fig. 8.

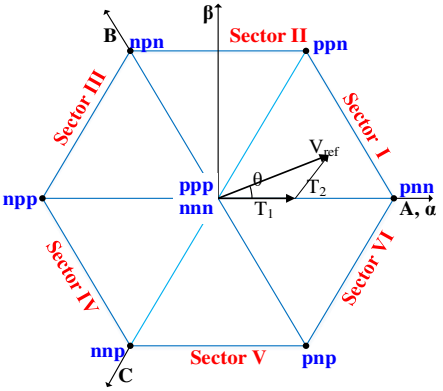


FIGURE 8. Space Vector Diagram of 2-Level Inverter

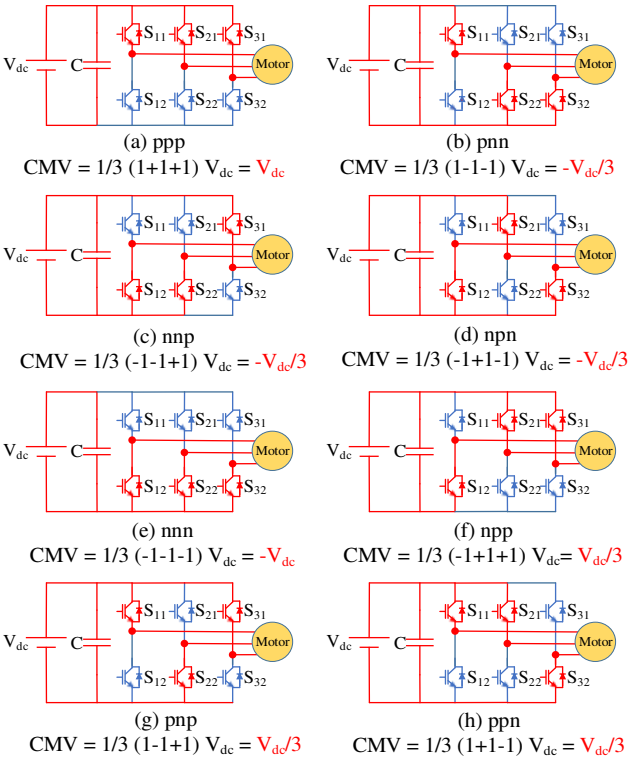


FIGURE 9. Effects of Switching States of 2L Inverter

Table 5. Conventional Switching Sequences of 2 Level Inverter

Sector	Switching Sequence
Sector 1	ppp-ppn-pnn-nnn-pnn-ppn-ppp
Sector 2	ppp-ppn-npn-nnn-npn-ppn-ppp
Sector 3	ppp-npp-npn-nnn-npn-npp-ppp
Sector 4	ppp-npp-nnp-nnn-nnp-npp-ppp
Sector 5	ppp-pnp-nnp-nnn-nnp-npn-ppp
Sector 6	ppp-pnp-pnn-nnn-pnn-pnp-ppp

The conventional SVM switching sequence for different sectors of 2L inverter is given in Table 5. The effects of

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various switching States with their CMV for 2L VSI is shown in Fig. 9.

If the reference vector is placed in sector I. V_1 and V_2 are the two nearest voltage vectors to reference vector and V_Z is the zero-voltage vector. T_1, T_2 and T_Z are the corresponding time duration for reference vectors. The Volt-Second equation is given as

$$V_{ref} T_s = V_1 T_1 + V_2 T_2 + V_z T_z \quad (2)$$

where $T_s = T_1 + T_2 + T_z$

From the vector diagram, the following equations are derived.

$$T_1 + T_2 \cos 60^0 = m\, T_s \cos \alpha \quad (3)$$

$$T_2 \sin 60^0 = m\, T_s \sin \alpha \quad (4)$$

Where $m = \frac{V_{ref}}{V_{dc}}$

On solving the above equations, the time period can be calculated.

$$T_1 = (m.T_s)\frac{\sin(60^0 - \theta)}{\sin(60^0)} \quad (5)$$

$$T_2 = (m.T_s)\frac{\sin(\theta)}{\sin(60^0)} \quad (6)$$

$$T_Z = T_s - T_1 - T_2 \quad (7)$$

Though 2L SVM is easy to apply, there are many disadvantages. The 2L inverters can be used only for low power and low frequency applications. For the application of high power and high frequency, the 3L inverter is introduced.

The SVM and switching sequence of 3L NPC MLI is discussed in following sub-section.

C. 3 Level SVM:

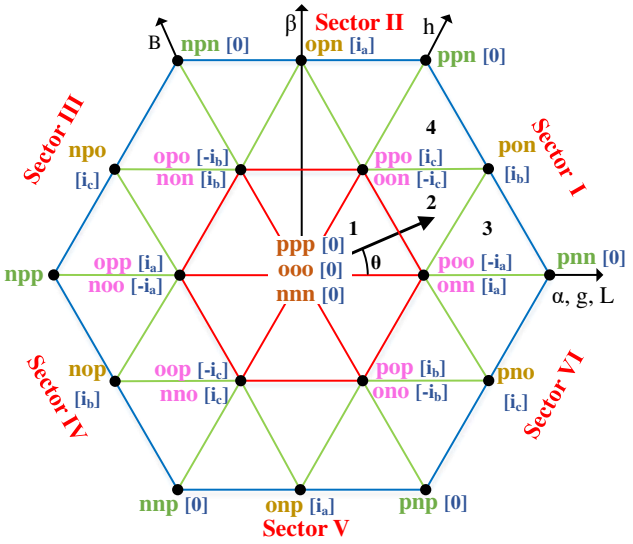

FIGURE 10. Space Vector Modulation of 3L Inverter

The 3L inverter has 27 switching states with 3 Zero vectors, 12 Small vectors, 6 Medium vector and 6 Large vectors. Among those 27 switching states ($x^n = 3^3 = 27$), 8 states are redundancy states and the remaining 19 vector states are placed in space vector diagram in Fig. 10. The SVM is divided into 6 sectors and each sector is divided into 4 sub-sectors. The neutral point current of each vector is denoted in the SVM diagram [72]-[78]. The effects of various switching states for the 3L inverter are shown in Fig. 11. The conventional SVM switching sequence for six sectors of the 3L NPC MLI is given in the Table 6.

Table 6. Conventional switching sequence of the three-level inverter SVM

Sector	Sub-sector	Switching sequence
1	1	nnn-onn-oon-ooo-poo-ppo-ppp-ppo-poo-ooo-oon-onn-nnn
	2	onn-oon-pon-poo-ppo-poo-pon-oon-onn
	3	onn-pnn-pon-poo-pon-pnn-onn
	4	ppo-ppn-pon-oon-pon-ppn-ppo
2	1	ppp-ppo-opo-ooo-oon-non-nnn-non-oon-ooo-opo-ppo-ppp
	2	non-oon-opn-opo-ppo-opo-opn-oon-non
	3	oon-opn-ppn-ppo-ppn-opn-oon
	4	non-npn-opn-opo-opn-npn-non
3	1	ppp-opp-opo-ooo-noo-non-nnn-non-noo-ooo-opo-opp-ppp
	2	opp-opo-npo-noo-non-noo-npo-opo-opp
	3	non-npn-npo-opo-npo-npn-non
	4	oop-nop-nnp-nno-nnp-nop-oop
4	1	ppp-opp-oop-ooo-noo-nno-nnn-nno-noo-ooo-oop-opp-ppp
	2	nno-noo-nop-oop-opp-oop-nop-noo-nno
	3	opp-npp-nop-noo-nop-npp-opp
	4	oop-nop-nnp-nno-nnp-nop-oop
5	1	ppp-pop-oop-ooo-ono-nno-nnn-nno-ono-ooo-oop-pop-ppp
	2	pop-oop-onp-ono-nno-ono-onp-oop-pop
	3	oop-onp-nnp-nno-nnp-onp-oop
	4	pop-pnp-onp-ono-onp-pnp-pop
6	1	ppp-pop-poo-ooo-ono-onn-nnn-onn-ono-ooo-poo-pop-ppp
	2	pop-poo-pno-ono-onn-ono-pno-poo-pop
	3	pop-pnp-pno-ono-pno-pnp-pop
	4	poo-pno-pnn-onn-pnn-pno-poo

In conventional SVM method, the reference vector is identified based on the three vectors which are placed nearest to the reference vectors. Hence it is also known as Nearest Three Vector (NTV) method.

IV. CMV AND NPF OF 3 PHASE INVERTER:

A. Common Mode Voltage

The common mode voltage for the inverter is calculated from $V_{CMV} = (V_{ao} + V_{bo} + V_{co})/3$. The High frequency model of a 3-phase inverter motor drive is shown in Fig. 12. The common mode current for 3-phase inverters will be flowing through the stray capacitance C_g and it is calculated by

$$i_g = i_a + i_b + i_c = 3i_o = C_g \frac{dv_g}{dt} \quad (8)$$

The common mode model for 3-phase load is shown in Fig. 13. (a), where l_o, R_o and C_{wo} are the zero-sequence component of L, R and C respectively. The differential mode model for three phase load is shown in Fig. 13. (b), where the l_q, R_q and C_{wq} are the q-axis component of L, R and C respectively, while the d-axis model will be same as the q-axis model [79], [80].

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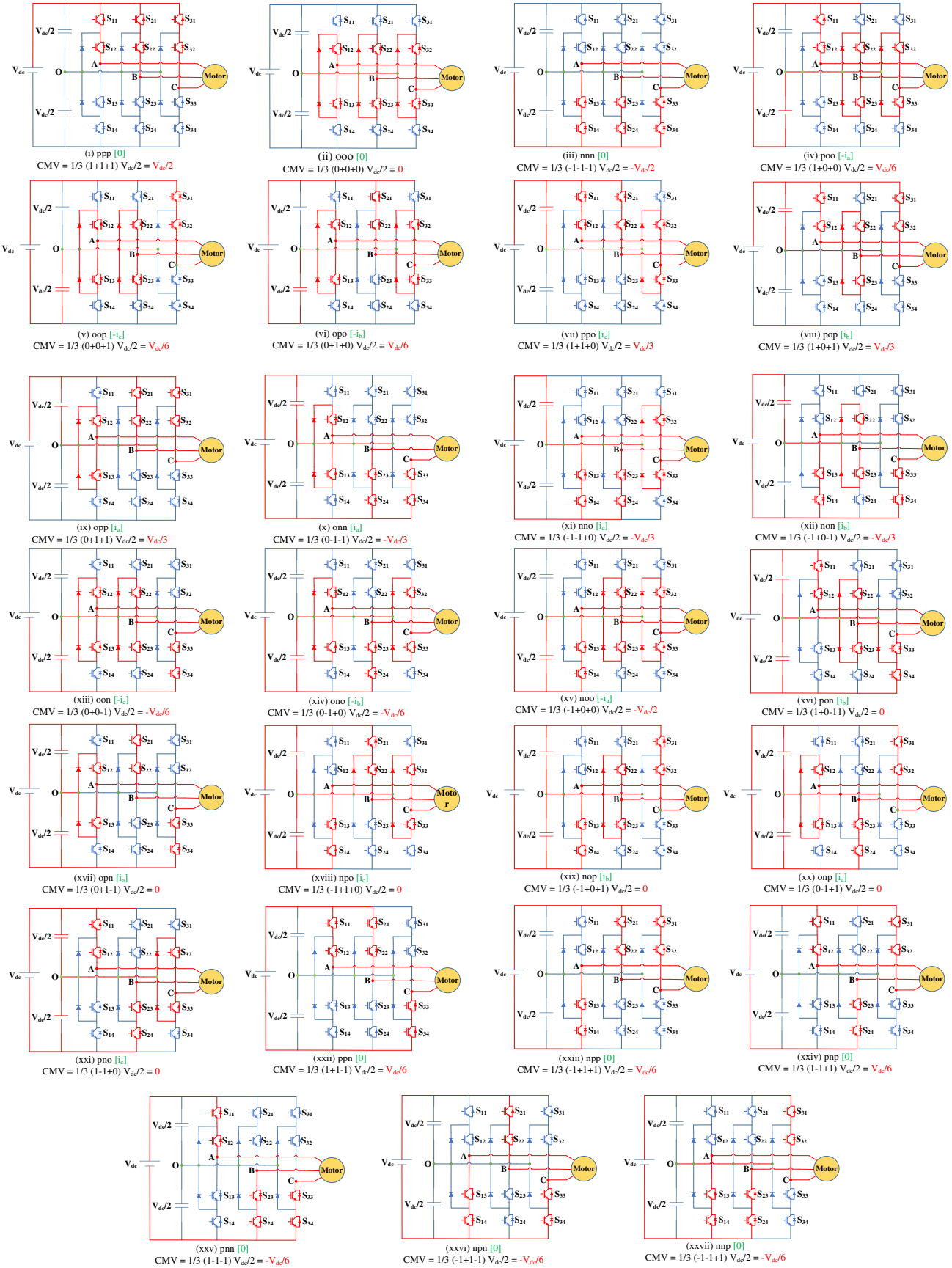

FIGURE 11. Effects of Switching States of 3 Level SVM

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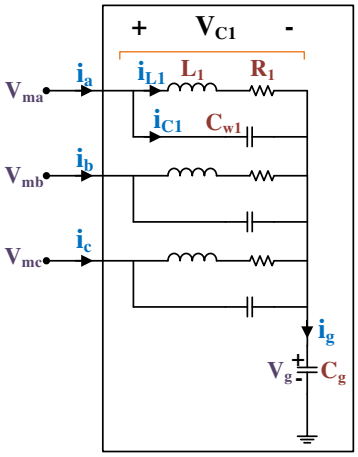

FIGURE 12. High Frequency model of CMV for 3 phase

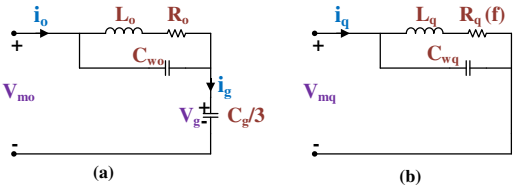

FIGURE 13. (a) Common Mode model of a 3-phase load, (b) Differential Mode model of a 3-phase load

The admittance transfer function for common mode model (Y_o) and differential mode model ($Y_q = Y_d$) is given as

$$Y_o = \frac{i_o}{v_o} = \frac{sC_gL_oC_{wo}\left[s^2+s\frac{R_o}{L_o}+\frac{1}{L_oC_{wo}}\right]}{L_o(C_g+3C_{wo})\left[s^2+s\frac{R_o}{L_o}+\frac{3}{L_o(C_g+3C_{wo})}\right]} \quad (9)$$

$$Y_d = Y_q = \frac{i_q}{v_q} = \frac{C_{wq}\left[s^2+s\frac{R_q(f)}{L_q}+\frac{1}{L_qC_{wq}}\right]}{L_q\left[s+\frac{R_q(f)}{L_q}\right]} \quad (10)$$

The CMV of 2L inverter is $\pm V_{dc}/3$ and $\pm V_{dc}$, while the CMV for 3L inverter is as follows: $\pm V_{dc}/6$, $\pm V_{dc}/3$, $\pm V_{dc}/2$ and 0. It is observed that the CMV for 3L inverter ($\pm V_{dc}/6$) is less when compared to CMV of 2L inverter ($\pm V_{dc}$). The CMV for each vector along with their output voltage levels of 2L and 3L inverters are listed in Table 7 and Table 8 respectively.

Table 7. Switching States and CMV of 2L Inverter

Switching States	CMV Calculation	CMV
nnn (Zero)	$(-V_{dc} -V_{dc} -V_{dc})/3$	$-V_{dc}$
pnn	$(V_{dc} -V_{dc} -V_{dc})/3$	$-V_{dc}/3$
ppn	$(V_{dc} +V_{dc} -V_{dc})/3$	$V_{dc}/3$
npn	$(-V_{dc} +V_{dc} -V_{dc})/3$	$-V_{dc}/3$
npp	$(-V_{dc} +V_{dc} +V_{dc})/3$	$V_{dc}/3$
nnp	$(-V_{dc} -V_{dc} +V_{dc})/3$	$-V_{dc}/3$
pnp	$(V_{dc} -V_{dc} +V_{dc})/3$	$V_{dc}/3$
111 (Zero)	$(V_{dc} +V_{dc} +V_{dc})/3$	V_{dc}

Table 8. Output voltage and CMV of the each switching states in 3L inverter

Vectors	Switching States	CMV	Voltage level
Zero Vectors	ooo	0	0
	ppp	$V_{dc}/2$	
	nnn	$-V_{dc}/2$	
Small Vectors	poo, oop, opo	$V_{dc}/6$	$V_{dc}/3$
	ppo, pop, opp	$V_{dc}/3$	
	onn, nno, non	$-V_{dc}/3$	
	oon, ono, noo	$-V_{dc}/6$	
Medium Vectors	pon, opn, npo, nop, onp, pno	0	$V_{dc}/\sqrt{3}$
Large Vectors	ppn, npp, pnp	$V_{dc}/6$	$2V_{dc}/3$
	pnn, npn, nnp	$-V_{dc}/6$	

The simulation results of CMV for 3L NPC MLI of various MC PWM is shown in Fig. 14 (a-f). The results are obtained for PO, POD, APOD, IC, PSC and VFC PWM techniques.

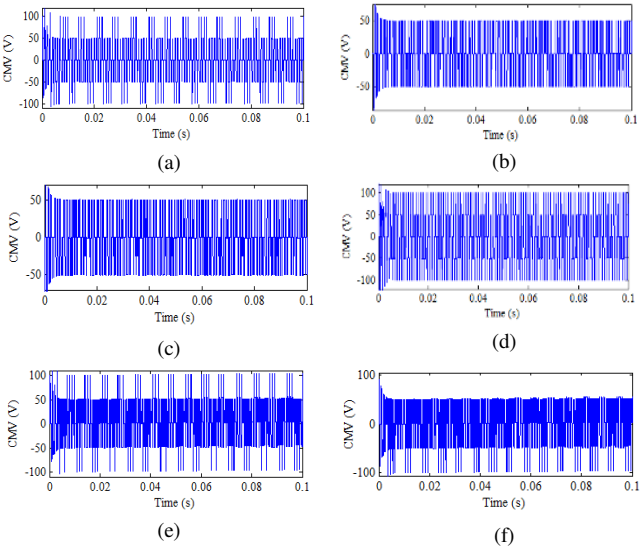

FIGURE 14. CMV of (a) PO, (b) POD, (c) APOD, (d) IC, (e) PSC and (f) VFC PWM.

The SVM diagram is redrawn with the values of CMV for each vector in Fig.15. It can be noticed that the CMV of medium vectors are zero which plays a major role in the reduction on CMV in the NPC MLI.

The effects of CMV in the sector I of the 3L SVM is shown in Fig. 16. The changes in CMV from one switching state to other switching state is also represented for each switching sequences of sector I.

B. Neutral Point Fluctuation:

The multi-level inverter has (n-1) DC-link capacitors which should have equal voltages (V_{dc}/n-1). Due to third harmonic injection, unequal commutation of semiconductors devices, etc. the DC-link voltages will not be same.

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This variation in DC-link voltage is known as Neutral Point Fluctuation [81] and it is calculated as

$$NPF = \frac{\frac{V_{dc}}{n-1} - V_{c2}}{\frac{V_{dc}}{n-1}} * 100 \qquad (11)$$

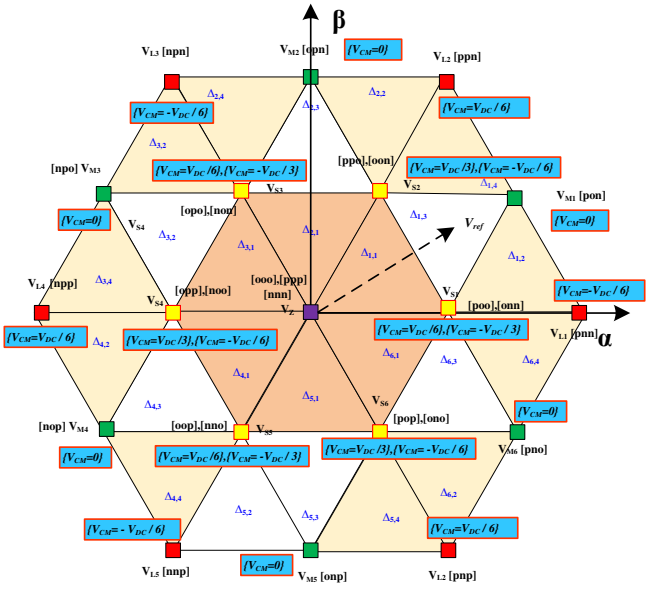

FIGURE 15. 3L SVM diagram with CMV calculation

The CMV and NPF has been noted in simulation by applying different PWM techniques in 3L NPC MLI which in given in the Table 9. The allowable value for Neutral Point Fluctuation is 1% as per IEEE standard [213]

Table 9. Common Mode Voltage and Neutral Point Fluctuation for various PWM Techniques

PWM Techniques	PD	POD	APOD	IC	PSC	VFC	SVM
NPF %	0.6	0.6	1.2	0.8	0.6	0.5	0.4
CMV	50	100	50	50	50	50	100

The Time duration of reference voltage from the nearest three vector for each sub-sector of the 3L inverter SVM is given in the Table 10.

C. Elimination of CMV:

The common mode voltage is eliminated by selecting the suitable vectors that produces zero CMV. The zero vectors like PPP and NNN can be neglected as it produces the CMV of $V_{dc}/2$ and $-V_{dc}/2$ respectively [82]-[84]. If the small vector is neglected, then the CMV will be reduced from $V_{dc}/3$ to $V_{dc}/6$. The large vector which is responsible for the production of CMV of $V_{dc}/6$ is removed and the resultant output will be free from CMV.

The different CMV reduction processes are discussed by various authors is given in Table 11. These effects have been researched by various authors as cited below.

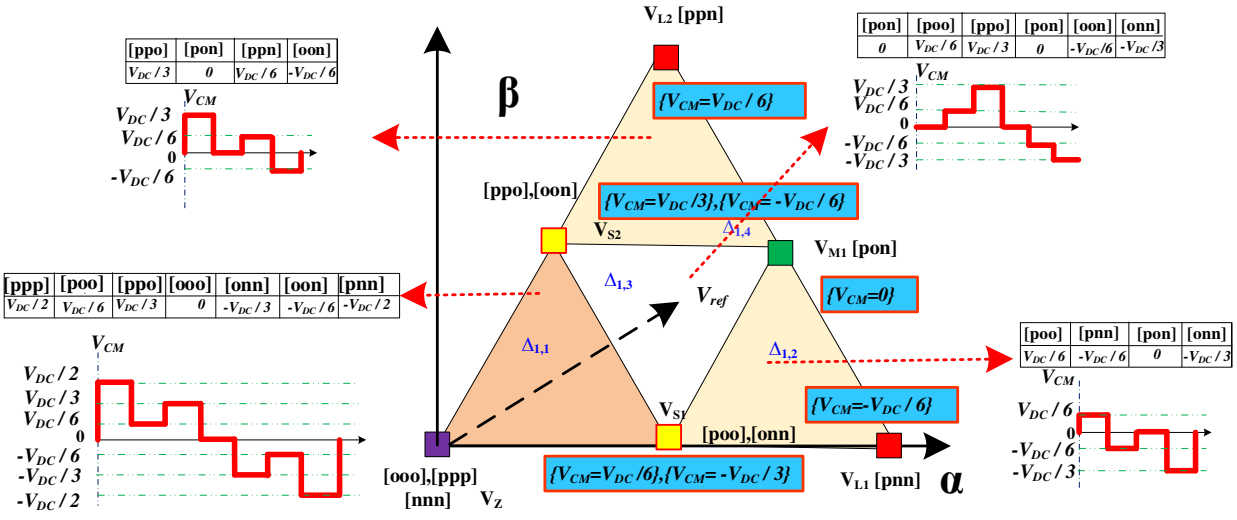

FIGURE 16. Sector I representation of 3L SVM with the effect of CMV

Table 10. Time duration of reference voltage from nearest three vector

Sub-Sector	T_1	T_2	T_3
1	$T_s\left(2 - m\sin\left(\frac{\pi}{3} - \theta\right)\right)$	$T_s\left(1 - 2m\sin\left(\frac{\pi}{3} + \theta\right)\right)$	$T_s\left(2m\sin(\theta)\right)$
2	$T_s\left(1 - 2m\sin(\theta)\right)$	$T_s\left(2m\sin\left(\frac{\pi}{3} + \theta\right) - 1\right)$	$T_s\left(1 - 2m\sin\left(\frac{\pi}{3} - \theta\right)\right)$
3	$T_s\left(2 - m\sin\left(\frac{\pi}{3} + \theta\right)\right)$	$T_s\left(2m\sin(\theta)\right)$	$T_s\left(2m\sin\left(\frac{\pi}{3} - \theta\right) - 1\right)$
4	$T_s\left(2m\sin(\theta) - 1\right)$	$T_s\left(2m\sin\left(\frac{\pi}{3} - \theta\right)\right)$	$T_s\left(2 - 2m\sin\left(\frac{\pi}{3} + \theta\right)\right)$

Table 11. Effect of CMV based on vector representation

Ref	CMV Reduction process	Effect of CMV
[85]	Large Vector and Medium Vector	The switching states which have CMV of $\pm V_{dc}/2$ and $\pm V_{dc}/3$ are not considered. Instead, their redundant states which has lower CMV alone is taken which results in the reduction of CMV.
[86], [94]	1 Zero vector (ooo) and 6 medium vectors	The "ooo" vector and medium vectors are only used and the remaining vectors are not included in SVM. As these vectors will generate only 0 CMV, the CMV is eliminated with this process.
[87], [91]	V_7 and V_0 is eliminated and the remaining vectors are rotated by 30^0	If the switching is from even to odd state or vice-versa and switching from even to V_7 or odd to V_0 then $1/3V_{dc}$ CMV is obtained, whereas switching from even to V_0 or odd to V_7 then $2/3V_{dc}$ CMV is obtained. While switching from even to even or odd to odd has no variation in common mode voltage. The vectors V_7 and V_0 is eliminated so as to reduce the CMV, but the reference voltage is restricted to $0.5V_{DC}/2$. If the reference voltage is exceeded then line-to-line voltage and phase currents are distorted. Therefore, remaining vectors are rotated by 30^0 and resultant vectors are used. This results in increasing the maximum peak voltage reference to $0.58V_{DC}/2$.
[88]	Zero Redundant State PWM	In PODPWM technique two carriers (A1 and A2) are used to generate the pulse, while in Zero redundant state PWM technique four carriers (A1, A2, A1* and A2*) are used. The A1* and A2* are the phase shifted by 1800 from A1 and A2. Due to this, the redundant states are eliminated which results in the reduction of CMV to $\pm V_{dc}/6$.
[89], [90]	Redundant vectors are removed	The redundant vectors in zero and small vectors are removed. Theses vectors produce $\pm V_{dc}/2$ and $\pm V_{dc}/3$ at zero and medium vectors respectively. On removing thes vectors, the CMV is reduced.
[92], [93]	Active Zero State PWM	The zero state is avoided in this process. The adjacent vectors (V_1 and V_2) of reference vector are accompanied by active zero pairs (V_3 and V_6). Since the zero state is avoided, CMV is reduced to $\pm V_{dc}/6$.
[94]	Three nearest medium vectors (M^3V)	In this method only 6 medium vectors are considered and the remaining vector are eliminated. As CMV of medium vector is zero, the resultant CMV of the inverter is also zero.

Many researches have been made for the reduction of CMV in NPC MLI inverter as discussed in [95]-[98]. The power loss and switching loss analysis of MLI is done in [99]-[103]. The comparative study between different PWM techniques is made in [104]-[106].

V. MODIFIED SVM TECHNIQUES:

In 3L inverter, the major issue is balancing of DC-link capacitance voltages. To eliminate this capacitance balancing issues, there are 3 main methods are available [107].

- Using two separate isolated DC-Voltage sources with the help of two independent rectifiers.
- Using back-to-back topology
- Using the carrier or space vector modulation techniques without external hardware

In Table 6, it is noticed that the number of switching sequence is not equal for all the sub-sectors which results in the different switching frequency. Due to the variation in switching frequency, the switching losses is increased. Many researchers have proposed some modified SVM Techniques that balances the DC-link capacitance voltages and reducing the losses. [108]- [110]. The Table 12 gives the effect of DC-link capacitance under modified SVM techniques as per citations given.

Table 12. Various Modified SVM Techniques for Balancing the DC-Link Capacitance

Citation	Effect of DC-link capacitor balancing
[111], [112]	The medium vectors with higher modulation index are restricted. The modulation indices for 4 regions are given below. $mg+mh \leq 0.5$ for region I $mg+mh > 0.5$ && $mg < 0.5$ && $mh < 0.5$ for region II $mg > 0.5$ && $mh > 0.5$ && $mg \geq mh$ for region III $mg > 0.5$ && $mh > 0.5$ && $mg < mh$ for region IV
[113]	1. Based on phase currents: a. Large and Zero vectors does not have the phase current that results in proper balancing of capacitor voltages b. Medium vectors that have non-zero phase creates the imbalance in capacitor voltages 2. Based on Modulation Index: a. When modulation index is $0 \leq m < 0.5$, only the small vector are active vectors. As a result, the DC-link capacitor is in balanced condition. b. When modulation index is $0.5 \leq m < 0.8$, both medium and small vectors are active vectors. Due to the presence of medium vectors, the capacitor balancing will be poor. c. When modulation index is $0.8 \leq m < 0.907$, the active medium vector will compensate the small vectors which leads to the high capacitor imbalance. Selected Three Vector Scheme: As the modulation index goes beyond 0.5, the capacitor balancing will happen due to the presence of medium vectors. To reduce the influence of medium vector, the V_g is introduced at equal distance from V_{S1}, V_{S2} and V_M which is considered as the mean of vectors.
[114]	Long Vectors and Zero vectors will have the balanced capacitor voltages as these vectors have zero neutral point current. The medium vectors are responsible for imbalance of capacitor voltages. The small vectors that have redundant vectors are used for the balancing of capacitor voltages. For small vectors, only one DC-link capacitor will have the charging and discharging effect. In large vector, both the capacitors (C_1 and C_2) will have charging and discharging effect with the active current of one leg that is involved in the medium vector. In medium vector, the DC-link capacitors C_1 will charge and discharge with the active current in one leg and the capacitor C_2 will charge and discharge with active current in other leg.
[115], [116]	In large unbalance condition of DC bus capacitor, the reference vector spends more time in region 3 when compared to the time spent in region 2 and 4. Thus the effect of redundant switching state becomes prominent for longer period of time that results in quick balancing of DC bus capacitor voltages. When the unbalancing in DC-link capacitor voltage reduces, the reference vector spends less

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	time in region 3 when compared to large unbalance condition. The initial and final trajectory position of V_{ref} is plotted. The V_{ref} in large unbalance condition follows the initial trajectory and V_{ref} in lesser unbalance condition follows the final trajectory position.

Abhijit Choudhury, et.al, have proposed few modified SVM techniques for balancing the DC-link capacitance. In [117], the author has compared the DC-link capacitor voltages and given as an input to control logic along with the carrier signal which selects the required switching sequence in SVM techniques. The diagram for this logic is given in Fig. 17.

When V_{dc1} is greater than V_{dc2}, the switching sequence is selected so that V_{dc1} is discharged. Likewise, when V_{dc2} is greater than V_{dc1}, the switching sequence is selected so that V_{dc2} is discharged. The corresponding switching sequence is given in Table 13. With this topology, the balancing of DC-link capacitance voltage is done. The control logic will update the information of voltage differences only at the beginning of each switching cycle, so that duty cycle cannot be changed in between the switching cycle. It makes the generated PWM more symmetrical.

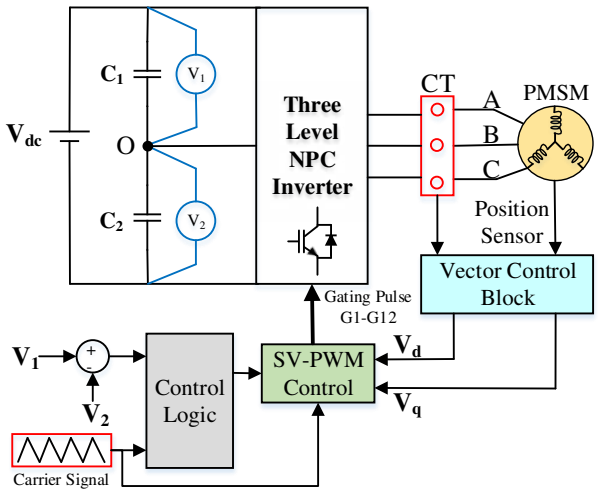

FIGURE 17. NPC inverter for DC-link balancing

Table 13. Switching sequence of the modified 3L inverter SVM for sector I

Sub-sector	Balancing Ability	Switching sequence
1	$V_{dc1} > V_{dc2}$	ooo-poo-ppo-poo-ooo
	$V_{dc2} > V_{dc1}$	nnn-onn-oon-onn-nnn
2	$V_{dc1} > V_{dc2}$	poo-ppo-pon-ppo-poo
	$V_{dc2} > V_{dc1}$	onn-oon-pon-oon-onn
3	$V_{dc1} > V_{dc2}$	poo-pon-pnn-pon-poo
	$V_{dc2} > V_{dc1}$	onn-pnn-pon-pnn-onn
4	$V_{dc1} > V_{dc2}$	ppo-ppn-pon-ppn-ppo
	$V_{dc2} > V_{dc1}$	onn-pon-ppn-pon-onn

The switching sequence is equal for all conditions which makes the switching frequency constant. as shown in Table 13. As a result of constant switching frequency, the switching losses is reduced. In this scheme, the total harmonics is reduced to 50% on comparing to conventional methods [118].

The above scheme is modified and proposed in [119]-[122]. In this scheme, the DC-link voltage balancing is done on considering the current direction along with voltage differences.

Table 14. Switching sequence of 3L inverter using current direction for sector I

Sub-sector	Balancing Ability	Current Direction	Switching sequence
1	$V_{dc1} > V_{dc2}$	$i_c<0$	ooo-poo-ppo-poo-ooo
		$i_c>0$	ooo-poo-oon-poo-ooo
	$V_{dc2} > V_{dc1}$	$i_c<0$	ooo-onn-oon-onn-ooo
		$i_c>0$	ooo-onn-oon-onn-ooo
2	$V_{dc1} > V_{dc2}$	$i_c<0$	poo-ppo-pon-ppo-poo
		$i_c>0$	poo-oon-pon-oon-poo
	$V_{dc2} > V_{dc1}$	$i_c<0$	onn-oon-pon-oon-onn
		$i_c>0$	oon-ppo-pon-ppo-oon
3	$V_{dc1} > V_{dc2}$	$i_a>0$	poo-pon-pnn-pon-poo
	$V_{dc2} > V_{dc1}$	$i_a>0$	onn-pnn-pon-pnn-onn
4	$V_{dc1} > V_{dc2}$	$i_c<0$	ppo-ppn-pon-ppn-ppo
		$i_c>0$	oon-pon-ppn-pon-oon
	$V_{dc2} > V_{dc1}$	$i_c<0$	oon-pon-ppn-pon-oon
		$i_c>0$	ppo-ppn-pon-ppn-ppo

The two DC-link capacitance voltages are compared and given to control logic which generates a command signal to the SVPWM control block. The load current is measured using current sensing block and given to SV-PWM control logic that generates the switching sequence. The diagram for this logic scheme is shown in Fig. 18 and the corresponding switching sequence is given in Table 14.

The selected vectors keep the capacitor voltage deviations within 5% of total DC-link voltage. Two zero switching vectors (i.e., ppp and nnn) which produces higher common mode voltages are also removed from all subsectors.

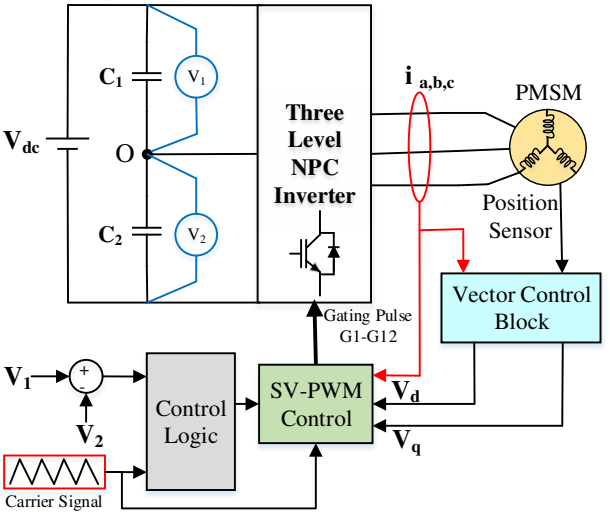

FIGURE 18. NPC inverter for DC-link balancing using current direction

The hybrid PWM strategy is discussed in [123]-[124], its block diagram is shown in Fig. 19. In this scheme, 5 blocks are used to generate the PWM. The reference voltage from load is given to duty cycle generator which produces the duty ratio. The duty ratio and carrier signal are given to comparator block and the reference gate pulse is

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generated which is given to revised gate pulse generator block and redundant vector identifier block. The redundant states are found by redundant vector identifier block with the help of reference gate pulse. If redundant voltage vector is found, then it is replaced by corresponding redundant states depending on two capacitance voltages.

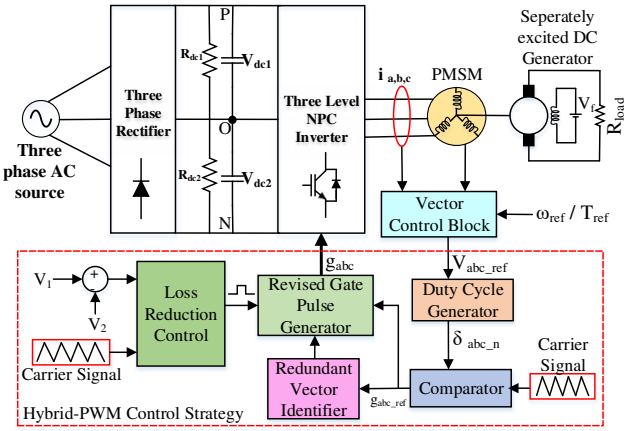

FIGURE 19. NPC inverter for DC-link balancing with Hybrid-PWM control strategy

The DC-link voltage differences are calculated and given to loss reduction control block along with carrier frequency. If loss reduction control block produces high signal, the redundant states are flipped by revised gate pulse generator block. Otherwise, it will generate the duties without flipping redundant states The redundancy vector and their corresponding switching sequence is given Table 15.

Table 15. Switching sequence of the Hybrid PWM Strategy

Sub-sector	Balancing Ability	Switching sequence
poo	$V_{dc1} > V_{dc2}$	poo
	$V_{dc2} > V_{dc1}$	onn
onn	$V_{dc1} > V_{dc2}$	poo
	$V_{dc2} > V_{dc1}$	onn
ppo	$V_{dc1} > V_{dc2}$	ppo
	$V_{dc2} > V_{dc1}$	oon
oon	$V_{dc1} > V_{dc2}$	ppo
	$V_{dc2} > V_{dc1}$	oon
opo	$V_{dc1} > V_{dc2}$	opo
	$V_{dc2} > V_{dc1}$	non
non	$V_{dc1} > V_{dc2}$	opo
	$V_{dc2} > V_{dc1}$	non
opp	$V_{dc1} > V_{dc2}$	opp
	$V_{dc2} > V_{dc1}$	noo
noo	$V_{dc1} > V_{dc2}$	opp
	$V_{dc2} > V_{dc1}$	noo
oop	$V_{dc1} > V_{dc2}$	oop
	$V_{dc2} > V_{dc1}$	nno
nno	$V_{dc1} > V_{dc2}$	oop
	$V_{dc2} > V_{dc1}$	nno
pop	$V_{dc1} > V_{dc2}$	pop
	$V_{dc2} > V_{dc1}$	ono
ono	$V_{dc1} > V_{dc2}$	pop
	$V_{dc2} > V_{dc1}$	ono
pon, opn, npo, nop, onp, pno	$V_{dc1} > V_{dc2}$ or $V_{dc2} > V_{dc1}$	pon, opn, npo, nop, onp, pno
pnn, ppn, npn, npp, nnp, pnp	$V_{dc1} > V_{dc2}$ or $V_{dc2} > V_{dc1}$	pnn, ppn, npn, npp, nnp, pnp

In [125] four different switching sequence control strategy is discussed. Out of 4 strategy, 3 strategies use two large and one redundant vector (medium vectors are removed) and the remaining 1 strategy uses two large and one null voltage vectors. The different strategies are as follows;

1. Lower Triangle Vector Sequence Based Control Strategy
2. Upper Triangle Vector Sequence Based Control Strategy
3. Mix Vector Sequence Based Control Strategy
4. Two-Level Equivalent of Three-Level Inverter

In these strategies, the medium vectors are removed and generated reference phase voltage is found with the help of two large and one redundant vector as shown in Fig. 20.

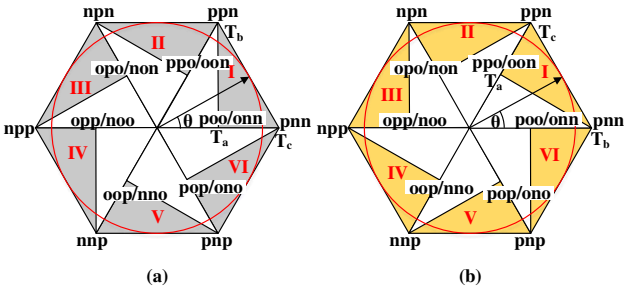

FIGURE 20. (a) Vector diagram with lower triangle. (b) Vector diagram with upper triangle

Because of the absence of medium voltage vectors, the neutral point fluctuation is reduced. The Switching sequence for upper and lower triangle vector sequence is given in Table 16. The number of switching states of both upper and lower triangle switching sequence is same.

Table 16. Lower and Upper Triangle vector control Switching Sequence

Sector	Balancing Ability	Lower Triangle Switching Sequence	Upper Triangle Switching Sequence
1	$V_{dc1} > V_{dc2}$	poo-pnn-ppn-pnn-poo	ppo-ppn-pnn-ppn-ppo
	$V_{dc2} > V_{dc1}$	onn-pnn-ppn-pnn-onn	oon-ppn-pnn-ppn-oon
2	$V_{dc1} > V_{dc2}$	ppo-ppn-npn-ppn-ppo	opo-npn-ppn-npn-opo
	$V_{dc2} > V_{dc1}$	oon-ppn-npn-ppn-oon	non-npn-ppn-npn-non
3	$V_{dc1} > V_{dc2}$	opo-npn-npp-npn-opo	opp-npp-npn-npp-opp
	$V_{dc2} > V_{dc1}$	non-npn-npp-npn-non	noo-npp-npn-npp-noo
4	$V_{dc1} > V_{dc2}$	opp-npp-nnp-npp-opp	oop-nnp-npp-nnp-oop
	$V_{dc2} > V_{dc1}$	noo-npp-nnp-npp-noo	nno-nnp-npp-nnp-nno
5	$V_{dc1} > V_{dc2}$	oop-nnp-pnp-nnp-oop	pop-pnp-nnp-pnp-pop
	$V_{dc2} > V_{dc1}$	nno-nnp-pnp-nnp-nno	ono-pnp-nnp-pnp-ono
6	$V_{dc1} > V_{dc2}$	pop-pnp-pnn-pnp-pop	poo-pnn-pnp-pnn-poo
	$V_{dc2} > V_{dc1}$	ono-pnp-pnn-pnp-ono	onn-pnn-pnp-pnn-onn

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The Mix vector sequence-based control strategy uses both lower and upper triangle vector sequence-based control strategy. When the position of reference voltage vector is less than 30° the lower triangle vector sequence is used because, the distance between upper triangle vector and the reference voltage vector is more. Likewise, when the position of reference voltage vector is greater than 300 then the upper triangle vector control strategy is used. The 2L equivalent of 3L inverter is also discussed. In this strategy, the small or redundant vectors are eliminated which will completely eliminate the neutral point voltage fluctuation as there is no redundancy vectors. The space vector diagram of 2L equivalent of 3L inverter is shown in Fig. 21.

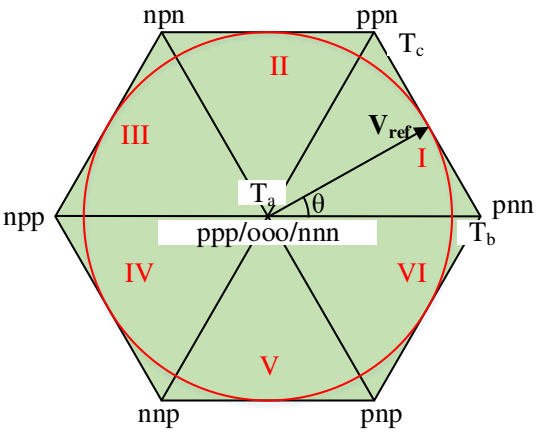

FIGURE 21. Two-Level Equivalent of Three-Level Inverter

The voltage and current harmonic values are measured in simulation and are tabulated collectively in the Table 17. From the table it is seen that the harmonics of Mix sequence control strategy is closer to conventional strategy.

Table 17. Voltage and current harmonics of various space vector strategies

Harmonics	Voltage Harmonics	Current Harmonics
Conventional	6.44%	1.75%
Lower Triangle	12.94%	2.49%
Upper Triangle	12.58%	2.58%
Mix Sequence	8.45%	2.16%
2 Level Equivalent	14.52%	4.53%

In three-medium vector (M^3V) method, only the medium vectors are used that reduces CMV to near zero value. The CMV voltages of the medium vector are calculated as zero as mentioned earlier.

Another method to reduce the CMV is one zero vector and two medium vectors (M^2ZV), where the "ooo" from zero vector and the medium vector which has zero CMV is utilized for the generation of pulses. The SVM of M^3V and M^2ZV is shown in Fig 22. (a) & (b). Though the M^3V and M^2ZV methods reduces the CMV to near zero value, they both fails to maintain the DC-link neutral point oscillation at low frequency. To overcome this issue, a hybridization of M^3V and M^2ZV is done. This hybridization of M^3V+M^2ZV not only reduces the CMV to near zero value, but also improves the DC-link capacitor balancing with lower conduction losses [94].

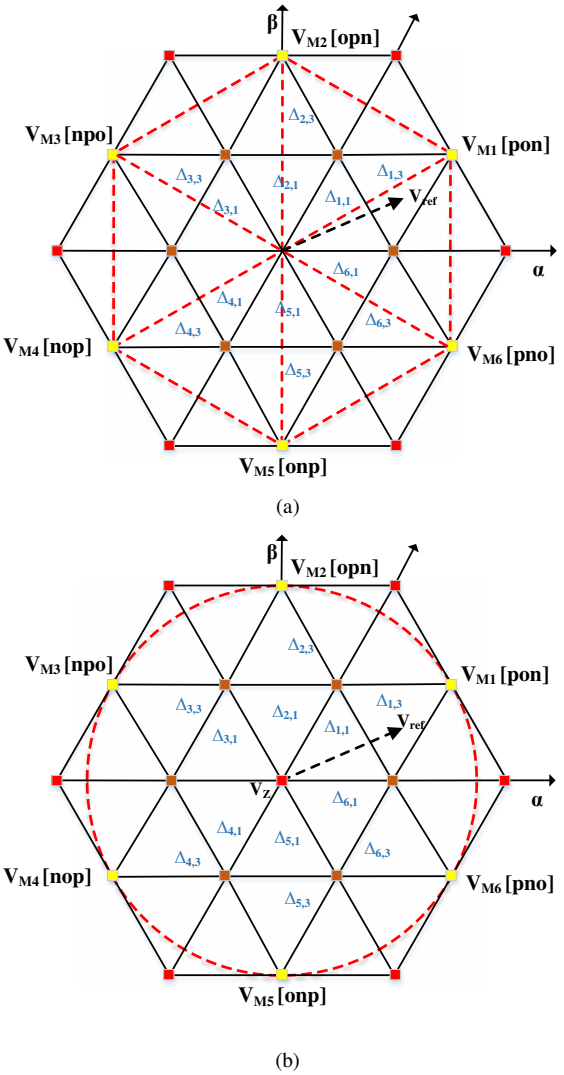

FIGURE 22. SVM Diagram of (a) M^3V method and (b) M^2ZV method

An optimized SVM Technique is proposed so as to reduce the neutral point ripple current [222]. In this technique, V_{ref} is generated without considering the small vectors in where V_{ref} is placed. The SVM diagram for this technique is shown in Fig 23.

The small vector in other sector is selected instead of small vector in current sector. The alternative small vector is selected by the following equations.

$$V_{small-alternate} = \begin{cases} \overrightarrow{V_{n+1}}, & when\ V_{ref}\ is\ in\ sector\ n-(A) \\ \overrightarrow{V_{n-1}}, & when\ V_{ref}\ is\ in\ sector\ n-(B) \end{cases} \quad (12)$$

where n = 1, 2, …, 6.

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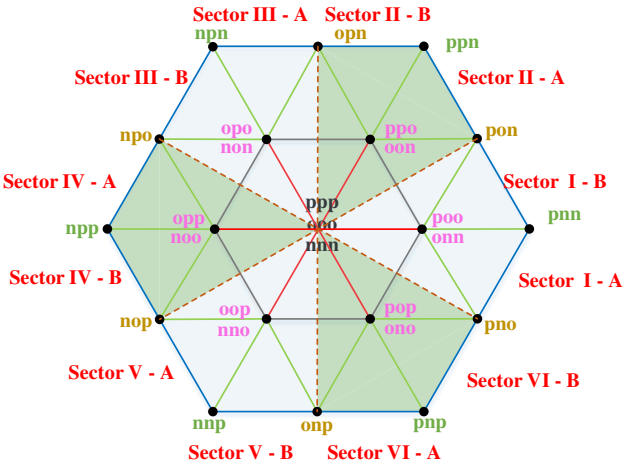

FIGURE 23. Optimized SVM Diagram of 3L NPC

The vector selection of the optimized SVM is shown in Fig. 24. From the vector selection is noticed that the switching states "onn and poo" is replaced by optimized vectors "ono and pon" in Sector I-B which reduces the neutral point current. The other possible vector "oon and pon" will provide higher current than optimized vector.

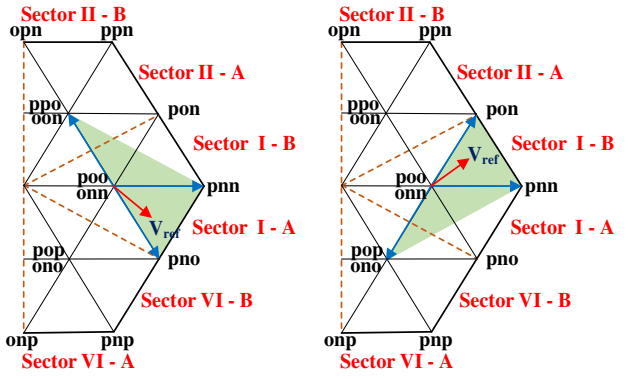

FIGURE 24. Vector representation Optimized SVM technique (a) Sector I-A, (b) Sector I-B

A SVM technique is proposed in [223] so as to reduce the common mode voltage. In this technique, sectors are divided into 12 divisions, based on the difference in upper capacitor voltage and lower capacitor voltage the vectors are selected. The vectors with lower CMV are only considered in this technique. The SVM diagram for this technique is shown in Fig. 25.

If the reference vector is placed in sector 1, the large vector (pnn or ppn), medium vector (pon), small vector (poo or oon) and zero vector (ooo) are selected. The small vector is selected based on differences in dc link capacitor voltages. If the upper capacitor voltage is high, the vector "poo" is selected. If the lower capacitor voltage is high, the vector "oon" is selected.

Various Control strategies like proportional controller [126], zero sequence injection [127],[128], Field Oriented Control (FOC), Direct Torque Control (DTC) [129]-[133], Sliding mode control [134]-[136] and hysteresis control [137] are developed by the researchers for reducing the DC-link voltage balancing issues for 3-phase NPC MLI.

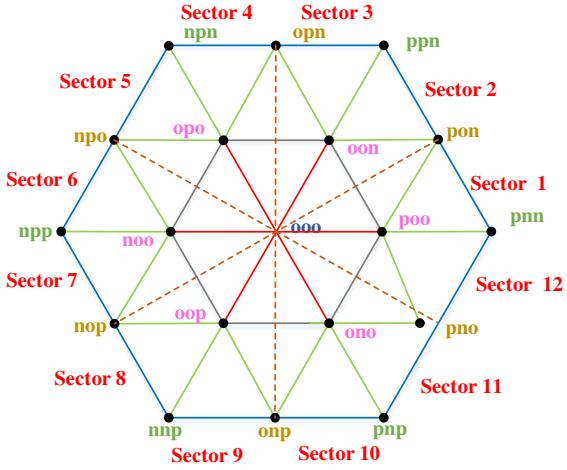

FIGURE 25. SVM Diagram for reduced CMV of 3L NPC

VI. VIRTUAL SPACE VECTOR MODULATION AND 3D SVM:

A. *Virtual Space Vector Modulation*

The VSVM is another modulation technique for controlling NPC inverter in which the medium vectors that are responsible for neutral point fluctuation is eliminated and the virtual vectors are considered instead of medium vectors [139]-[142], [230], [231]. The virtual vector is chosen based on two small vectors and medium vector in corresponding sector. There are 27 inverter states available in VSVM, which is divided into 3 null vectors, 12 small vectors, 6 virtual vectors and 6 large vectors. The voltage calculation for virtual vector based on two small vectors and one medium vector is given in the following eqn.

$$V_v = \frac{(V_{sv1}+V_{sv2}+V_{mv})}{3} \quad (13)$$

where V_{sv1} and V_{sv2} are the voltages of small vectors and V_{mv} is the voltage of medium vector in corresponding sectors.

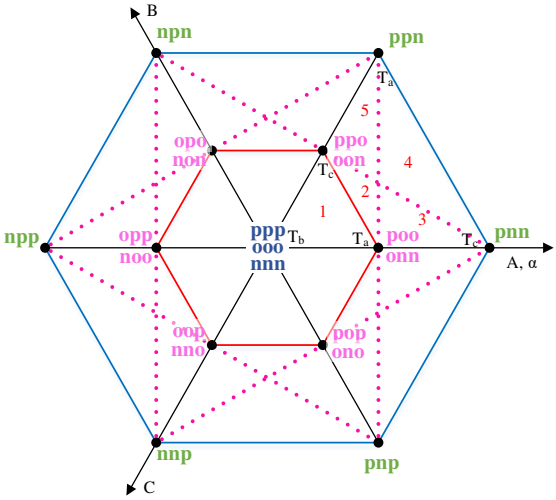

FIGURE 26. Virtual Space Vector Modulation

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The VSVM diagram is given in Fig. 26. The number of subsectors in each sector is increased from 4 to 5 because of the introduction of Virtual vector. The sector representation of both SVM and VSVM are shown in the Fig. 27. Finding the NTV in VSVM will take less time when compared to conventional SVM. The conventional switching sequence for VSVM of sector 1 is given in the Table 18.

Table 18. Switching Sequence for VSVM of Sector I

Sector	Sub-sector	Switching sequence
1	1	ooo-poo-ppo-ooo-oon-onn
	2	poo-onn-ppo-oon-onn-pon-ppo
	3	poo-onn-onn-pon-ppo-pnn
	4	pnn-ppo-onn-pon-ppn
	5	ppo-oon-ppo-onn-pon-ppn

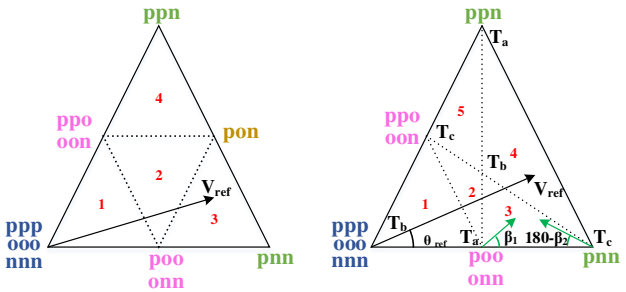

FIGURE 27. Sector one representation for conventional and virtual SVM

The reference voltage vector angles (β_1 *and* β_2) are used to cover all the subsectors. The position of reference voltage vector is identified based on the values of β_1 *and* β_2 which is given in the Table 19.

Table 19. Subsector Identification

β_1	β_1	Subsector
> 120°	> 150°	1
< = 120° && > 90°	> = 150°	2
< = 90°	> = 150°	3
< = 90°	< 150°	4
> 90°	< 150°	5

In modified VSVM [143], the DC-link capacitance voltages are compared and switching sequence is selected based on the difference in capacitance voltages. This results in balancing the DC-link capacitance voltages. The switching sequence for modified VSVM is given in Table 20.

Table 20. Modified Switching Sequence of VSVM for sector I

Sub-sector	Balancing Ability	Switching sequence
1	$V_{dc1} > V_{dc2}$	ooo-poo-ppo-poo-ooo
	$V_{dc2} > V_{dc1}$	ooo-oon-onn-oon-ooo
2	$V_{dc1} > V_{dc2}$	ppo-poo-pon-poo-ppo
	$V_{dc2} > V_{dc1}$	onn-oon-pon-oon-onn
3	$V_{dc1} > V_{dc2}$	pnn-pon-poo-ppo-poo-pon-pnn
	$V_{dc2} > V_{dc1}$	pnn-onn-oon-pon-oon-onn-pnn
4	$V_{dc1} > V_{dc2}$	pnn-ppn-ppo-poo-pon-poo-ppo-ppn-pnn
	$V_{dc2} > V_{dc1}$	ppn-pnn-onn-oon-pon-pon-oon-onn-pnn-ppn
5	$V_{dc1} > V_{dc2}$	ppn-ppo-poo-pon-poo-ppo-ppn
	$V_{dc2} > V_{dc1}$	ppn-pon-oon-onn-oon-pon-ppn

In this modified VSVM, out of 3 zero vectors only "ooo" vector is used and the remaining two zero vectors either "ppp or nnn" is not utilized. Due to the elimination of "ppp and nnn", the common mode voltage is reduced to 1/3rd of V_{dc}.

A Reduced CMV VSVM technique is discussed in [224], the space vector diagram of this technique is shown in Fig. 28. The reduction of CMV is achieved by abandoning the vectors which generates higher CMV. The vector $U_{NZS1.1}$ located in small vector region at 0° angle (poo, onn region) can be virtualized by "pon and ono" at the same action time. Here we can notice that "pop" state which generate high CMV is not considered. Likewise, the vector $U_{NZS1.2}$ is virtualized by "oon and pno". The vector $U_{NZS2.1}$ and $U_{NZPS2.2}$ can be virtualized by (pon, opo) and (poo, opn) respectively.

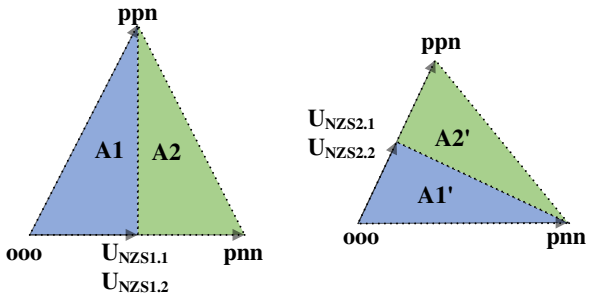

FIGURE 28. SVM diagram of Reduced CMV VSVM

B. 3D SVM:

The 3D SVM technique is the advanced PWM method of SVM. The 3D SVM can be applied to three leg and four leg (four wire) inverters. Initially the three leg inverters are considered for discussion. [146]-[148]

In 2D SVM, there are 6 redundant switching states available, but in case of 3D SVM the redundant switching states are not present. The absence of redundant switching states provides the better performance in inverter by reducing the switching losses. The 3D SVM is represented in a cubic structure. The 27 switching states of 3D SVM are classified into 4 types of vectors similar to 2D SVM (3 Zero vectors, 12 Small vectors, 6 Medium vectors and 6 Large vectors). The 3D SVM for three leg NPC inverter is shown in Fig. 29.

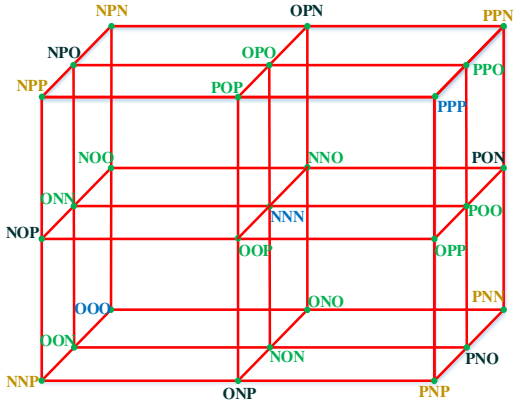

FIGURE 29. 3D SVM diagram for 3L inverter

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The 3D SVM can also be applied to four-leg inverter. The first three leg represents three phases and the fourth leg represents neutral line [149]-[152]. The SVM for 3-phase 2L four-leg inverter is given in Fig. 30. The 3-dimensional axis for vector diagram is named as α, β and δ axis. There are 16 switching states placed in seven δ plane (2L SVM plane) available for 2L four-leg inverter whose voltage levels are V_{dc}, 2/3 V_{dc} ,1/3 V_{dc}, 0, -1/3 V_{dc}, -2/3 V_{dc} and -V_{dc} respectively from top to bottom of SVM. [165]

For 3L four leg inverter, 81 switching states are placed in fifteen δ planes (3L SVM plane) with the voltage level various from V_{dc} to - V_{dc} at the difference of $V_{dc}/2\sqrt{3}$ between each plane [153].

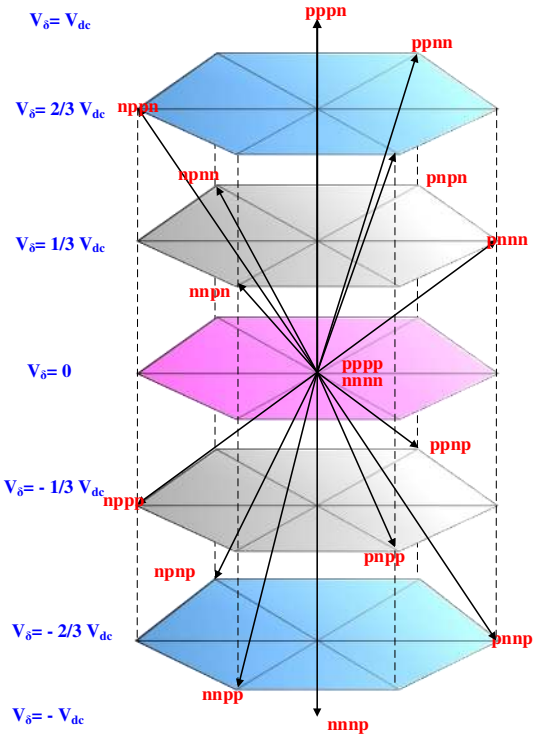


FIGURE 30. 3D SVM diagram for 2L four leg inverter

VII. ASYMMETRICAL DC-LINK VOLTAGES FOR INVERTERS AND OVERMODULATION REGION IN SVM:

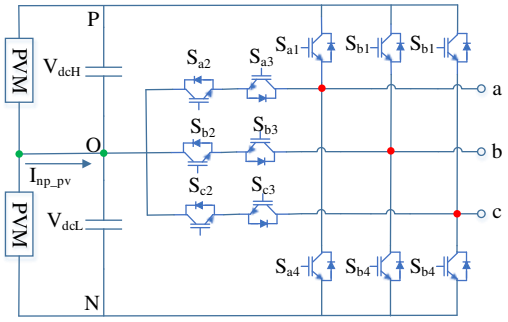
A. Asymmetrical DC-link Voltages

In multi-level inverter generally the DC-link capacitance voltages are kept symmetrical. In PV applications, the DC-link voltages will be asymmetrical due to the partial shading conditions [154], [155], [233]. The schematic diagram for 3L inverter in PV applications is given in Fig. 31. The split DC-link voltage can be described as

$$V_{dcH} + V_{dcL} = V_{dc} \quad (14)$$

$$\boldsymbol{V_{dcH} - V_{dcL} = \delta V_{dc}} \quad (15)$$

In sector 1, consider if the system gets asymmetrical DC-link voltages, then the small, medium and large vector are placed as in Fig. 32. The two redundant small vectors "ppo and oon" will be overlapping each other. If the system gets asymmetrical DC-link voltages, the position of small vectors "opp and noo" will be deviated from its vector positions which results in the deviation of medium vector



(npo and nop) positions.

FIGURE 31. PV modules and the T-type three-level PV inverter

The real voltage difference between the capacitor voltages ($V_{dcH} - V_{dcL}$) is defined as V_{dif} and the reference voltage difference is defined as V_{dif}*. The capacitor voltage can be controlled by adding or subtracting the minimum time T_{min} to T_a, T_b and T_c. If ΔV_{dif} is outside $\Delta V_{dif\text{-}band}$ the following equation is used to calculate new time offset.

The turn on time for V_{dif}* - V_{dif} > 0 is given as

$$T_a' = T_a + T_{min} \quad (16)$$

$$T_b' = T_b + T_{min} \quad (17)$$

$$T_c' = T_c + T_{min} \quad (18)$$

The turn on time for V_{dif}* - V_{dif} < 0 is given as

$$T_a' = T_a - T_{min} \quad (19)$$

$$T_b' = T_b - T_{min} \quad (20)$$

$$T_c' = T_c - T_{min} \quad (21)$$

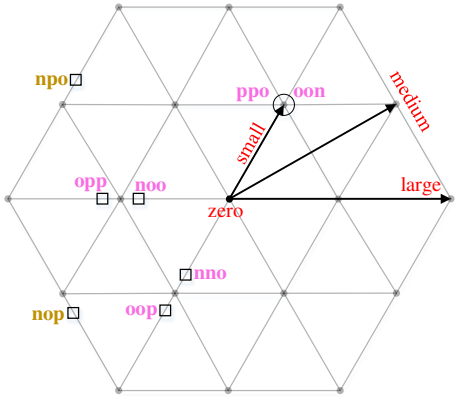


FIGURE 32. Space-vector diagram of three-level inverters for asymmetrical DC-link voltages

If ΔV_{dif} is in $\Delta V_{dif\text{-}band}$, then the time offset is reduced to $\alpha.T_{min}$. The magnitude of α is set according to ΔV_{dif}. The switching sequence for different conditions are shown in Fig. 33. The calculation of time offset is shown in the flowchart in Fig. 34

The change in turn on time will result in change in output voltages [156], [157], [232]. The pole voltages are shown in Fig. 35. For symmetrical DC-link voltage, the capacitor voltage is $V_{dc}/2$. Nevertheless, in asymmetrical condition, the capacitor voltage will not be equal to $V_{dc}/2$.

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To control this voltage, the turn on time is varied which maintains the pole voltage constant.

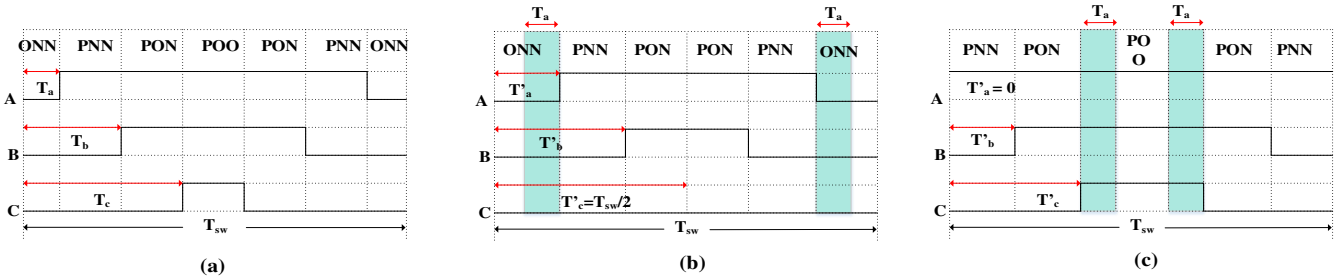


FIGURE 33. Switching sequence. (a) Normal condition. (b) After Tmin is added. (c) After Tmin is subtracted

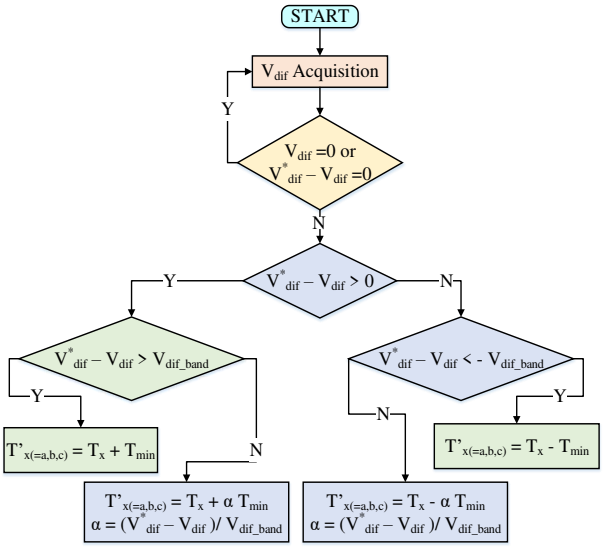


FIGURE 34. Flowchart of the proposed asymmetric control method of two capacitor voltages

If the turn on time is reduced then the resultant voltage is obtained as in Fig. 35 (a) and if the turn on time is increased by adding the T_{min} the resultant pole voltage is obtained as in Fig. 35 (b).

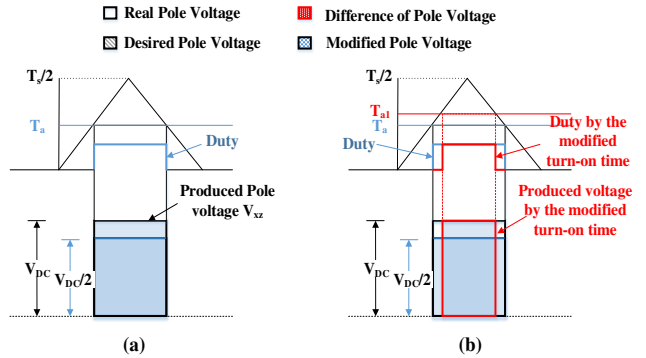


FIGURE 35. Change of output pole voltage by modifying the turn-on times

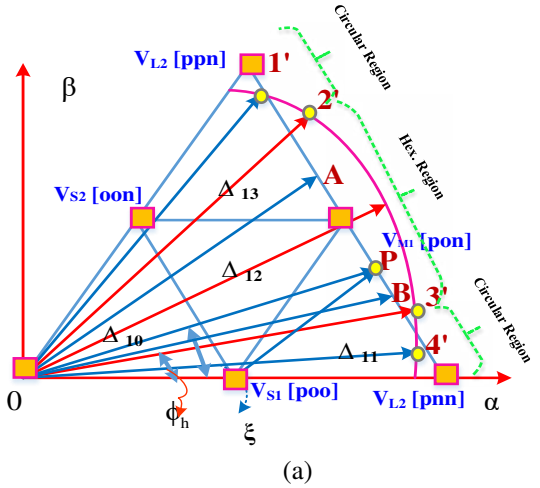
B. Over modulation region

In SVM, the normalized output voltage of the inverter is described with modulation index (M_i) ranging from zero to unity and sub-divided as linear modulation (LM) and over overmodulation (OVM). The M_i range 0 to 0.907 is LM and 0.908 to 1.0 is called OVM region. The OVM is further classified as OVM-I (M_i: 0.908 to 0.953) and OVM-II (M_i: 0.954 to 1).

In previously discussed chapters, the SVMs used in MLI are focused in LM (under modulation) indices as the performance requirements are meet out in under modulation itself. Generally, the OVM scheme is essential in electrical drive applications, if the drive is required to operate at extended speed including the field-weakening region and with higher torque and power characteristics [234], [235]. Hence the researchers tread in this field to give the significant performance of the MLI in OVM [158], [159].However, the mathematical complexity for achieving OVM is difficult. The CMV elimination in OVM is performed in [160] - [162].

The partial elimination (PE) and full elimination (FE) of CMV in OVM region is discussed and implemented in induction motor control. In PE SVM, the zero vectors which produce $\pm V_{dc}/2$ and the small vectors which produce $\pm V_{dc}/3$ is eliminated. Hence, the resultant CMV is reduced to $\pm V_{dc}/6$. The PE SVM is classified into OVM-0.908 $\leq M_i \leq$ 0.953) and OVM-II (0.953 $< M_i <$ 1) and their corresponding Space vector diagram of sector 1 is shown in Fig. 36 (a) & (b). The trajectory of V_{ref} is the combination of circular and hexagonal trajectory [160], [161]. When $M_i \leq$ 0.953, PE-OVM-I is considered and their transition from circular trajectory to hexagonal trajectory is determined by the crossover angle $\propto_c$ defined by

$$\alpha_c = \left(\frac{\pi}{6}\right) - \cos^{-1}\left(\frac{\pi}{2\sqrt{3}} M_i\right) \qquad (22)$$



(a)

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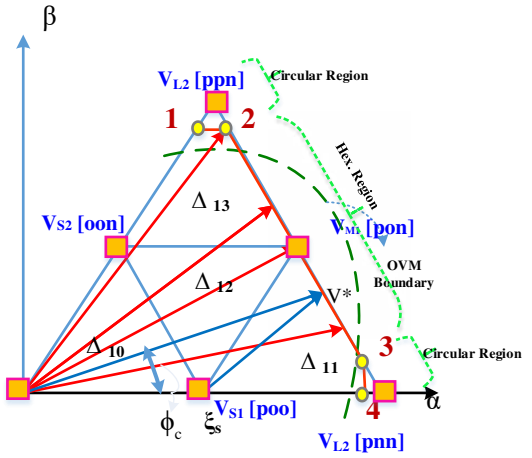

(b)

FIGURE 36. Sector-1 switching diagram for (a) PE-OVM-I, (b) PE-OVM-II

The path of original trajectory 4′-3′-2′-1′ is modified to 4-3-2-1 by changing the on-time. When the modulation index is more than 0.953 (M_i > 0.953), PE-OVM-II is considered in which the path of circular trajectory is vanished. The switching is selected based on the holding angle $\propto_h$. If V_{ref} is in upper circular region($\pi/3 - \propto_h$ *to* $\pi/3$), the large vector V_{L2} is chosen as a nearest vector. If the desired angle is between $\propto_h$ and $\pi/3 - \propto_h$, then V_{ref} tends to follow the hexagonal path.

The holding angle is calculated by the following equation.

$$\propto_h = 10.5\left(1.05 - \frac{1}{M_i}\right) \qquad (23)$$

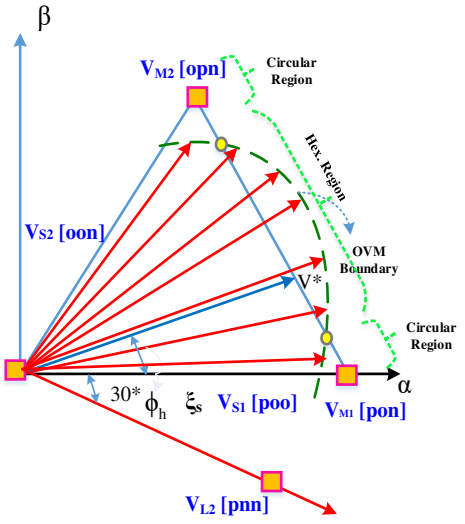

FIGURE 37. SVPWM switching and its CMV of FE-OVM

In FE OVM, the vectors which produces $\pm\frac{V_{dc}}{2}, \pm\frac{V_{dc}}{3}$ and $\pm\frac{V_{dc}}{6}$ are totally excluded and only 6 medium vector and 1 zero vectors are used. If the V_{ref} is placed in sector I, then zero vector [ooo] and medium vectors [pon & opn] are used for FE-OVM scheme. As this scheme utilizes the medium vector by neglecting small and large vectors, the reference vector is shifted by 30° and makes the drive system free from CMV. The holding angle is determined for FE OVM scheme in eq. 24. and the space vector diagram for FE OVM is shown in Fig. 37 [160].

$$\propto_h = 9.06\left(0.906 - \frac{0.866}{M_i}\right) \qquad (24)$$

In [161], the Selected Three Vector (STV) scheme used for balancing DC-link capacitor in OVM region. In this method the medium vectors are neglected to reduce neutral point fluctuation and five subsectors are used in each sector. The five subsectors which is used in sector I are (V_{zo} V_{S1} V_{S2}), (V_{S1} V_{L1} V_{S2}), (V_{S1} V_{L1} V_{L2}), (V_{S2} V_{L1} V_{L2}) and (V_{L2} V_{S1} V_{S2}). The on-time calculation for the STV is given in Table 21. This STV SVM improves the DC-link voltage utilization, THD and it reduces the neutral point fluctuation. Moreover, this scheme can be used in OVM range.

Table 21. On Time Calculation of STV

V_{ref}	Triangle	Duty Cycle
$\alpha \le 30^o$ and $V_\alpha + \sqrt{3}\,V_\beta \le 2$	Δ_a	$\delta_{VS1} = 2 - V_\alpha + \sqrt{3}\,V_\beta$ $\delta_{VS2} = V_\beta / m$ $\delta_{VL1} = 1 - \delta_{VS1} - \delta_{VS2}$
$\alpha \le 30^o$ and $V_\alpha + \sqrt{3}\,V_\beta > 2$	Δ_b	$\delta_{VL1} = -1 + V_\alpha$ $\delta_{VL2} = V_\beta / 3$ $\delta_{VS1} = 1 - \delta_{VL1} - \delta_{VL2}$
$\alpha > 30^o$ and $V_\alpha \ge 1$	Δ_c	$\delta_{VS2} = 2 - V_\alpha - (V_\beta / 3)$ $\delta_{VL1} = 0.5\,[V_\alpha - (V_\beta / 3)]$ $\delta_{VL2} = 1 - \delta_{VS2} - \delta_{VL1}$
$\alpha > 30^o$ and $V_\alpha < 1$	Δ_d	$\delta_{VS1} = V_\alpha - (V_\beta / 3)$ $\delta_{VS1} = 2 - 2V_\alpha$ $\delta_{VL2} = 1 - \delta_{VS1} - \delta_{VS2}$

VIII: SIMULATION AND EXPERIMENTAL RESULTS Of 3L SVM:

A. Simulation Results:

The MATLAB simulation for SVM technique is carried out for different modulation indices and the results of line voltage and THD% are listed in Table 22. The results obtained from SVM can be compared with the results obtained from other PWM techniques in Table 3. It can be noticed that the SVM techniques provides better results in all modulation indices when compared to other PWM techniques.

Table 22. Line Voltage and THD of SVM Technique

M_i	V	THD%
1	296.4	6.75
0.9	266.7	6.58
0.8	237.1	6.03
0.7	207.4	6.37
0.6	177.8	6.81

The simulation is carried out for different SVM techniques like conventional SVM, PE SVM, M^3V, M^2ZV and M^3V+M^2ZV techniques for the comparative purpose. The input parameters chosen for the simulation is 200V DC voltage, C_1 and C_2 is 220μF and the switches are operated in 10kHz switching frequency (f_s) and the fundamental

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frequency (f_o) as 50Hz. The line voltage, CMV and Common Mode Current of the NTV SVM, PE SVM, M^2ZV and M^3V are shown in Fig. 38. The simulation result of the hybrid M^3V+M^2ZV are shown in Fig. 39.

The DC-Link capacitor voltage waveforms are obtained from simulation for NTV SVM, PE SVM, M^2ZV, M^3V and hybrid M^2ZV and M^3V is shown in Fig. 40. The comparative results of different PWM techniques are given in Table 23.

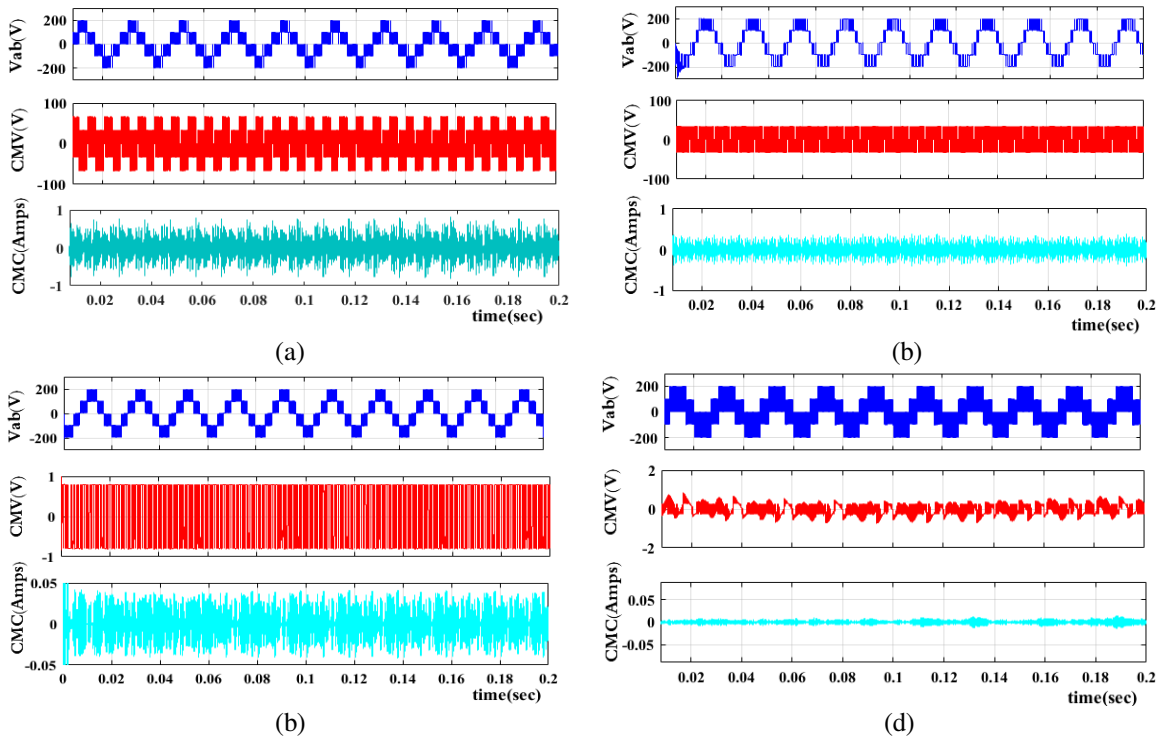


FIGURE 38. Line-to-line voltage (Vab), CMV, and CMC. (a). conventional NTV SVM, (b). PE SVM, (c). M^2ZV, (d). M^3V

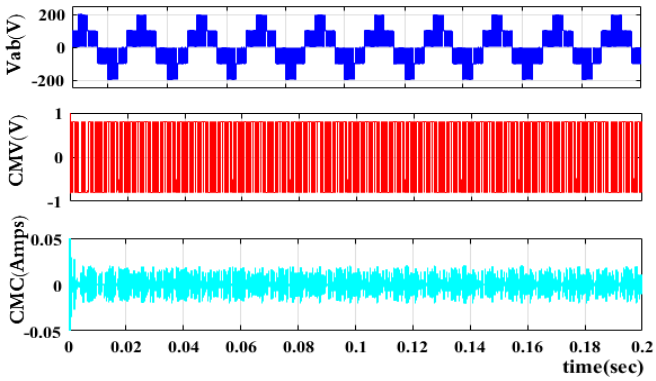
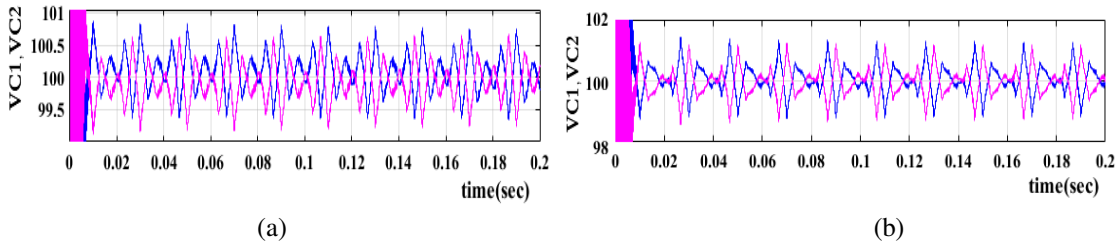


FIGURE 39. Line-to-line voltage (Vab), CMV, and CMC for hybrid M^3V+M^2ZV



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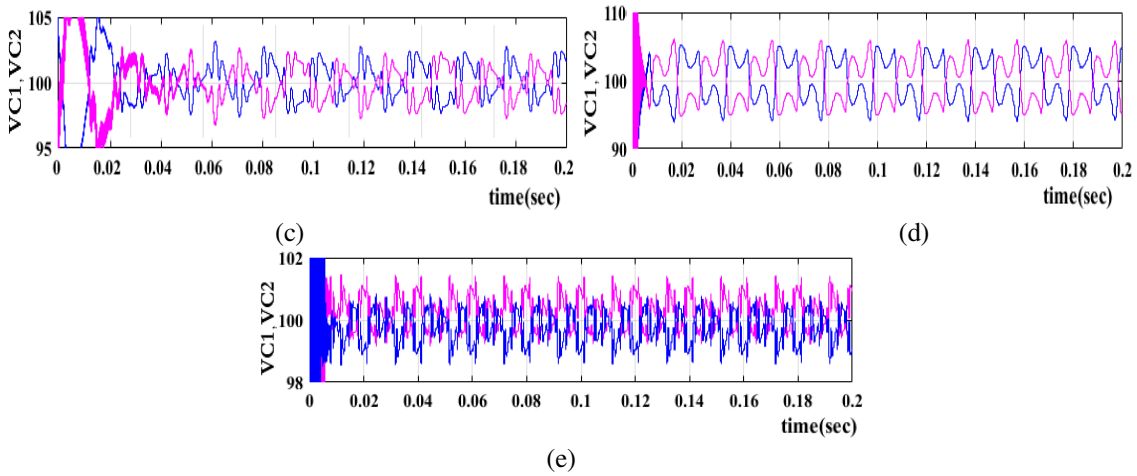

FIGURE 40. DC -link capacitor voltages V_{C1} and V_{C2} for (a). NTV SVM, (b). PE SVM, (c). M^2ZV, (d). M^3V, (e) hybrid M^3V+M^2ZV

TABLE 23 Comparison of various PWM techniques in contrast to V_{L-L}, CMV, CMC, NPF, and VTHD

PWM methods	V L-L (V)	CMV (V)	CMC (A)	NPF (%)	V THD (%)
PD	168.2	64	0.8	1.2%	13.4%
POD	167.6	34	0.4	1.5%	14.9%
APOD	168.4	36	0.4	1.9%	18.5%
PSC	173.5	65	0.8	1.1%	12.6%
NTV SVM	176.8	66	0.8	0.7%	11.8%
PE SVM	168.8	33	0.4	2.7%	26.2%
120° shift M^3V	140.3	0.4	0.02	6.1%	31.3%
M^3V	140.9	0.2	0.01	8.2%	37.9%
M^2ZV	141.4	0.8	0.04	5.1%	26.1%
Hybrid SVM	141.0	0.4	0.02	1.8%	19.5%

The simulation is carried out for over modulation region with 10kHz switching frequency. The Fig. 41 shows the output voltage waveforms at linear modulation region (M_i<0.907), OVM-I region (0.907 < M_i ≤0.953) and OVM-II region (0.953< M_i <1). For the simulation purpose, the modulation indices are taken at 3 different regions: M_i = 0.907 (Linear Modulation), 0.953 (OVM-I) and 0.999 (OVM-II).

B. Experimental Results:

The hardware setup is prepared for the 3L NPC MLI with the Sparton-6 XC6SLX9 FPGA is used for the generation of PWM signal as shown in Fig. 42. The experimental results are taken form the experimental setup to validate the simulation results and shown in Fig. 43 and 44. The input parameters for the inverters are given as V_{dc}=200V, C_1=C_2=220µF, f_s=10 kHz and f_o=50Hz. The switching devices in inverter are IGBT modules.

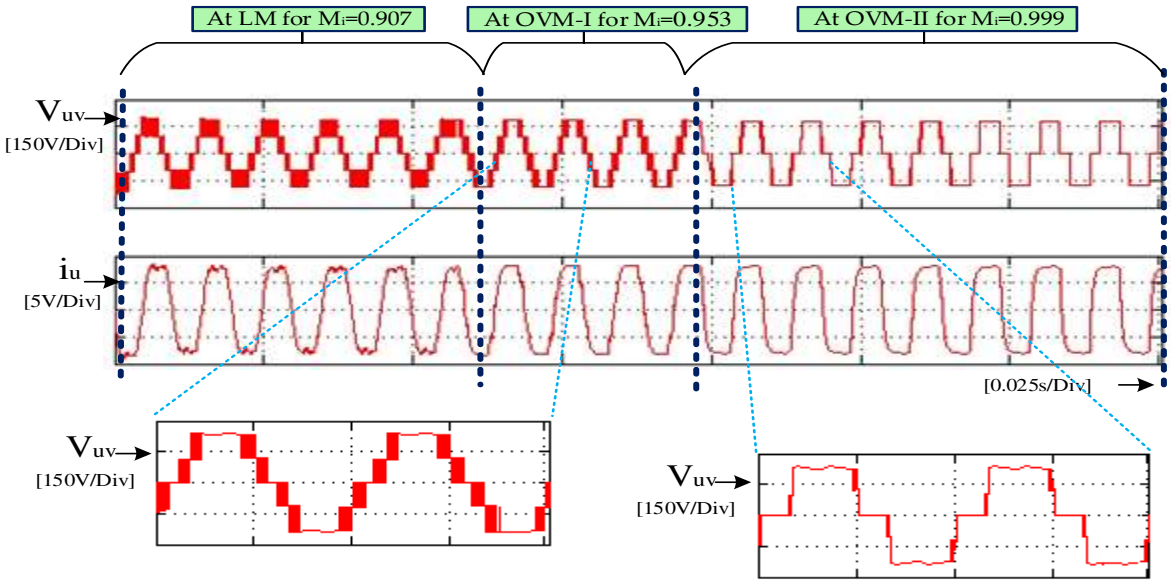

FIGURE 41. Simulation result for entire modulation range for Mi = 0.907 (Linear Modulation), 0.953 (OVM-I) and 0.999 (OVM-II).

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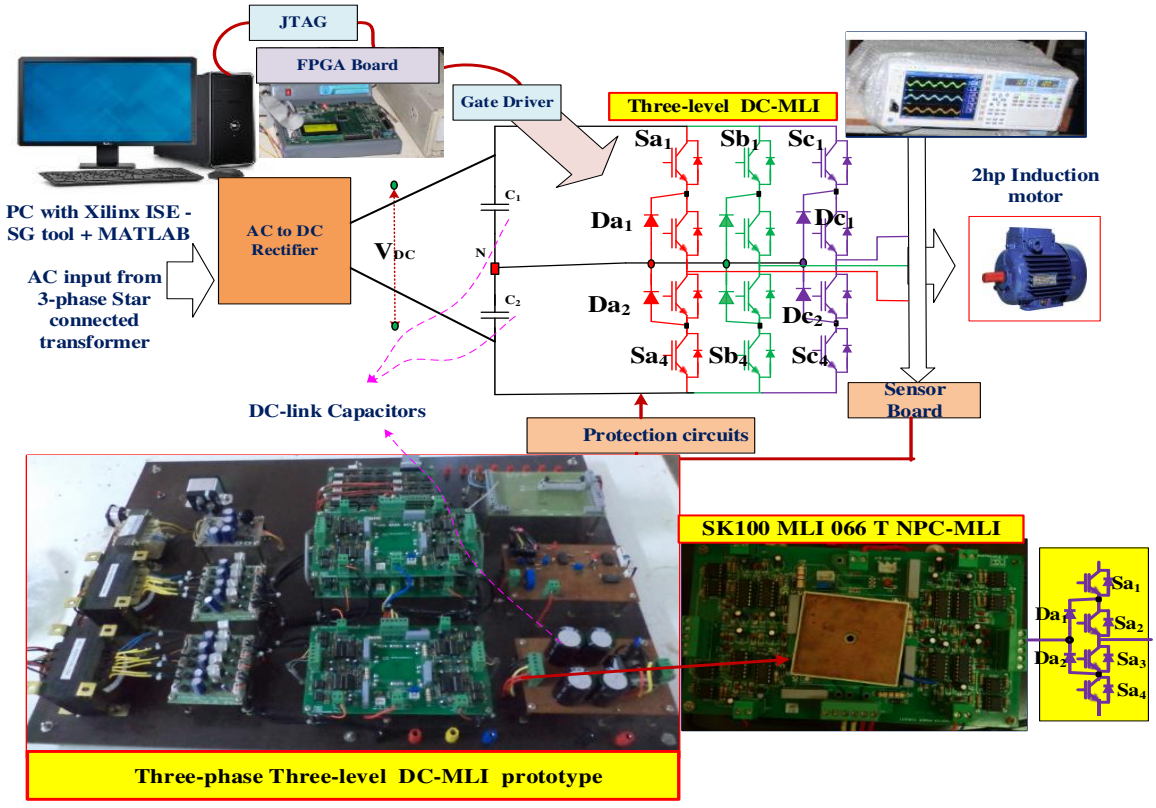

FIGURE 42. Experimental Setup of 3L NPC MLI with Spartan-6 XC6SLX9 FPGA

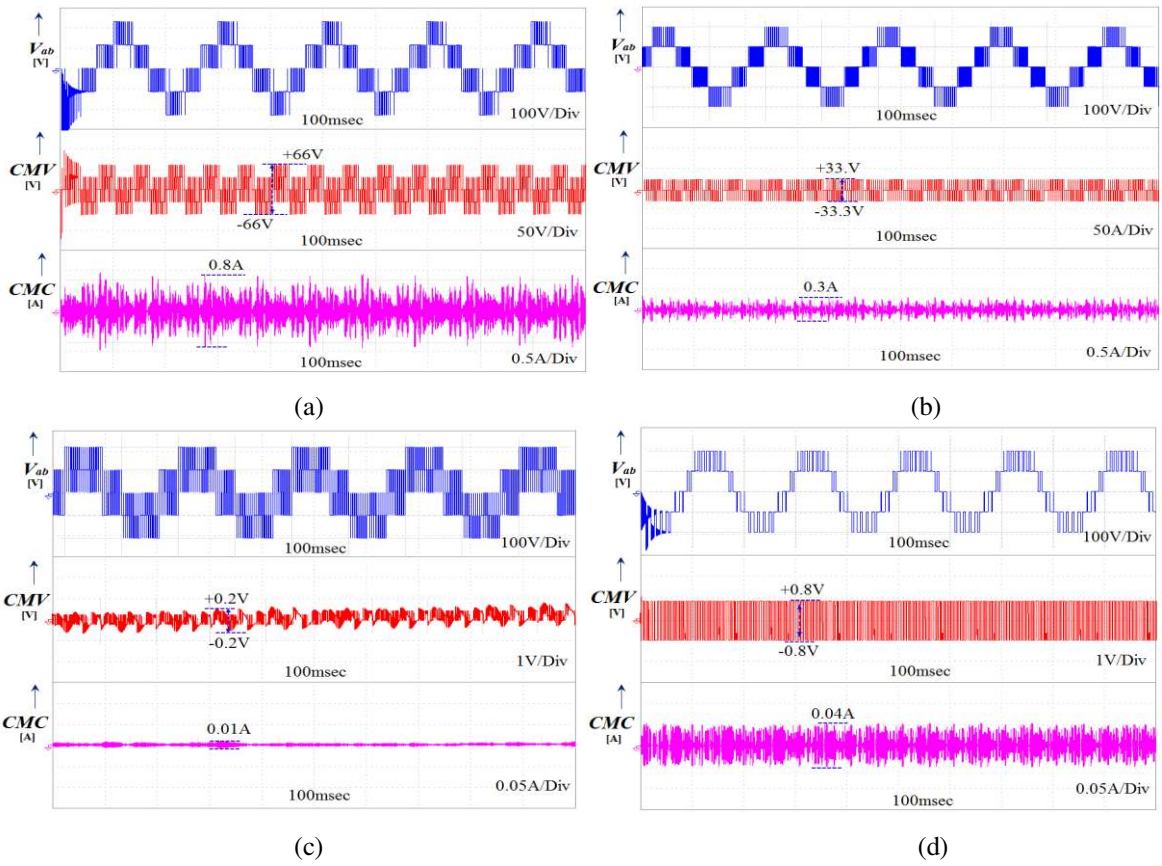

FIGURE 43. Experimentation line-to-line voltage (Vab), CMV, and CMC for (a) NTV SVM(b). PE SVM, (c). M²ZV, (d). M³V

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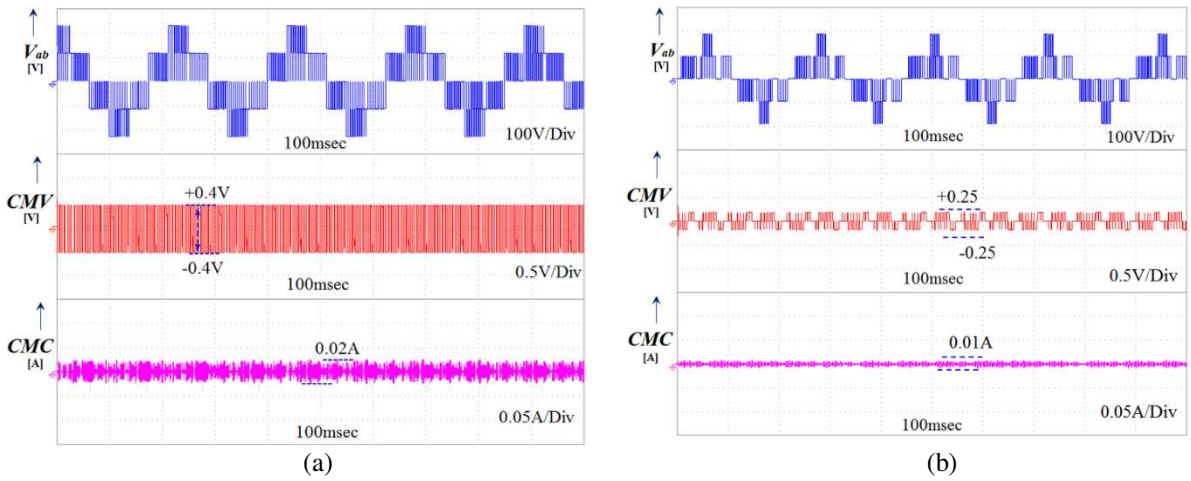

FIGURE 44. Experimentation line-to-line voltage (V_{ab}), CMV, and CMC for M³V+ M²ZV: (a) higher modulation index, (b) lower modulation index

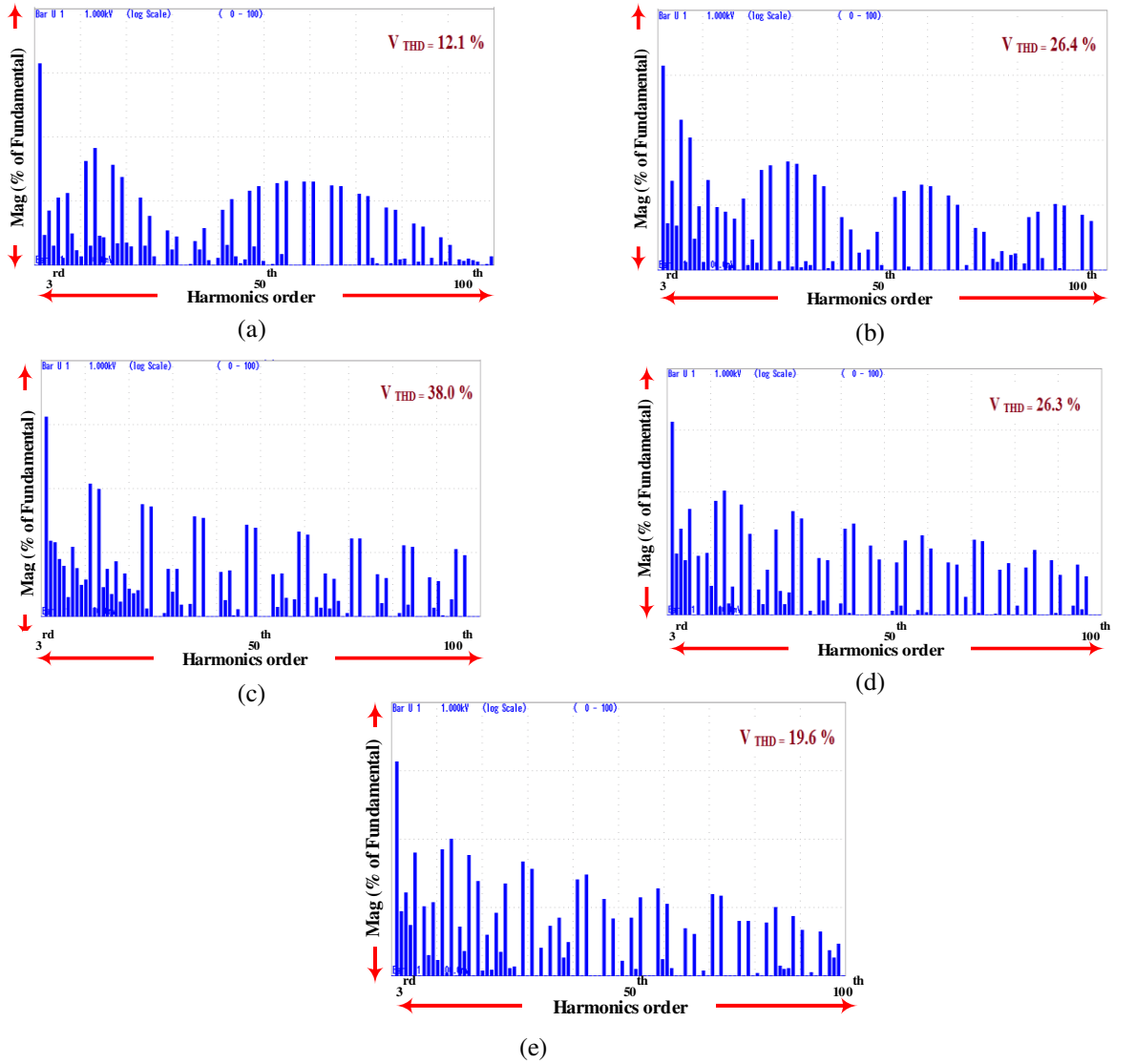

FIGURE 45. Line voltage THD spectrum for (a). NTV SVM, (b).PE SVM, (c).M2ZV, (d).M3V, (e). Hybrid M³V+ M²ZV.

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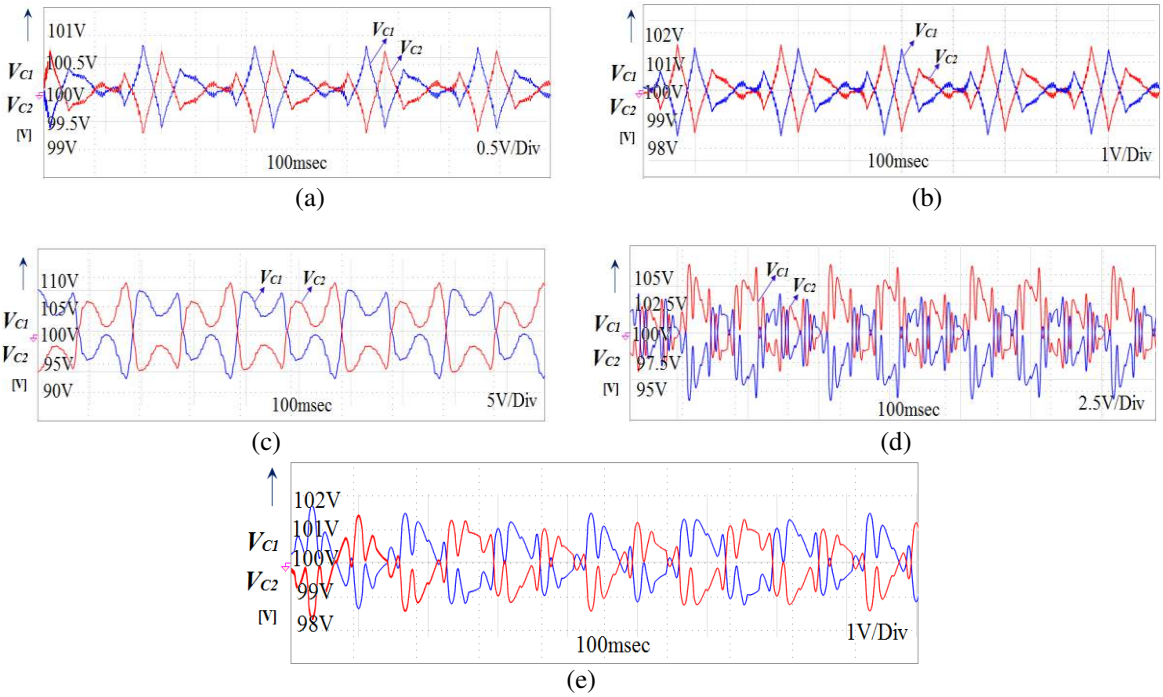


FIGURE 46. DC -link capacitors voltages V_{C1} and V_{C2} for (a). NTV SVM, (b).PE SVM, (c).M²ZV, (d).M³V, (e). hybrid M³V+ M²ZV

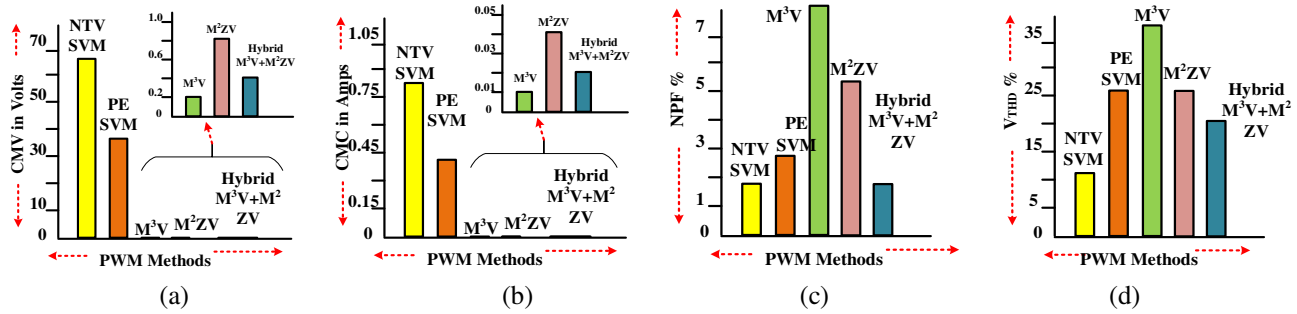
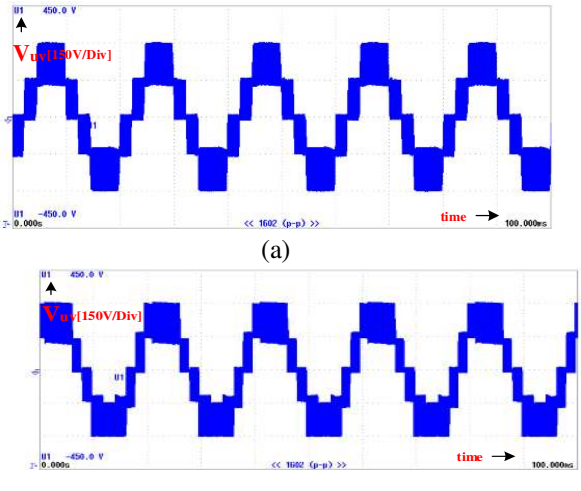


FIGURE 47. Comparison chart of different SVM techniques vs (a) CMV, (b) CMC, (c) NPF%, (d) V_{THD}%

The experimental results of voltage THD for different SVM techniques are shown in Fig. 45. The DC-link capacitor voltages of various SVM techniques are shown in Fig. 46. The comparison chart is drawn between various SVM techniques and CMV, CMC, NPF% and V_{THD}% and it is shown in Fig. 47. Among the various SVM techniques, the NTV SVM method delivers higher line-to-line voltage, lower NPF% and the voltage THD, but the CMV is higher in this method. The neutral pinot fluctuation is very high in the case of M³V SVM. In hybrid M³V+M²ZV the CMV is reduced to minimum value as the NPF% is low while the voltage THD is little higher than NTV SVM among the SVM techniques. The comparison chart is prepared for different SVM techniques with CMV, CMC, NPF% and V_{THD}%.

The simulation results of output voltage for 3L NPC MLI at different modulation indices (M_i= 0.7, 0.9, 0.958 and 0.997) are shown in Fig. 48.



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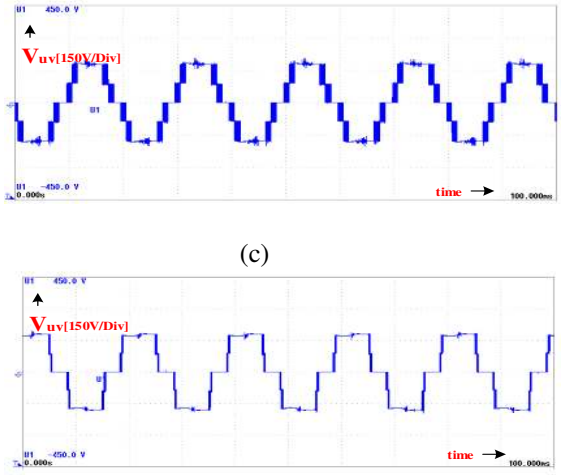

FIGURE 48. Experimental results; Output Voltage (a). M_i =0.7, (b). M_i =0.9, (c). M_i =0.958, (d). M_i =0.997

The Fig. 49 give the idea about the processing time of the FPGA during the step change. It is noted that, the processing time is equal throughout the linear modulation region. In OVM-I, the processing time is high because of the calculation of new duty cycle ratio, while in OVM-II it is less than OVM-I and higher than linear modulation.

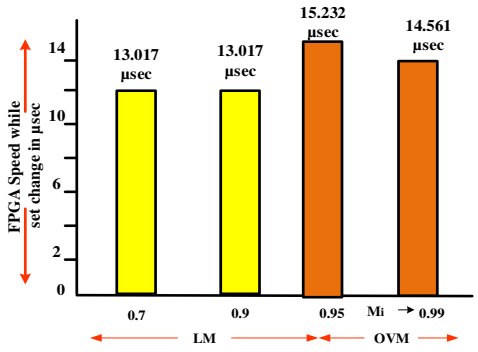

FIGURE 49. FPGA processing time during the step change

IX. OPEN-END WINDING THREE PHASE INVERTER

The open-end winding topology doesn't contain clamping diodes thus the magnitude is reduced to half when compared to conventional 3L inverter [162], [163]. As the supply voltage is reduced, the voltage stress across the power devices is reduced in this topology. In OEW inverter, two 2L inverter fed from their respective source are connected to the motor which generates 3L output. The circuit for the 3-phase OEW topology is shown in Fig. 50.

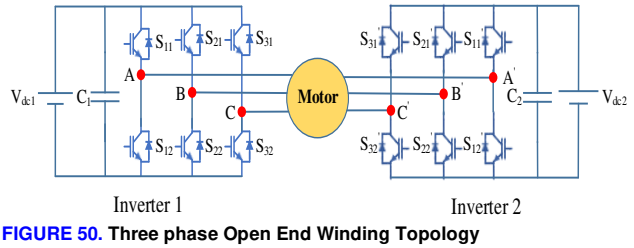

FIGURE 50. Three phase Open End Winding Topology

The DC input voltages of inverter 1 (V_{dc1}) and inverter 2 (V_{dc1}) is considered as $V_{dc}/2$. The pole voltages of inverter 1 is V_{AO}, V_{BO} and V_{CO}, while the pole voltages of inverter 2 is $V_{A'O}$, $V_{B'O}$ and $V_{C'O}$. The voltage across phase windings is given as

$$V_{AA'} = V_{AO} - V_{A'O} \quad (25)$$

$$V_{BB'} = V_{BO} - V_{B'O} \quad (26)$$

$$V_{CC'} = V_{CO} - V_{C'O} \quad (27)$$

The resultant voltage will produce three level voltage at output such as $+V_{dc}/2$, 0 and $-V_{dc}/2$. The resultant space vector for OEW inverter is defined as below [162].

$$V_S = V_{AA'} + V_{BB'}e^{j\frac{2\pi}{3}} + V_{CC'}e^{j\frac{4\pi}{3}} \quad (28)$$

The total switching combination of OEW inverter is 64 which are placed in 19 locations in the space vector diagram which are shown in Fig. 51 (b). The SVM diagram of individual inverters are shown in Fig. 51 (a). The resultant vectors are calculated by adding the two vectors in individual inverters which results in 3L output. [164]-[167].

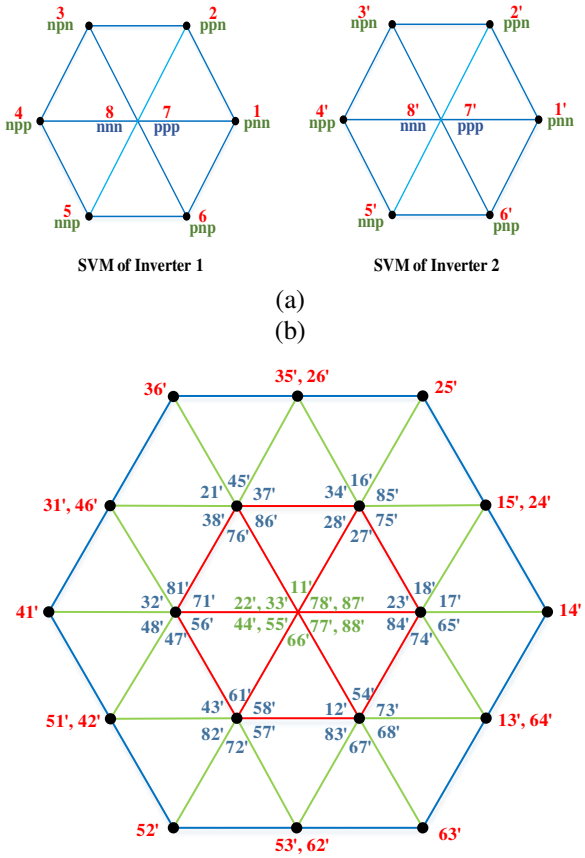

FIGURE 51 (a) SVM Diagram of Inverter 1 and 2, (b) SVM Diagram of OEW Inverter

The vectors combinations that produce zero CMV is listed in Table 24. Out of 64 vectors available, 20 vectors will generate Zero CMV. It is noticed that all the 8 zero vectors and all the 12 medium vectors are producing Zero CMV.

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TABLE 24 Resultant Vectors that produces Zero CMV

Space Vector Combinations	CMV of Inverter 1 (V_{C1})	CMV of Inverter 1 (V_{C2})	Resultant CMV (V_{C1}-V_{C2})
13', 15', 35', 31', 51', 53', 11', 33', 55'	$V_{dc}/6$	$V_{dc}/6$	0
64', 24', 26', 46' 42' 62', 22', 44', 66'	$V_{dc}/3$	$V_{dc}/3$	0
77'	$V_{dc}/2$	$V_{dc}/2$	0
88'	0	0	0

The switching loss of the OEW is less when compared to the conventional inverter. In OEW topology, neutral point is not available in the inverter, so there is no issue of neutral point balancing. The common mode voltage elimination is much easier in the OEW topology on comparing with the conventional NPC inverter as there are two separate sources available in the OEW topology. The OEW topology can be used in high power applications of electrical drives.

X. SIMPLIFICATION OF MLI FROM 2L INVERTERS:

The Space vectors of multilevel inverter can be multiple space vectors of 2L inverters. In [168], it is said that the space vector diagram of 3L can be resolved into 6 two-level inverters. The 3L SVM consists of 6 hexagons which individually represents the space vectors of 2L inverters. This simplification of 3L inverter SVM from 2L inverter SVM is shown in Fig. 52.

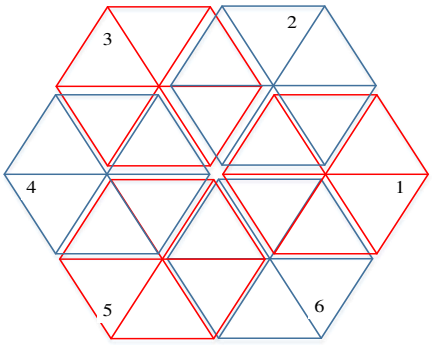

FIGURE 52. Simplification of three-level inverter from two-level inverter

Similar to 3L inverters, the higher-level inverters also can be reduced to 2L inverters. The SVD of four-level inverter is simplified into 2L inverters as shown in Fig. 53. The Four level inverter consists of 12 two-level hexagons in the outer ring and the remaining area is also a 2L hexagon. This each four-level inverter has 13 two-level hexagons.

For a five-level inverter, the outer ring of the SVD consists of 18 two-level inverters and the remaining area has single 3L inverter SVD. Further the 3L inverter is simplified to 6 two-level inverters. As a result, the five-level inverter totally contains 24 two-level inverters. The representation of five level inverter into reduced level is shown in the Fig. 54.

The n-level inverter can be resolved into six [1+ (n-1)/2] level hexagons with the centre of first hexagon lies on 0^0 and the subsequent hexagon has the centre shifted by 60^0 each.

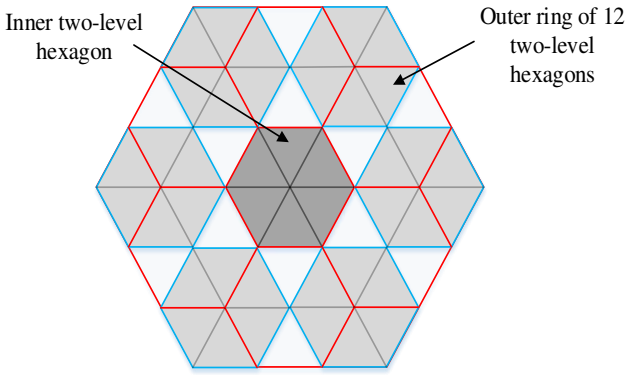

FIGURE 53. SVD of four level inverter is reduced to 2L Inverter

The above conditions suit when the no. of level is odd and greater than 5. The seven-level inverter has 6 [1+ (7-1)/2] = 6 (4) level hexagons, which further reduced to 2L hexagons as 6 x 13 (four level to two level) = 78 two-level hexagons. For nine-level inverter, the SVD is resolved into 6 five-level inverter as described above and it has 6 x 24 = 144 two-level hexagons [168]-[169]. The number of 2L hexagons available in multilevel inverter is calculated and given in Table 25.

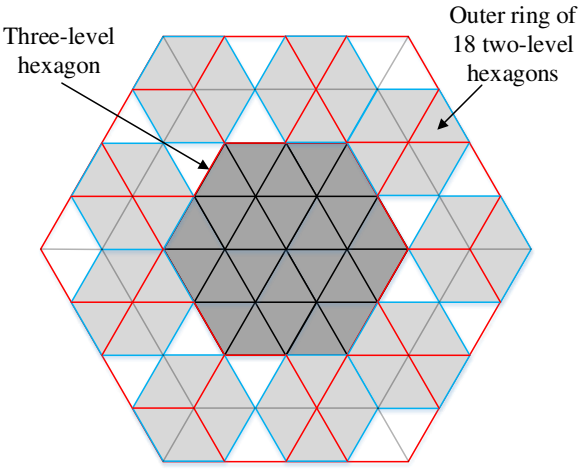

FIGURE 54. SVD of Five level inverter is reduced to lower-level inverter

The space vector representation of higher levels (greater than 3L) and their voltage balancing strategies are discussed in [170]-[176]. The following sections discusses about the SVM techniques and the Open-End Winding topology for Five Phase Inverters.

XI. FIVE PHASE INVERTER:

Though the 3-phase multi-level inverter is ruling the industrial application. The multi-phase motor drives started gaining attraction as they have many advantages like reduced switching losses, lower common mode voltage, lower harmonic contents and optimum DC-link voltage. The voltage stress across power switching devices is reduced in multiphase inverter as the voltage is shared across each phase. The MCPWM techniques for 5-phase inverter will be similar to 3 phase inverter which is discussed in section II. This section discusses about the SVM techniques for 2L and 3L inverters of 5-phase drives [177], [178].

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TABLE 25 Comparison No of 2L hexagons for various multilevel inverters

	3 level	4 level	5 level	6 level	7 level	9 level	11 level
Six [1+ (n-1)/2] (When n > 5, n is odd)	-	-	-	-	6 [4 level]	6 [5 level]	6 [6 level]
No of two-level hexagons	6	13	24	37	6*13 = 78	6*24 = 144	6*37 = 222

A. Five Phase Two Level Inverter:

The 5-phase 2L inverter circuit diagram is shown in Fig. 55. Like 3-phase 2L inverter, the 5-phase 2L inverter also consists of two switches in each leg which are complement to each other [178]-[180].

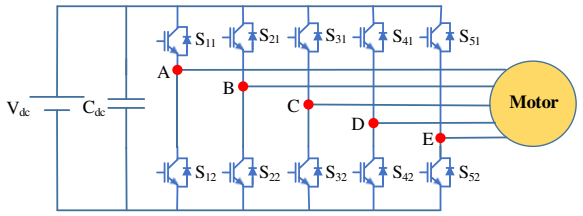

FIGURE 55. Five Phase Two level inverter

The SVM Technique of 2L inverter has 32 vectors (2^5), out of which 2 vectors are zero vectors and the remaining 30 vectors are active vectors (10 large, 10 medium and 10 small vectors) that are placed in d-q plane and the x-y plane. The space vector representation of 5-phase 2L inverter is shown in Fig. 56 for d-q plane and the x-y plane. The switching vectors are placed in 10 sectors in a decagonal shape and their phase voltage is expressed as

$$\begin{bmatrix} V_{dq} \\ V_{xy} \end{bmatrix} = \frac{2}{5}\begin{bmatrix} 1 & a & a^2 & a^3 & a^4 \\ 1 & a^3 & a & a^4 & a^2 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \\ V_d \\ V_e \end{bmatrix} \quad (29)$$

where $a = e^{\frac{j2\pi}{5}}$

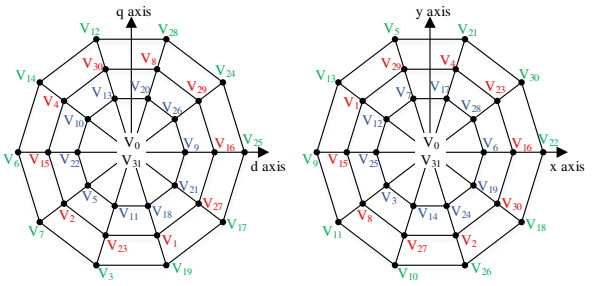

Figure 56. Space Vectors of Five phase two level inverter at α-β plane and x-y plane.

The magnitude of small, medium and large vectors is calculated by the following equation and their values are 0.2472 V_d, 0.4 V_d and 0.6472 V_d respectively.

$$\left|V_s = \frac{4}{5}\cos\left(\frac{2\pi}{5}\right)V_d\right| \quad (30)$$

$$\left|V_m = \frac{2}{5}V_d\right| \quad (31)$$

$$\left|V_l = \frac{4}{5}\cos\left(\frac{\pi}{5}\right)V_d\right| \quad (32)$$

The time for each vector in large vector is calculated by the following equation

$$t_a = \frac{|V_{ref}|\sin\left(\frac{s\pi}{5}-\alpha\right)}{|V_l|\sin\left(\frac{\pi}{5}\right)}t_s \quad (33)$$

$$t_b = \frac{|V_{ref}|\sin\left(\alpha-\frac{(s-1)\pi}{5}\right)}{|V_l|\sin\left(\frac{\pi}{5}\right)}t_s \quad (34)$$

$$t_o = t_s - t_a - t_b \quad (35)$$

where t_s is the sampling time, V_{ref} is the reference voltage, V_l is large vector voltage, s is sector number in which the reference voltage is present and α is the angle difference between reference vector and large vector. The same equation can also be used to calculate the time duration for small and medium vectors by replacing the large vector. The common mode current and it is calculated by

$$i_g = i_a + i_b + i_c + i_d + i_e = 5i_o = C_g\frac{dv_g}{dt} \quad (36)$$

The High frequency model of 5-phase inverter motor drive is shown in Fig. 57. The common mode model and differential mode model for 5-phase load is shown in Fig. 58. (a) and (b), where l_o, R_o and C_{wo} are the zero-sequence component of L, R and C respectively, while l_q, R_q and C_{wq} are the q-axis component of L, R and C respectively. The d-axis model will be same as the q-axis model in differential mode model [181]-[183].

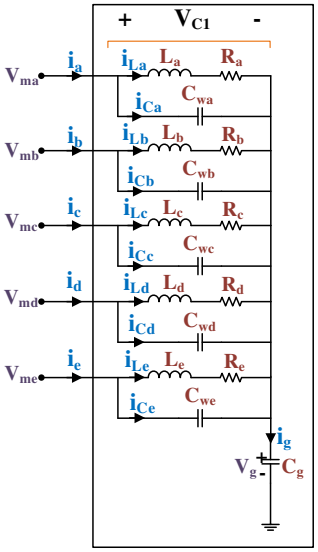

FIGURE 57. High Frequency model of 5 phase inverter

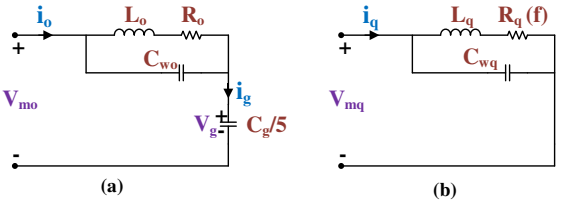

FIGURE 58. (a) Common Mode model of a 5-phase load, (b) Differential Mode model of a 5-phase load

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The admittance transfer function for common mode model (Y_o) and differential mode model ($Y_q = Y_d$) is given as

$$Y_o = \frac{i_o}{v_o} = \frac{sC_gL_oC_{wo}\left[s^2+s\frac{R_o}{L_o}+\frac{1}{L_oC_{wo}}\right]}{L_o(C_g+5C_{wo})\left[s^2+s\frac{R_o}{L_o}+\frac{5}{L_o(C_g+5C_{wo})}\right]} \quad (37)$$

$$Y_d = Y_q = \frac{i_q}{v_q} = \frac{C_{wq}\left[s^2+s\frac{R_q(f)}{L_q}+\frac{1}{L_qC_{wq}}\right]}{L_q\left[s+\frac{R_q(f)}{L_q}\right]} \quad (38)$$

The common mode voltage for 5-phase inverter is given as

$$V_{cm} = \frac{1}{5}(V_{ao} + V_{bo} + V_{co} + V_{do} + V_{eo}) \quad (39)$$

where V_{ao}, V_{bo}, V_{co}, V_{do} and V_{eo} are the pole voltages of phase A, B, C, D and E. The CMV of 5-phase 2L inverter in d-q plane is calculated and listed in the Table 26.

Table 26. CMV of Five Phase Two Level Inverter in d-q Plane

Vectors	Type of Vectors	CMV
ppppp (V_0), nnnnn (V_{31})	Zero	$\pm V_{dc}/2$
npnnp (V_9), pnppn (V_{22}), ppnpn (V_{26}), nnpnp (V_5), npnpn (V_{10}), pnpnp (V_{21}), pnpnn (V_{20}), npnpp (V_{11}), nppnp (V_{13}), pnnpn (V_{18})	Small	$\pm V_{dc}/10$
nnpnn (V_4), ppnpp (V_{27}), pppnp (V_{29}), nnnpn (V_2), pnnnn (V_{16}), npppp (V_{15}), npnnn (V_8), ppppn (V_{30}), pnppp (V_{23}), nnnnp (V_1)	Medium	$\pm 3V_{dc}/10$
ppnnp (V_{25}), nnppn (V_6), ppnnn (V_{24}), nnppp (V_7), npppn (V_{14}), pnnnp (V_{17}), pppnn (V_{28}), nppnn (V_{12}), nnnpp (V_3), pnnpp (V_{19})	Large	$\pm V_{dc}/10$

It can be seen that the maximum CMV of 2L inverter is $\pm V_{dc}/2$. The CMV in x-y plane for zero ($\pm V_{dc}/2$), small ($\pm V_{dc}/10$), medium ($\pm 3V_{dc}/10$) and large ($\pm V_{dc}/10$) vectors will be same as in d-q plane.

B. Five Phase Three Level Inverter:

The circuit diagram for 5-phase 3L inverter is shown in Fig. 59. and the possible switching states are 243 (3^5) vectors. Among these 243 vectors, many redundant states are present.

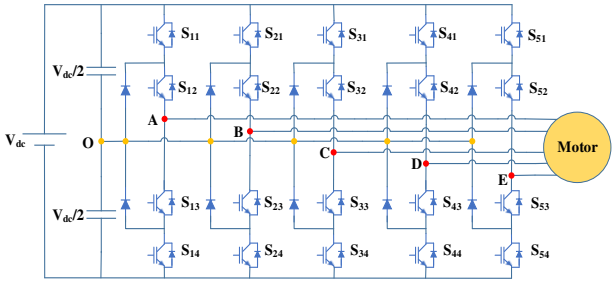

FIGURE 59. Five Phase Three Level Inverter

The vector representation for the 5-phase 3L inverter is given in d-q plane and the x-y plane. The space vector diagram of the 5-phase 3L inverter with 243 vectors in d-q frame is shown in Fig. 61. The vectors which are along the decagonal axis is called as vertex vectors and the vectors which are present at the axis that is formed between two decagonal axis is called as non-vertex vectors. The sector I representation of the 243 vectors are shown in Fig. 60.

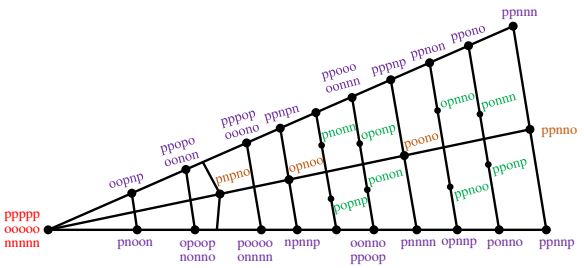

FIGURE 60. Sector I representation of five phase three level inverter in d-q frame

The Magnitude of the vertex vectors are 0.076 V_d, 0.124 V_d, 0.2 V_d, 0.247 V_d, 0.324 V_d, 0.4 V_d, 0.447 V_d, 0.524 V_d and 0.647 V_d respectively, while the magnitude of the non-vertex vectors are 0.145 V_d, 0.235 V_d, 0.38 V_d and 0.615 V_d respectively [184]-[187].

The CMV of 5-phase 3L inverter is calculated and it is noted that the CMV is reduced from $\pm V_{dc}/2$ to $\pm 3V_{dc}/10$ for vertex vector and reduced to Zero for non-vertex vector. The CMV obtained for different types of vectors for 3L inverter are given in Table 27.

Table 27. CMV of Five Phase Three Level Inverter

Type of Vector	Type of Vectors	CMV	Type of Vector	Type of Vectors	CMV
Vertex Vector	Zero	$\pm V_{dc}/2$	Non-Vertex Vector	Zero	0
	Small	$\pm V_{dc}/10$		Small	0
	Medium	$\pm 3V_{dc}/10$		Medium	0
	Large	$\pm V_{dc}/10$		Large	0

The 243 vector which are available in 5-phase 3L inverter is not used completely due to inequality relationship between 5-phase voltages. Therefore, 113 eligible vectors have been chosen from the available 243 vectors and it is named as Optimized Five Vectors These 113 vectors are selected so as to generate the desired voltage reference at main subspace (d-q subspace) and to make the average voltage as zero in auxiliary subspace (x-y subspace). The redundant vectors that are present in SVM are responsible for the balancing of DC-link capacitor voltages during unbalanced condition. The OFV representation of sector I for 5-phase 3L inverter is shown in Fig. 62.

The OFV will have 21 vectors in sector I as compared to 39 vectors in actual 5-level space vector. The potential switching sequences of 5-phase 3L inverter in sector I is given in Table 28. Out of 16 potential switching sequence, 10 switching sequence (A1-K1) can be used as it generates the desired voltage reference at d-q sub-space by eliminating the x-y voltage vectors. The remaining switching sequence (11-16) are not able to nullify the x-y voltage vectors. So, only 10 vector switching sequence are utilized for OFV which assures the minimum number of transitions that reduces the switching losses.

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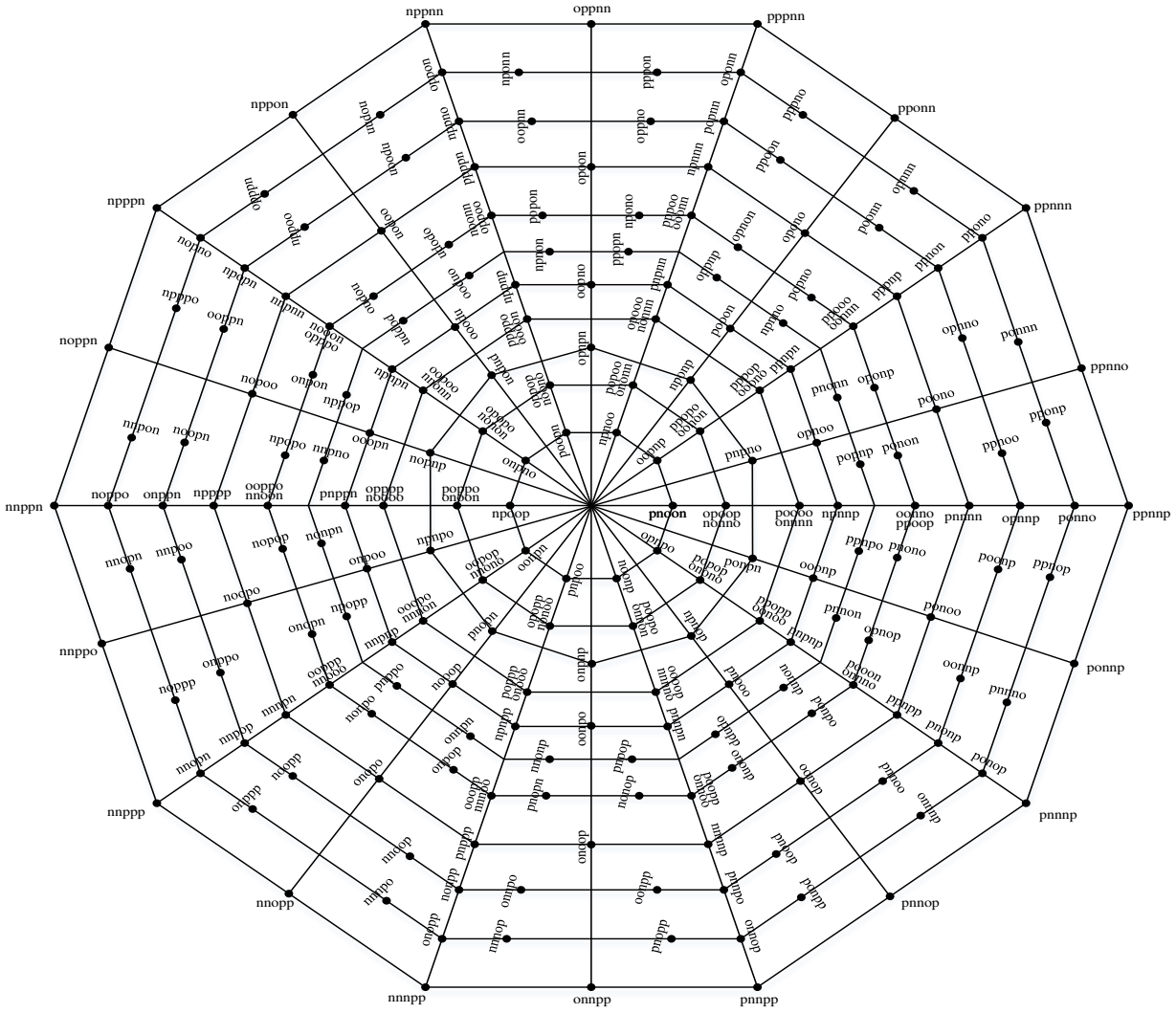

FIGURE 61. Space Vector Modulation diagram of five phase three level inverter in d-q frame

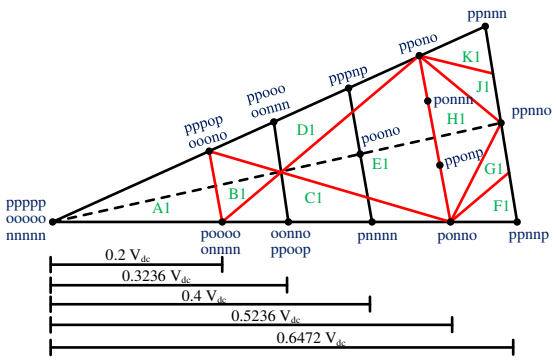

FIGURE 62. Sector I representation of OFV in d-q frame

Table 28. Potential Switching Sequence in Sector I

Sub Region	Switching Sequence
1 (A1)	oonno-ooono-ooooo-poooo-ppooo-ppoop
2 (B1)	oonno-ooono-poono-poooo-ppooo-ppoop
3 (C1)	oonno-ponno-poono-poooo-ppooo-ppoop
4 (D1)	oonno-ponno-poono-ppono-ppooo-ppoop
5 (E1)	oonno-ooono-poono-ppono-ppooo-ppoop
6 (F1)	oonno-ponno-ppnno-ppnnp-pponp-ppoop
7 (G1)	oonno-ponno-ppnno-ppono-pponp-ppoop
8 (H1)	oonno-ponno-ppnno-ppono-ppooo-ppoop
9 (J1)	oonnn-ponnn-ponno-ppnno-ppono-ppoop
10 (K1)	oonnn-ponnn-ppnnn-ppnno-ppono-ppoop
11	oonno-ponno-poono-ppono-pponp-ppoop
12	oonnn-ponnn-ponno-poono-ppono-ppooo
13	onnnn-oonnn-ponnn-ponno-poono-poooo
14	oonno-ooono-poono-ppono-pponp-ppoop
15	onnnn-pnnnn-ponnn-ponno-poono-poooo
16	ooono-poono-ppono-pponp-pppnp-pppop

The dwell time ratio is important for eliminating the x-y space vector component. The volt-sec equation of resultant vector is given as

$$T_s\overrightarrow{V_{dq\,ref}} = T_o\overrightarrow{V_o} + T_1\overrightarrow{V_1} + T_2\overrightarrow{V_2} + T_3\overrightarrow{V_3} + T_4\overrightarrow{V_4} \quad (40)$$

$$T_s\overrightarrow{V_{xy\,ref}} = T_o\overrightarrow{V_o} + T_1\overrightarrow{V_1} + T_2\overrightarrow{V_2} + T_3\overrightarrow{V_3} + T_4\overrightarrow{V_4} = 0 \quad (41)$$

$$T_s = T_o + T_1 + T_2 + T_3 + T_4 \quad (42)$$

where, T_o, T_1, T_2, T_3 and T_4 are the dwell time of switching vectors $\overrightarrow{V_o}$, $\overrightarrow{V_1}$, $\overrightarrow{V_2}$, $\overrightarrow{V_3}$ and $\overrightarrow{V_4}$ of the selected switching sequence, T_s is the switching period, $\overrightarrow{V_{dq\,ref}}$ and $\overrightarrow{V_{xy\,ref}}$ are the reference output voltage in d-q and x-y space.

$$\begin{bmatrix} T_0 \\ T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \begin{bmatrix} V_{d0} & V_{d1} & V_{d2} & V_{d3} & V_{d4} \\ V_{q0} & V_{q1} & V_{q2} & V_{q3} & V_{q4} \\ V_{x0} & V_{x1} & V_{x2} & V_{x3} & V_{x4} \\ V_{y0} & V_{y1} & V_{y2} & V_{y3} & V_{y4} \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V_d \\ V_q \\ V_x \\ V_y \\ T_s \end{bmatrix} \quad (43)$$

In [189]-[191] the number of vectors has been further reduced to 51 vectors. These 51 vectors are selected such that all these vectors will produce zero CMV. The space vector diagram of vectors that give zero CMV is shown in Fig. 63. and the corresponding vectors are listed in the Table 29.

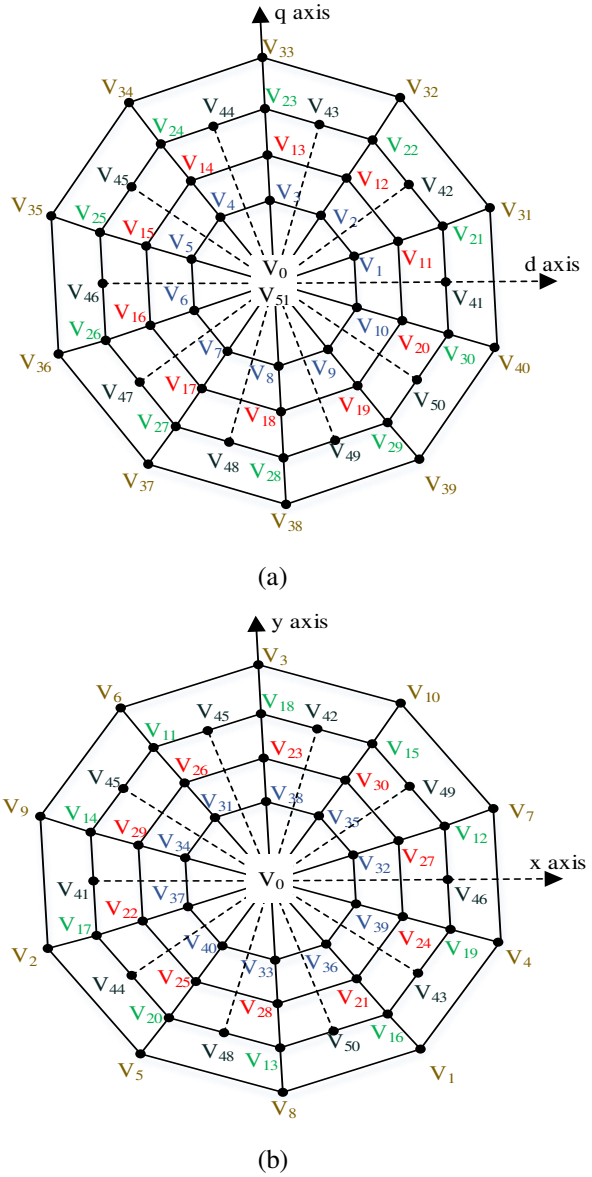

FIGURE 63. Space Vector diagram of five phase three level inverter with zero CMV in (a) d-q frame (b) x-y frame.

Table 29. Vectors of five phase 3L inverter with zero CMV

Vector number	Switching State	Vector number	Switching State	Vector number	Switching State
V0	ooooo	V17	nopnp	V34	pnooo
V1	pnpno	V18	ooopn	V35	oonop
V2	opnoo	V19	nopoo	V36	pnnop
V3	poono	V20	noppn	V37	ponpn
V4	ppnno	V21	npnpo	V38	ooonp
V5	nponp	V22	onpoo	V39	ponoo
V6	pooon	V23	noopo	V40	ponnp
V7	opono	V24	nnppo	V41	opnnp
V8	pponn	V25	pnopn	V42	ppnon
V9	opnpn	V26	nooop	V43	popnn
V10	oopno	V27	onopo	V44	nppno
V11	opoon	V28	nnopp	V45	npopn
V12	oppnn	V29	onpnp	V46	onppn
V13	pnpon	V30	oonpo	V47	nnpop
V14	npooo	V31	onoop	V48	nonpp
V15	oopon	V32	onnpp	V49	pnnpo
V16	nppon	V33	npnop	V50	pnonp

Many researches have been done by the researchers in 5-phase NPC MLI for the elimination of CMV using SVM PWM techniques. The research has been categorized in the following Table 30.

Table 30. SVM Techniques for Five phase NPC MLI

Reference	Types of SVM	Inferences
[156]	SVM with 243 vectors is reduced to 113 vectors	The available 243 vectors of 5 phase 3 level inverter are developed and the switching vectors are reduced to 113 vectors (OFV) by eliminating the undesired switching states. By using the OFV vectors, the switching combination is reduced so that the complexity is reduced for a certain level. The switching states are selected so as that x-y vector produces the zero-average voltage.
[157]	SVM with 113 vectors	The comparative analysis between the carrier based PWM with the apace vector PWM has been done in this paper. The SVM is done for 113 vectors. The time taken for finding the vector and complexity of implementation is measured in this paper.
[178] [191]	SVM for 2 L inverter	The SVM switching states for 2 L inverter has been generated for d-q space and x-y space. The performance analyzes of two inverter SVM has been done for the 5-phase inverter. The mathematical analyze also made for 2L SVM. In 2L inverter, the vector in the outer decagon (large vector) of the d-q subspace is mapped at inner decagon (Small vector) of the x-y subspace, while the middle decagon (medium vector) will remain in the same decagon for both d-q and x-y subspace.
[184]	SVM with 243 vectors is reduced to 113 vectors	This paper also deals with the OFV vectors. The dwell time calculation and the mapping of switching states has been explained for 2L and 3L inverters. The reference vectors are identified with the help of signum function.
[187],	SVM with	The switching vector has been further

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[188]	51 vectors and Carrier based PWM	reduced to 51 vectors from 113 vectors. These 51 vectors will generate zero CMV. So, the resultant output will be free from CMV. The comparative analyzes between 5-phase 2L and 3L inverter is done in these papers.
[189], [190]	SVM for OEW Inverter	These papers discussed about the Open-End Winding Inverters. The SVM technique has been used to generate the pulse for the inverter. The 51-switching vector that eliminates the CMV has been selected for this inverter.
[193], [194]	SVM with 31 vectors	This paper deals with the reduction of CMV in the 5-phase 3L NPC MLI. The 51 switching vectors will have zero CMV, from these 51 vectors only 31 vectors are selected which restricts the x-y components.
[198]	SVM Decomposition method	The Open-End Winding drive is used in this paper and the 3L SVM is generated by decomposition method. The 3L SVM is developed by combining several 2L SVM which is called as decomposition method.

C. Open End Winding Five phase inverter:

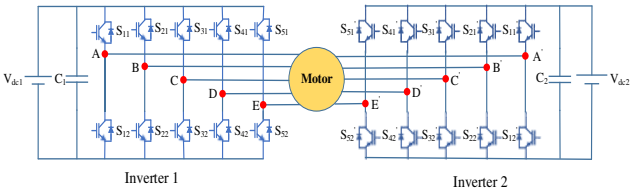

FIGURE 64. Five phase Open End Winding Topology

Fig. 64. represents the open-end winding structure of 5-phase 2L VSIs. In OEW, two inverters on either side of the 5-phase motor are connected with separate dc source as input [192]-[197]. The legs of inverter 1 are denoted as A, B, C, D and E, while the inverter 2 legs are denoted as A', B', C', D' and E' in the OEW inverter topology.

This topology has 211 space vectors with 1024 possible switching states. As the number of switching state is more, there will be a complexity in selecting the proper switching states. This complexity can be reduced by decomposing the 3L decagons into 2L decagons [198-199]. The decomposed space vector diagram of d-q subspace for 5-phase 3L inverter is shown in Fig. 65.

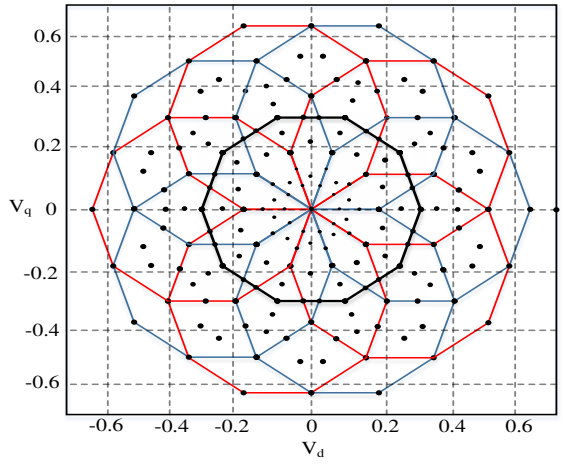

FIGURE 65. Decomposition of 3L into 2L inverter

XII. FUTURE TRENDS AND RESEARCH DIRECTIONS:

A. Literature work:

The 3L NPC inverter has been discussed throughout this paper. The multi-carrier PWM techniques are used at initial stages. Among the various MC PWM techniques like PO, POD, APOD, IC PWM, PSC PWM and VFC PWM techniques, the IC PWM techniques gives better output voltage but THD% is higher which is a drawback [29] – [33]. The output voltage of other PWM techniques is very closer to each other, but the PO technique provides better THD % value. Likewise, the MC PWM technique doesn't provide both higher output voltage and better THD% [213].

To overcome this issue, the SVM is introduced which provides better THD% along with higher output voltage than the MC PWM techniques. The reason behind this advantage is SVM are capable of controlling the switching states which is not possible in MC PWM techniques [34] – [38]. The CMV is controlled by eliminating some of the vectors which produces CMV. The utilization of one zero vector "ooo" and medium vector for generating the switching sequence will completely eliminate the CMV [86] – [94]. The partial elimination of CMV also possible with modification of SVM techniques. The other issue that is available in MLI is balancing of DC-link capacitor voltages. This balancing can be done with few changes in SVM techniques like comparison of DC-link voltages at each switching states and giving the pulses accordingly [87] – [93].

The Virtual SVM techniques is also introduced to rectify the DC-link voltage balancing [139] – [142]. In VSVM, the medium vectors are eliminated which are responsible for neutral point fluctuation. All the SVM techniques and their modifications are done in 2D plane. As an advancement of 2D SVM, the SVM is developed in the 3D plane. This 3D SVM is introduced for both three-leg and four-leg topology. In three-leg topology, the SVM diagram is of cubical structure [146] – [148]. In four-leg topology, the SVM diagram will have multiple hexagonal layers [149] – [153]. As the redundant vectors are not available in 3D SVM technique, the switching losses are considerably reduced. Also, the efficiency is increased on comparing with 2D SVM. But, the disadvantages in 3D is its complex structure and computation.

In renewable energy application like PV, the dc input voltages are asymmetrical for the inverter, there comes a challenge to operate the inverter by providing suitable pulses to the switches [154], [155]. The issues from asymmetrical dc sources can be resolved by altering the time duration in volt-sec equation of each vector. As the time duration is changed, SVM generates the pulses for corresponding time duration which controls the inverter in asymmetric dc source condition [156], [157]. In NPC MLI, the modulation index less than 0.907 is considered as linear modulation region that are mostly in practice which is as discussed above. In this region, only hexagonal trajectory path is considered. But, when the modulation index greater than 0.907, both circular and hexagonal trajectory path is considered. This region is called as over modulation region

[158], [159]. In OVM region, the Partial Elimination and Full Elimination of CMV can be done as studied in [160], [161].

The OEW topology is introduced to overcome the DC-link balancing issues that are noticed in conventional NPC MLI. In this topology, the load is connected to two inverters with separate DC sources. As the sources are separate, only one capacitor is available in parallel to dc source where there is no opportunity for the DC-link balancing to occur. Also, the voltage stress across switches is reduced since dc source is reduced to half of the voltage used in conventional NPC MLI [162] – [167].

The multi-phase inverters are gaining interest in recent researches as they have lesser CMV, switching loss and harmonic content than the conventional 3-phase inverters [177], [178]. The DC-link voltage is also at its best range. This leads to the development of 5-phase inverters. The SVM techniques for controlling the 5-phase inverters are developed. The CMV reduction can be done for 5-phase 3L NPC MLI by reducing the switching states [156], [157], [184] – [188]. The OEW topology of 5-phase inverter is studied in [192] – [197].

B. Challenges in Multi-level PWM techniques:

- The CMV and DC-link balancing is the important issue reported in the MLIs. Many research has been made to address this problem. Nevertheless, it is difficult to solve both the issue at the same time using SVM techniques. Particularly achieving zero CMV with capacitor balance is not possible. This is because, the medium vectors which has zero common mode voltage is the responsible for the increase in DC-link balancing issue.
- The applications such as PV and battery supplied inverters are supplied by asymmetrical DC source. Hence, the conditional or any selected vector schemes are fail to attain desired output. Hence, the SVM duty cycle has to be modified by adding or subtracting the minimum offset time to change the SVM as operated in normal condition. This leads to more mathematical and implementation complexities.
- The implementation of SVM in over modulation region is complex as it needs to perform switching operation beyond the circular trajectory path. Also, implementing the OVM in application such as FOC, DTC and vector control involves additional mathematical burden and it needs higher end digital controllers.
- In open-end winding topology, the SVM of dual two level inverters has to be combined to perform the three level operation. This leads to the increase in computational process of the SVM. Further, elimination zero CMV is more complex.
- In high power applications, the usage of lower-level inverter will suffer from high voltage stress across each switch which leads to the increased switching and conduction losses. To reduce voltage stress, the rating of components to be high like large capacitor, high current switches which leads to increase in space and cost. Thus, it is not preferred to use lower-level inverters.
- The high-level inverters are preferred for high-power applications such as HVDC and FACTS where the voltage stress is reduced with less components rating. But the NPC MLI has DC-link balancing issues as the number of DC-link capacitor increases. Therefore, the Cascaded H-Bridge inverter is preferred in high-level inverters. All the PWM techniques will be similar in NPC, Cascaded H-Bridge and Flying Capacitor inverter.[225]-[229]
- The number of switches, diodes and capacitors are increased in high-level inverters. As a result, the switching stress, CMV and EMI has been reduced. Though the high-level inverter has such advantages, the calculation is very complex for SVM techniques as the level increases. For example, in three phase applications the nine-level inverter has 729 (9^3) switching combinations which increases the complexity of implementation.
- Preforming the pulse generation in voltage ride through (change in voltage due to fault) condition is difficult. The voltage has to be same throughout the pulse generation process, if the voltage is changed in between then the generated pulse will not be able to give better performances.
- The protection circuit for high power applications is large and heat sink has to be designed to tolerate the thermal effect in the switches. The processing time of the high-level MLI is high and it requires more memory to compute the pulses.

C. Motivation:

To meet-out the power demands in driving multiple loads with reduced cost and size, an optimal solution is given in the form of multi-machine system. This multi-machine system has multiple loads connected to single inverter. For driving many loads, individual inverter is used in the conventional methods which increases the cost, size and the controlling scheme. To overcome this the multi-machine system is introduced. This topology is designed to control multiple motors with the help of single inverter. The multi-motor drive can be employed in industrial application where high performance is required. [200]. The important application of multi-motor drive is Electrical Vehicle in which more than one motor is used. The main advantage of this topology is reduced number of components when compared to conventional Voltage Source Inverter. The operation of multiple motors is done by two topologies for three phase two level inverter.

- Five Leg Inverter [201-203]
- Nine Switch Inverter [204-208]

In five Leg Inverter, the first two leg will be given to one motor and the last two legs will be given to other

motor, while the third leg will be connected to both motors in common. This topology consists of 10 switches to control the two motors. In Nine Switch Inverter, only three legs are used where each leg consists of three switches. The top and middle switches are responsible to give pulse to upper motor while the middle and bottom switches are responsible to give pulse to the lower motor. A comparative analysis for five-leg inverter and nine-switch inverter is done in [209]. The research is further developed for 5-phase motor. The individual control of two 5-phase motor is done by Fifteen Switch Inverter topology [210]. This topology is similar to the Nine Switch Inverter topology for 3-phase loads. This, Fifteen Switch Inverter topology contains 3 switches in each leg which produces 2L output for each motor. The 3L inverter for controlling 3-phase load is developed and their performances are observed in [211]. The bearing current is eliminated by introducing the Fourth-Arm technique in [214] which may be considered for 5-phase inverters. The 3-phase transformer-less NPC MLI is designed for the grid connected PV applications in [215].

D. Future Trends:

The research on 5-phase NPC MLI can be extended as follows:

- Modern Predictive Control can be applied for 5-phase NPC MLI to reduce the CMV and DC-link voltage balancing.
- In PV applications, the SVM technique for asymmetrical DC source NPC MLI can be studied.
- Based on Five Leg Inverter topology in 3-phase inverter, a Nine Leg Inverter topology where 5th leg is common to both motors can be developed for controlling two motors.
- Similar to Fifteen Switch Inverter topology in 3-phase inverter, a Twenty-Five Switch Inverter topology can be developed for controlling two 5-phase motors with 3L output.
- Transformer-less 5-phase NPC MLI can be developed for renewable energy applications like PV, Wind, etc.,
- In future the Artificial Intelligence (AI) can be introduced to reduce the processing time and memory issues

XIII. CONCLUSION:

This paper provides a brief discussion on different carrier based PWM techniques and SVM techniques for 3-phase and 5-phase NPC inverter. The simulation is carried out for all MC PWM techniques and NTV SVM techniques and it is noticed that the NTV SVM provides the better output voltage as well as reduced CMV and NPF. Thus, the SVM techniques are elaborated in depth with their classifications such as PE SVM, M3V, M2V, Hybrid M3V+M2V in the linear modulation range (Mi < 0.907). The simulation and hardware results are obtained for these SVM techniques for the validation purpose. From the results, it is observed that NTV SVM gives better output voltage, however it suffers with poor CMV. Then the M^3V technique is developed to reduce the CMV to minimum value and found the success, but due to the presence of only medium vectors the NPF is very high compared to other SVM techniques. To overcome the CMV and NPF issues, hybrid SVM technique is considered by combining M^3V and M^2ZV. This hybrid M^3V+M^2ZV SVM technique resulted in lower CMV and NPF when related to other SVM techniques. Then the discussion is made on 3D SVM techniques, where the performance is increased due to the absence of redundant vectors.

For the applications of renewable energy sources link PV, Wind, etc., the capacitor voltages at the upper and lower leg are unequal. The issue of asymmetrical DC source is rectified by making a modification in the time duration. Thus, the operation of NPC MLI for asymmetrical DC source is made possible. Then, the discussion is made on SVM techniques for the Over modulation Region ($M_i \geq 0.907$). When the OVM region comes into act, the circular trajectory is also considered along with the hexagonal trajectory path. This process is divided into two regions as OVM-I ($0.907 < Mi < 0.9535$) and OVM-II ($0.9535 < M_i < 1$). The results are taken for Linear modulation region, OVM-I region and OVM-II region and compared. The processing speed at the OVM region is higher when compared to Linear Modulation region due to the time taken to calculate new duty cycle ratio. The CMV and NPF problems are minimized by the introduction of OEW topology, where two inverters are used with separate DC sources to operate the motor. Due to usage of separate DC source, the NPF problem is resolved and the CMV is minimized by selecting the specific switching vectors.

Then the review is made for 5-phase inverter drive where the voltage stress is reduced when compared to 3-phase inverter drives. Also, the harmonic content and CMV is reduced along with optimum DC-link voltages. The SVM techniques for 2L and 3L inverters are explained along with the available CMV reduction techniques for 5-phase NPC MLI. The OEW topology for 5-phase inverter is also explained. This paper also gives the mathematical analysis of the CMV generation for both 3-phase and 5-phase inverter drives. Based on the studies made in this paper, the future advancements are listed in the Future Trends and Research Directions section.

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