A Constant Frequency Output-Ripple-Voltage-Based Buck Converter Without Using Large ESR Capacitor

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***Abstract*—A constant frequency output-ripple-voltage based CMOS current-mode dc–dc buck converter, providing fast load transient response and reference-tracking speed, is proposed in this paper. Unlike V^2 control output-ripple-voltage based buck converter, the proposed buck converter can achieve fast and stable load transient response without relying on ESR value of output capacitor. In addition, the proposed converter has faster reference-tracking speed than the V^2 control counterparts by about 25 times.**

***Index Terms*—Buck converter, current-mode control, V^2 control, reference tracking.**

I. Introduction

In TODAY'S consumer market, computing power of battery-operated portable equipments such as mobile handsets, MP3 players and personal digital assistances (PDAs) is increasing in order to meet faster data processing demands. Since higher processing speed may result in higher power consumption, active and idle power management through dynamic supply voltage and load current scaling becomes an effective solution to maintain battery operation-time [1]–[5]. When a system changes from the deep sleep mode to the active mode and vice versa, fast supply voltage and load current switching are necessary for lower latency. This motivates the need of high performance dc–dc converters with faster dynamic responses in reference tracking and load transient.

In this paper, a novel constant frequency output-ripple-voltage based control method, based on ideas of derivative-output ripple voltage (DOR) and end-point prediction (EPP), is proposed. A buck converter using this control method can achieve the same fast load transient response as a V^2 control buck converter [6]–[9] without relying on equivalent series resistance (ESR) of output capacitor, which is a widely varying parameter and thus makes the performance of V^2 control buck converter unreliable. Besides the load current switching, dynamic supply voltage scaling is another method recently used for power-performance optimization. Therefore, dc–dc converters with fast reference tracking to provide fast change of regulated supply voltages are also important for energy-saving purpose. As will be explained in the next section, inherent architecture of V^2 control buck converter cannot achieve fast reference tracking. By making use the idea of EPP scheme, the tracking speed of the proposed buck converter can be much faster than the one with V^2 control.

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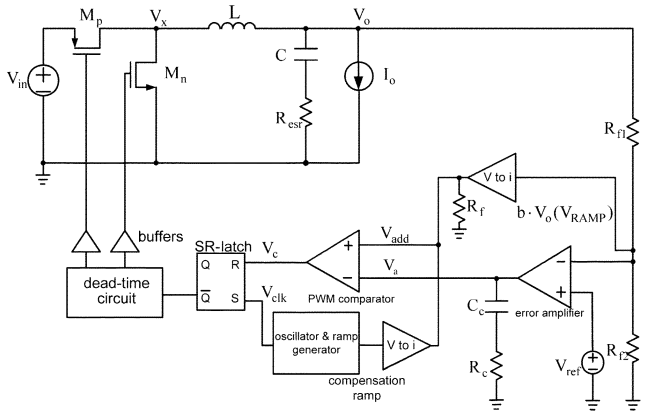

Fig. 1. V^2 control buck converter.

Problems on V^2 control buck converter, including the ESR-dependent reliability and slow reference tracking speed, will firstly be addressed in Section II. The proposed control method will be introduced in Section III; comparison with the V^2 control method will also be given. In Section IV, experimental results will be included to verify the design and performance.

II. Limitations of V^2 Control Buck Converter

In this section, the drawbacks of V^2 control method are discussed. The structure of a V^2 control buck converter is shown in Fig. 1. Output voltage (V_o) is used to generate pulsewidth modulation (PWM) ramp signal $(V_{\rm ramp})$ as well as error voltage signal (V_a). Duty ratio (D) is determined by comparing V_a to $V_{\rm ramp}$ in a switching period. Since V_o is used to generate $V_{\rm ramp}$, change in load current (I_o) will affect the dc level of $V_{\rm ramp}$ and thus alter D immediately bypassing the slow varying V_a. Therefore, an improvement in load transient response can be achieved. The output ripple voltage (v_o), generated by inductor ripple current (i_L) flowing into the output capacitor (C), is composed of two components which is given by

$$v_o = v_{o|\rm esr.} + v_{o|c} \tag{1}$$

where $v_{o|\rm esr}$ is the ripple voltage generated by the ESR of the output capacitor and $v_{o|c}$ is the ripple voltage generated by the output capacitance C. The ripples of $v_{o|\rm esr}$ and $v_{o|c}$ can be expressed as

$$\Delta V_{o|\rm esr.} = \Delta i_L \cdot R_{\rm esr} \tag{2}$$

$$\Delta V_{o|c} \approx \frac{V_o(1-\mathrm{D})}{8\mathrm{LCf}_{\mathrm{sw}}^2} = \frac{\Delta i_L}{8\mathrm{Cf}_{\mathrm{sw}}} \tag{3}$$

respectively, where f_{sw} is the switching frequency of the buck converter and Δi_L is the inductor current ripple. With the assumption that the output voltage ripple ΔV_o is dominated by $\Delta V_{o|\mathrm{esr}}$, the ripple of V_{ramp} can be linear and proportional to the inductor current ripple. Therefore, the small signal analysis of V^2 control is similar to peak current-mode control as both control methods sense the inductor ripple current as the ramp signal [8]. Like peak current-mode control, V^2 control also suffers the problem of sub-harmonic oscillation. A compensation ramp with adequate amplitude is needed to add to V_{ramp} to avoid the oscillation as shown in Fig. 1. The validity of the assumption that ΔV_o is dominated by $\Delta\, V_{o|\mathrm{esr}}$ depends on the ratio of $\Delta V_{o|c}$ to $\Delta V_{o|\mathrm{esr}}$ which is given by

$$\frac{\Delta V_{o|c}}{\Delta V_{o|\mathrm{esr}}} = \frac{1}{8 \cdot R_{\mathrm{esr}} \cdot C \cdot f_{\mathrm{sw}}}. \tag{4}$$

Equation (4) shows that the assumption is only valid when output capacitor with high ESR value and output capacitance product $(R_{\mathrm{esr}} \cdot C)$ is used. For typical parameters of 500 kHz switching frequency, 10 μF output capacitance and 50 mΩ ESR, the ratio of capacitive ripple to ESR ripple is 0.5, which means that the effect of the capacitive ripple to the system stability should be considered in general cases. Impedance of output capacitor is given by

$$Z_c = R_{\mathrm{esr}} + \frac{1}{\mathrm{j}\omega C}. \tag{5}$$

Equation (5) implies that the impedance can sense the inductor ripple current with phase delay due to the imaginary part. The phase delay increases with decreasing $R_{\mathrm{esr}} \cdot C$. It will be shown in next section that too large phase delay not only cause the pulse skipping problem [9], but also degrade the settling time. Even though increasing the amplitude of the compensation ramp can solve the pulse skipping problem, the V^2 control method will behave more like a voltage-mode control rather than the peak current-mode control as V_{add} is dominated by the compensation ramp. This will further degrade the dynamic response of V^2 control converter [10].

Another limitation of V^2 control method is the slow reference-tracking speed. This can be explained by the opposite polarity of the ramp signal path and the error signal V_a path in modulator gain [8]. Suppose an increment of V_o is triggered by positive step of V_{ref} as shown in Fig. 2. V_a will increases as follows to the increase of the duty ratio D and hence V_o. However, the increase of the dc-voltage of ramp signal V_{ramp}, which is proportional to V_o, will tend to decrease D and slow down the transient response of V_a at the same time.

III. Proposed Ouput-Ripple-Voltage Based Control

The proposed output-ripple-voltage based control method, based on two control scheme: DOR and EPP, is proposed in this section. The DOR control scheme provides the buck converter an ESR-independent fast load transient response comparable with V^2 control while the EPP control scheme significantly enhances reference tracking speed of the buck converter.

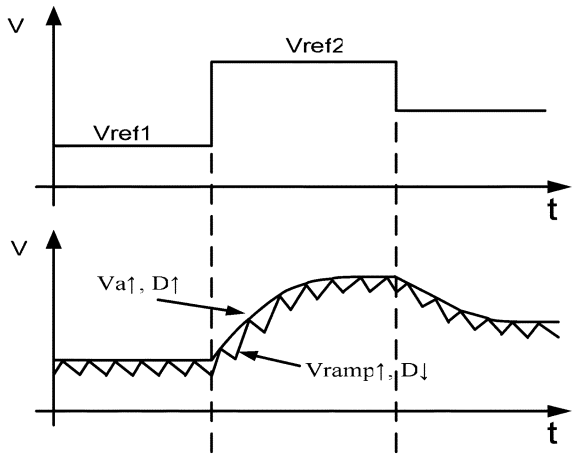

Fig. 2. Change of V_{ref}, V_a and V_{ramp} during reference tracking.

A. DOR Control Scheme

It is known that the 90° phase-shifted capacitive ripple accounts for the phase delay of output ripple voltage. The ESR ripple, which carries real-time inductor ripple current information, should dominate the output ripple voltage for stable operation of V^2 control buck converter. This is difficult to be achieved, especially when low-ESR, high quality surface-mount ceramic capacitors are used. Therefore, this subsection introduces the idea of DOR scheme. The goal of this control scheme is to retain and amplify the sensed inductor ripple current at any $R_{\mathrm{esr}} \cdot C$ condition. The capacitive ripple voltage $v_{o|c}$, which is inherently generated by integration of inductor ripple current i_L, can be expressed as

$$v_{o|c} = \frac{1}{C} \int i_L \mathrm{dt}. \tag{6}$$

Thus, differentiate $v_{o|c}$ can recover the inductor ripple current information. Fig. 3 shows the structure of the differentiator for DOR scheme. The transfer function of the differentiator is given by

$$H(s) = \frac{A_o}{1+A_o} \cdot \frac{1 + sR_dC_d}{1 + \frac{s}{1+A_o}\left(R_dC_d + \frac{1}{p_1}\right) + \frac{s^2}{1+A_o}\left(\frac{R_dC_d}{p_1}\right)} \tag{7}$$

where A_o and p_1 are low frequency gain and dominant pole of the transconductance amplifier, respectively. The second order transfer function in (7) indicates that the differentiator has a pair of complex poles at the same frequency. The zero and the complex poles in (7) define the frequency range f_{diff} of the input signal that can be effectively differentiated, which is given by

$$\frac{1}{2\pi R_dC_d} < f_{\mathrm{diff}} < \sqrt{\frac{(1+A_o)p_1}{2\pi R_dC_d}} \approx \sqrt{\frac{\mathrm{UGB}}{R_dC_d}} \tag{8}$$

where UGB is the unity-gain bandwidth of the amplifier.

At low-frequency domain, the differentiator acts as a voltage buffer to provide V_{ramp} with dc-output voltage information.

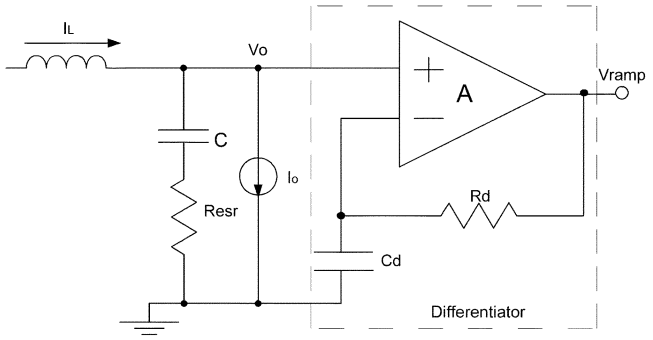

Fig. 3. Structure of the differentiator.

After the differentiation, $v_{o|c}$ is converted to $v'_{o|c}$, which can be expressed as

$$v'_{o|c} = \frac{R_d C_d}{C}\frac{d}{\mathrm{d}t}\int i_L \mathrm{d}t = \frac{R_d C_d}{C} i_L. \tag{9}$$

Based on (7) and (9), the ripple voltage of V_{ramp} is superposition of output ripple voltage v_o and $v'_{o|c}$ which is given by

$$v_{\mathrm{ramp}} = \left(R_{\mathrm{esr}} + \frac{R_d C_d}{C}\right)\cdot i_L + \frac{1}{C}\int i_L \mathrm{d}t. \tag{10}$$

Equation (10) neglects the differentiation of ESR ripple as it only determines the amplitude of v_{ramp} and has no effect to the rising/falling slope of v_{ramp}. Fig. 4 shows the waveform of v_{ramp} at non-zero and zero-ESR condition, respectively. It can be found that even at zero-ESR condition, i_L can still be sensed by the factor of $R_d C_d/C$. The ratio of the capacitive ripple $\Delta V_{o|c}$ to the sensed inductor current ripple ΔV_{iL} at zero-ESR condition is

$$\frac{\Delta V_{o|c.}}{\Delta V_{\mathrm{iL}}} = \frac{1}{8\mathrm{R}_d C_d f_{\mathrm{sw}}}. \tag{11}$$

Equation (11) shows that $\Delta V_{o|c}$ can always be ignored with condition that $R_d C_d \gg 1/8f_{\mathrm{sw}}$. This condition is independent of ESR and the output capacitance, which means that the performance of DOR control buck converter is not constrained by selection of the output capacitor.

Simulation using AMS 0.35-μm BSIM3v3 CMOS model have been carried out to verify the idea of DOR control scheme. Figs. 5 and 6 show the simulation results of load transient responses (I_o: 50 $\rightarrow$ 500 mA) of a V^2 control buck converter and a DOR control buck converter with different value of $R_{\mathrm{esr}} \cdot C$. Both converters are equipped with same inductor ($L = 3.3$ μH) and dominant-pole compensation network ($C_c = 22$ nF, $R_c = 0$) for fair comparison. The switching frequency f_{sw} is 500 kHz. At sufficient large $R_{\mathrm{esr}} \cdot C$ condition, both converters perform fast load transient response with 10 μs settling time. When lower $R_{\mathrm{esr}} \cdot C$ is used, the 90° phase shifted capacitive ripple $v_{o|c}$ becomes comparable to the ESR ripple $v_{o|\mathrm{esr}}$. The settling time of V^2 control buck converter increase as the converter cannot detect the inductor ripple current information correctly during the load current switching. In contrast, DOR control buck converter performs the same settling time at different $R_{\mathrm{esr}} \cdot C$. condition. Therefore, with the idea of DOR control scheme, fast load transient response can be guaranteed without relying on ESR or capacitance value.

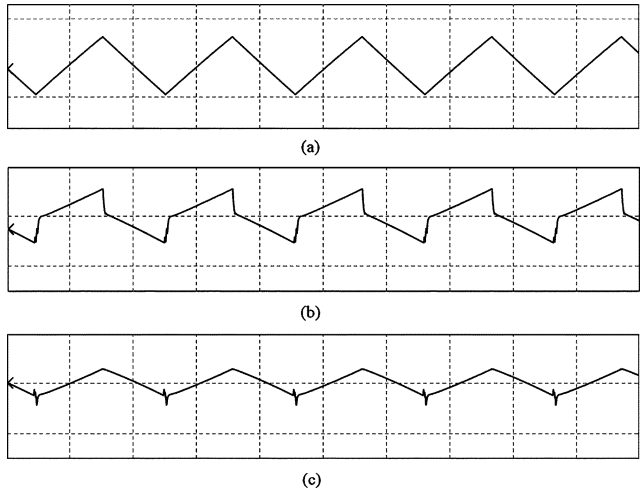

Fig. 4. Waveform of (a) inductor ripple current I_L (b) v_{ramp} with non-zero ESR (c) v_{ramp} with zero ESR.

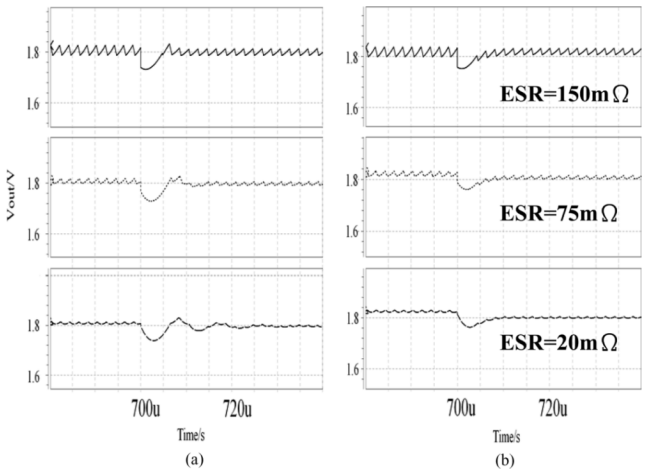

Fig. 5. Simulated load transient response with fixed C (10 μF) and variable ESR. (a) V^2 control buck converter. (b) DOR control buck converter.

B. EPP Control Scheme

Like V^2 control, the buck converter using DOR control scheme also suffers the same problem of slow reference-tracking speed since both methods obtain inductor ripple current information from V_o. An EPP control scheme has been proposed by Siu *et al.* [11] to improve the reference-tracking speed of a voltage-mode buck converter. The realization of EPP scheme has been simplified without using the ramp-amplitude alteration circuit and applied to the DOR control buck converter to improve the tracking speed.

In either V^2 control or DOR control scheme, the dc voltage of V_{ramp} is proportional to V_o. Therefore, the step change of V_{ramp} for reference tracking is given by

$$\Delta V_{\mathrm{ramp}} = b \cdot \Delta V_o = \Delta V_{\mathrm{ref}} \tag{12}$$

where b is the feedback factor, ΔV_o and ΔV_{ref} are the step change of V_o and the reference voltage (V_{ref}), respectively. As the duty cycle (D) is determined by comparing the peak

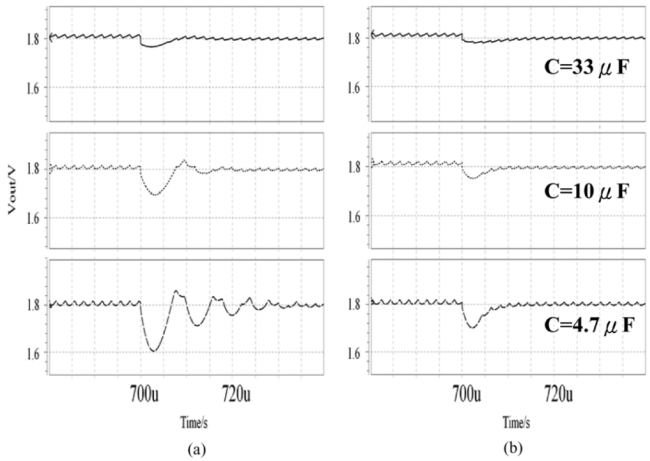

Fig. 6. Simulated load transient response with fixed ESR (50 mΩ) and variable C. (a) V^2 control buck converter. (b) DOR control buck converter.

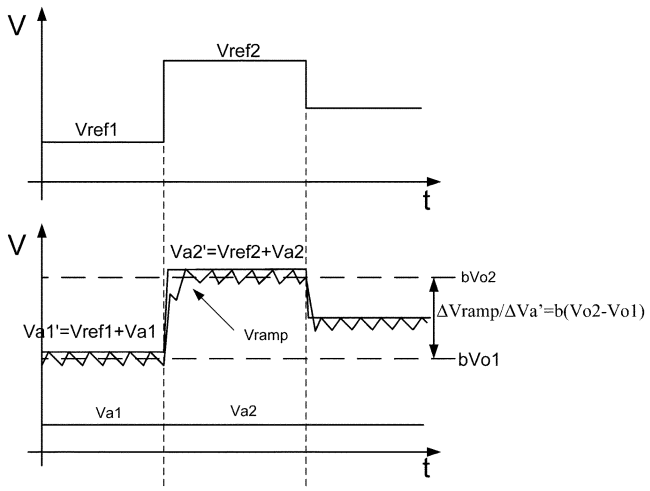

Fig. 7. Change of $V_{\rm ref}$, V_a, V_a' and $V_{\rm ramp}$ during reference tracking with EPP control scheme.

of $V_{\rm ramp}$ with the error-amplifier output voltage (V_a), the step change of V_a for reference tracking is expressed as

$$\Delta V_a = \Delta V_{\rm ramp} = \Delta V_{\rm ref}. \tag{13}$$

Equation (13) shows that ΔV_a can be predicted. Based on the concept of EPP scheme, a new voltage V_a', which is the sum of $V_{\rm ref}$ and V_a, is generated and compare with $V_{\rm ramp}$. The summation is implemented with the current-mode voltage adder shown in [11]. During reference tracking, a step change of $V_{\rm ref}$ will directly move V_a' to targeted position as shown in Fig. 7. Since the change of V_a' is independent of the slow varying signal V_a, the reference-tracking speed is much improved.

Simulation results of DOR control buck converters with and without EPP control scheme are shown in Fig. 8. Same pole-zero cancellation network with $C_c = 4.7$ nF and $R_c = 5$ kHz are used for comparison. When EPP control scheme is applied to the DOR control buck converter, the reference-tracking speed is improved by 25 times with 0.5 V V_o change.

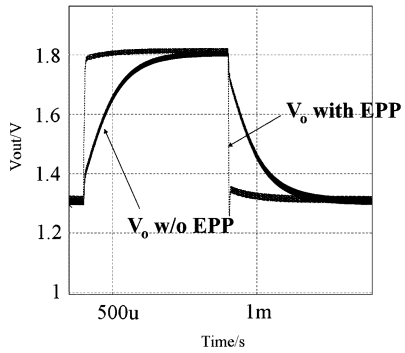

Fig. 8. Simulated reference tracking of DOR control buck converter with and without EPP control scheme.

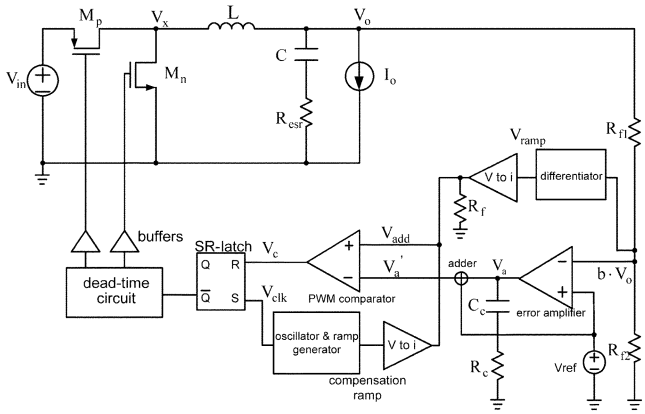

Fig. 9. Proposed buck converter with DOR and EPP control schemes.

C. Structure of the Proposed Buck Converter

Fig. 9 shows the structure of the buck converter with DOR and EPP control schemes. Comparing with the V^2 control buck converter shown in Fig. 1, only an additional differentiator and an adder are needed to implement the ideas of DOR and EPP, respectively. The schematic of the differentiator is shown in Fig. 3 where the amplifier is implemented with a standard current mirror amplifier structure.

IV. Experimental Results

The constant frequency output-ripple-voltage based buck converter has been implemented in AMS CMOS 0.35-μm technology. The micrograph of the proposed buck converter is shown in Fig. 10 and the chip area is 1800 μm $\times$ 1000 μm, including the test pads. The buck converter is supplied with an input voltage $(V_{\rm in})$ of 2.4 V and switching frequency ($f_{\rm sw}$) of 500 kHz. To satisfy the condition that $R_dC_d \gg 1/8f_{\rm sw}$, the values of R_d and C_d inside the differentiator are 270 kΩ and 10.5 pF, respectively, and are integrated into the control circuit.

Fig. 11 shows the steady-state measurement results of the inductor ripple current (i_L), $v_{\rm ramp}$, output ripple voltage (v_o) and V_x in Fig. 9 for the cases of D larger than and less than 0.5. The output capacitance is 4.7 μF and the measured ESR is around 30 mΩ, which means v_o is dominated by the capacitive ripple voltage. It can been seen from the measurement results that the proposed DOR control scheme can effectively sense the rising edge of the inductor current by differentiating v_o.

Fig. 12 shows the load transient response of the proposed buck converter at $V_o = 1.8$ V. The output current change is

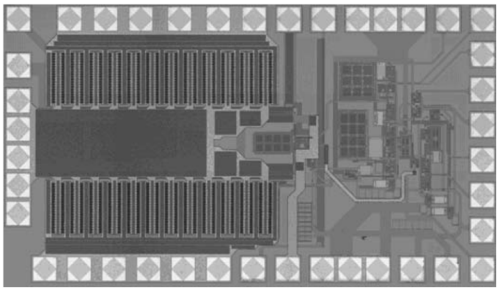

Fig. 10. Micrograph of the buck converter with DOR and EPP control schemes.

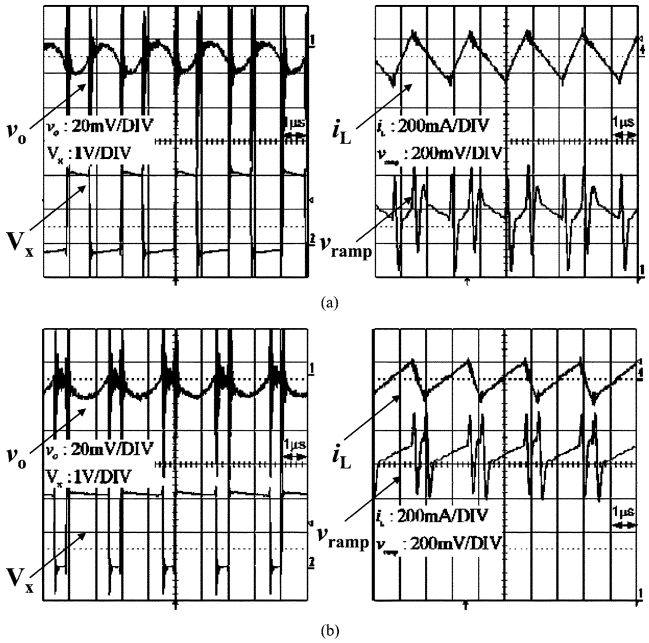

Fig. 11. Steady-state measurement results with (a) $V_o = 0.8$ V ($D < 0.5$), and (b) $Vo = 1.8$V ($D > 0.5$).

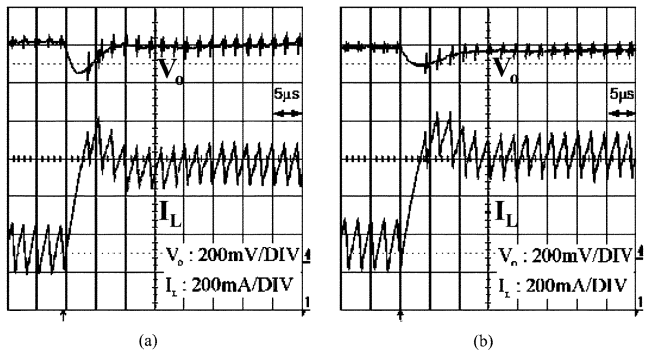

Fig. 12. Measured load transient response of the proposed buck converter with (a) $C = 4.7$ μF, ESR ≅ 30 mΩ, and (b) $C = 10$ μF, ESR ≅ 15 mΩ.

450 mA. Fig. 12 shows no ringing occurs for both cases, which agree well with the theory that fast-load transient response performance can be maintained at low $R_{\rm esr}\,C$ condition.

V_o of the proposed buck converter is measured under $V_{\rm ref}$ switching from 0.65 to 0.9 V and then back to 0.65 V. The feedback factor b is 0.5 and the output current is kept at 250 mA. The measurement results of V_o, $V_{\rm ref}$, V_a', and V_a are shown in Fig. 13. Note that ΔV_a' is approximately equal to $\Delta V_{\rm ref}$. It is

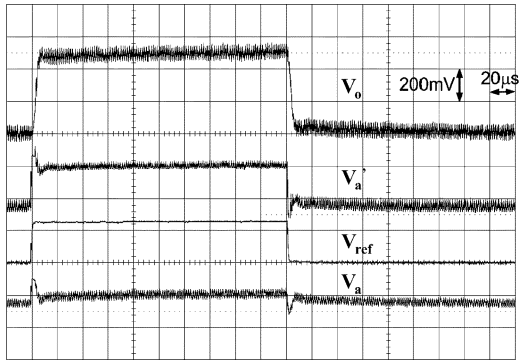

Fig. 13. Measured transient response of the proposed buck converter at reference tracking.

thus verified that the idea of EPP scheme can enhance the reference-tracking speed of DOR control buck converter.

Both the load transient and reference-tracking response time are ~ 10 μs which is much faster than the conventional dominant pole compensated PWM converter response of ~ 100 μs.

V. Conclusion

A constant frequency output-ripple-voltage based buck converter has been reported in this paper and verified by experimental results. The control method is developed based on ideas of DOR scheme and EPP scheme. The problem of ESR-dependent performance for V^2 control converter has been solved by the DOR scheme while the reference-tracking speed has been greatly improved by the EPP scheme.

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