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A Continuous-Time Delta-Sigma Modulator for Biomedical Ultrasound Beamformer Using Digital ELD Compensation and FIR Feedback

Yi Zhang, *Student Member, IEEE*, Chia-Hung Chen, *Member, IEEE*, Tao He, *Student Member, IEEE,* and Gabor C. Temes, *Life Fellow, IEEE*

Abstract—This paper presents the design of a continuous-time ΔΣ modulator (CTDSM) to be used in an ultrasound beamformer for biomedical imaging. To achieve better resolution, the prototype modulator operates at 1.2 GHz. It incorporates a digital excess loop delay (ELD) compensation to replace the active adder in front of the internal quantizer. A digitally controlled reference-switching matrix, combined with the data-weighted averaging (DWA) technique, results in a delay-free feedback path. A multi-bit FIR feedback DAC, along with its compensation path, is used to achieve lower clock jitter sensitivity and better loop filter linearity. The modulator achieves 79.4 dB dynamic range, 77.3 dB SNR and 74.3 dB SNDR over a 15 MHz signal bandwidth. Fabricated in a 65 nm CMOS process, the core modulator occupies an area of only 0.16 mm^2 and dissipates 6.96 mW from a 1 V supply. A 58.6 fJ/conversion-step figure of merit is achieved.

***Index Terms*—Ultrasound beamformer, continuous-time ΔΣ modulator, digital excess loop delay compensation, FIR feedback DAC**

I. Introduction

MEDICAL ultrasound imaging is commonly used for obtaining diagnostic medical images, as a compact and affordable diagnostic tool. It uses beamforming techniques to construct an image of the interrogated medium.

The function of the beamforming receiver is to amplify and demodulate the separate echo signals, provide the proper time delay in each channel, and add the signals. Conventional digital beamformers use Nyquist rate ADCs as an interpolation filter to effectively up-sample the digital sample, so that accurately delayed samples are acquired [1][2]. However, this requires increased hardware complexity.

Oversampling ΔΣ ADCs have recently become attractive in signal processing applications due to their simplicity and ease of integration [3][4]. As shown in Fig. 1, in the ΔΣ ADC based beamforming receiver, the digital signal processing circuitry applies dynamic delays to the digitized output of the ΔΣ modulator in the each channel, so that a coherent combination of the received signals is focused at points along a particular direction of interest [4][5]. In the few reported use of ΔΣ modulation in biomedical ultrasound beamformers [6][7], the dynamic range was only around 60 dB. In the detection of the blood flow by a pulsed Doppler ultrasound receiver, the ultrasound system sends a signal pulse into the body at F_0. The returning echo has a very strong component at F_0 from stationary tissue (the vessel walls) and a very weak signal within 1 kHz of F_0 due to the slow blood flow. To detect this weak blood flow signal in the presence of the strong signal from the tissue, it requires a dynamic range larger than 12 bits.

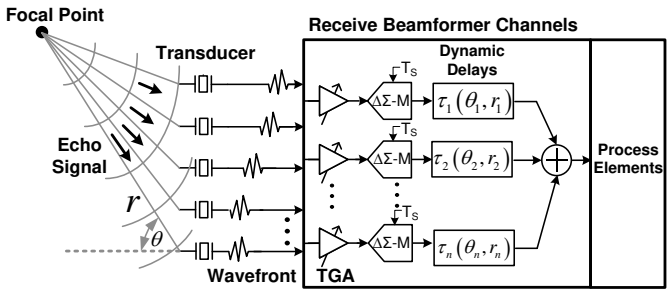

Fig. 1. Block diagram of an ultrasound receiver using dynamic focusing.

In this work, a continuous-time ΔΣ modulator (CTDSM) was chosen as a power-efficient solution to achieve 12-bit effective number of bits (ENOB) over the target signal bandwidth (BW = 15 MHz) of the medical ultrasound. However, CTDSM is susceptible to severe non-idealities, such as excess loop delay (ELD) and clock jitter. Their correction in this project will be discussed next.

In this paper, we give the details of the design, which was reported earlier in [13]. The remainder of the paper is organized as follows. Section II gives the architecture of the modulator. Section III provides a brief overview of prior art addressing the excess loop delay issue, and introduces the proposed technique. Section IV presents the FIR filtering applied in the feedback path, along with its compensation. Circuit design details of important building blocks of the prototype are discussed in Section V. Measurement results of the prototype test chip are provided in Section VI. Section VII concludes the paper.

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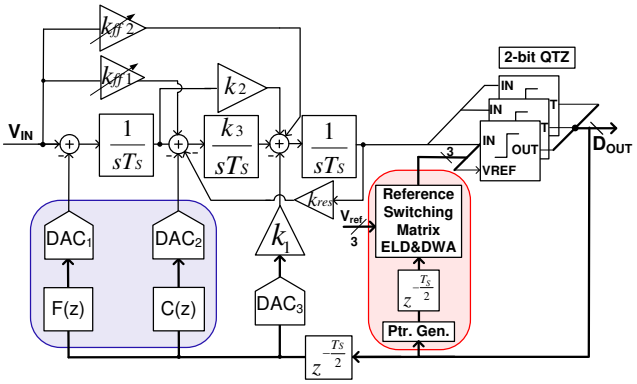


Fig. 2. Block diagram of the proposed CT ΔΣ modulator using digital ELD compensation and FIR feedback.

II. Architecture Details

The architecture of the proposed CT ΔΣ modulator is shown in Fig. 2 [18]. It is well known in loop filter design that the first-order path is usually required to be a fast one, since it largely determines the unity-gain bandwidth of the loop filter, and is essential for the loop stability [8]. Therefore, the parasitic poles of the first-order path may degrade stability [21]. In the conventional Cascade of Integrators with Feedforward (CIFF) topology, the first-order path is implemented by the first integrator feeding the adder at the input of the quantizer. Hence the amplifier used in the first stage integrator is required to be very fast, so as not to limit the unity gain bandwidth of the first-stage integrator. However, the in-band gain of the first-stage integrator also needs to be high enough to provide sufficient attenuation of the non-idealities from the following stages. Hence, it may not be a power-efficient solution to place the first integrator in the high-speed path as in the conventional CIFF topology.

In order to separate the requirements of both high gain and high speed in the first-stage integrator, this work incorporates a 3rd-order loop filter with combined feedforward and feedback paths. Instead of implementing the fastest first-order path by the first integrator, the first-order path is formed by the feedback path k_1 to the input of the last integrator, which replaces an extra summation node required in the CIFF topology. The input feed-forward path k_{ff1} *and* k_{ff2} help to reduce the swing of the internal state.

In addition, a local resonator path k_{res} formed by the second and third integrator introduces zeros in the noise transfer function (NTF) to further suppress the in-band quantization noise. The out-of-band gain (OBG) of the NTF is chosen to be 2, allowed by the use of a 2-bit internal quantizer. Data Weighted Averaging (DWA) technique is employed to randomize the unit element mismatch in the feedback DAC. The feedback DAC is implemented with switched-resistors, which have better noise performance and matching under low supply voltage (1 V) than current steering DAC. To counter the RC time constant variation, the digitally tunable integrating capacitor arrays are employed.

The CTDSM suffers from the excess loop delay [9]. A reference-switching matrix for both ELD compensation and DWA technique is introduced as shown in Fig. 2. In addition, error due to the clock jitter applied in the feedback path increases the in-band noise of CTDSM. To mitigate this effect, a multi-bit FIR filtering path *F(z)* are employed with its compensation path *C(z)*. Both techniques will be discussed in the following sections.

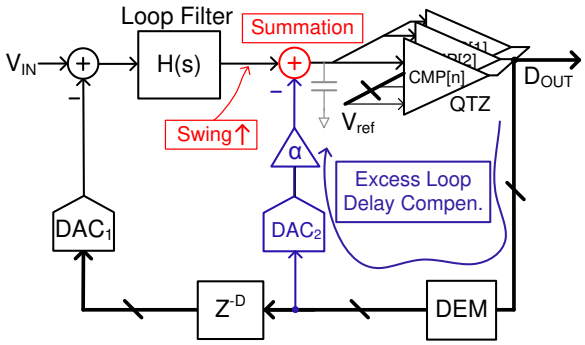


Fig. 3. Block diagram of a general continuous-time ΔΣ modulator with a direct feedback path to compensate for the ELD [9].

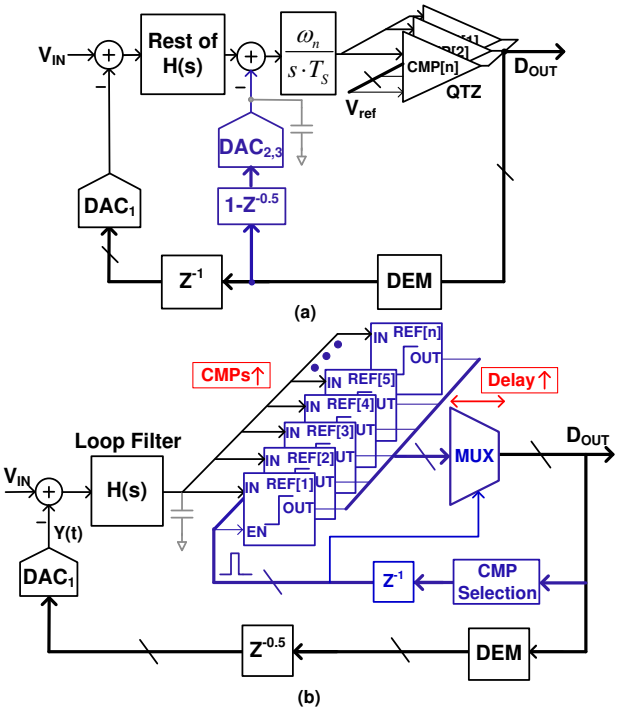
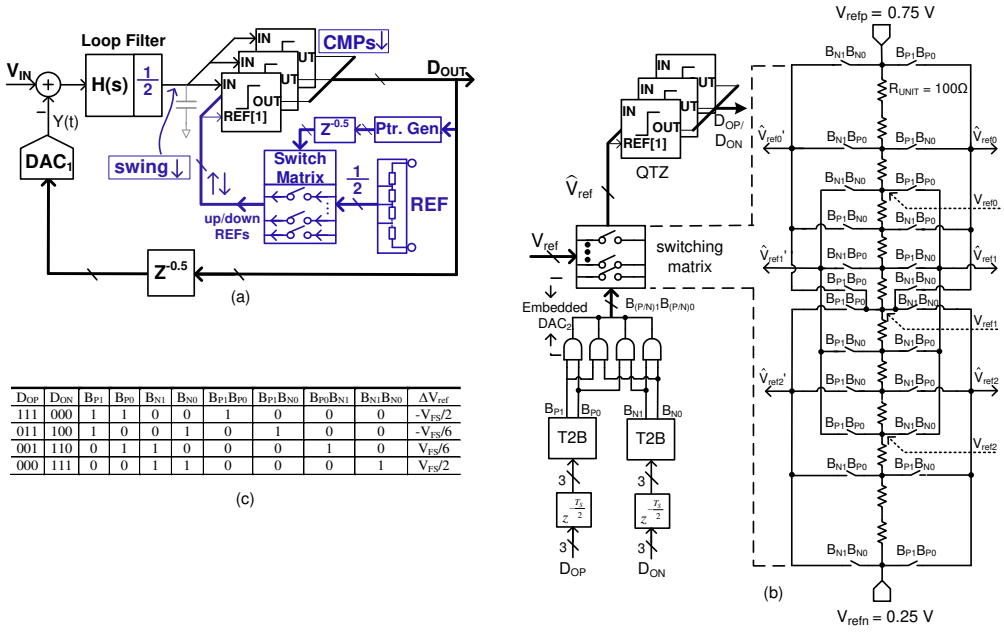


Fig. 4. Prior art. (a) Discrete-time differentiation technique [8] (b) Comparator switching technique [11].

III. Excess Loop Delay Compensation

A. Overview of the Prior Arts

A general block diagram of a continuous-time (CT) ΔΣ modulator with ELD compensation is depicted in Fig. 3 [9][10]. It contains a CT loop filter *H(s)* for in-band noise attenuation; an internal quantizer; a feedback DAC; and a dynamic element matching (DEM) block to filter the DAC element mismatch signal. The ELD compensation absorbs the



D_{OP}	D_{ON}	B_{P1}	B_{P0}	B_{N1}	B_{N0}	$B_{P1}B_{P0}$	$B_{P1}B_{N0}$	$B_{P0}B_{N1}$	$B_{N1}B_{N0}$	ΔV_{ref}
111	000	1	1	0	0	1	0	0	0	$-V_{FS}/2$
011	100	1	0	0	1	0	1	0	0	$-V_{FS}/6$
001	110	0	1	1	0	0	0	1	0	$V_{FS}/6$
000	111	0	0	1	1	0	0	0	1	$V_{FS}/2$

(c)

Fig. 5. (a) Proposed ELD compensation by reference-switching technique with the scaled quantizer (b) Differential implementation details of the control logic and reference-switching matrix, in which $R_{UNIT} = 100\Omega$ (c) possible digitized output sample and the pointer generated to determine the shifted amount.

signal-dependent delay by introducing an intentional delay Z^{-D} between the quantizer and feedback DAC. As a result, a direct feedback path around the internal quantizer is necessary to compensate the inserted delay Z^{-D}. However, this compensation path requires the use of an adder in front of the quantizer. This adder is in the main path, and may introduce a parasitic pole, which is undesirable in high-speed operation.

Several techniques to eliminate the use of this adder have been proposed in recent years [8] [28]. In [8], as illustrated in Fig. 4(a), the addition is shifted to the input node of the last stage integrator using discrete-time differentiation. The pulse of the feedback DAC is first differentiated and then integrated on the capacitor of the last stage integrator, creating a path equivalent to summation in front of the quantizer. In [28], an equivalent feedforward path is introduced by putting a phase-lead resistor (PLR) in series with the integrating capacitor in the last stage integrator. Thus it eliminates the use of a summing amplifier in front of the quantizer. Both technique suffer from one drawback: a feed-in path to the last integrator required to implement the ELD compensation. The extra feed-in path mandates a wide opamp finite gain bandwidth (FGBW) in the last integrator. In addition, the increased parasitics at the input node of the last integrator make it difficult for this integrator to form the fast first-order feedback path, especially for high speed operation

Instead of using an analog feedback path, [11] proposed a digital ELD compensation method, shown in Fig. 4(b). The summation in front of the quantizer is replaced by a group of switching comparators with fixed reference voltages. The increased number of comparators mandates the following multiplexing of the quantizer outputs. The comparator selection logic takes the previous output sample of the modulator, enables the corresponding comparators upwards or downwards and controls the multiplexer to perform the digital summation for ELD compensation. This technique, however, requires additional comparators in the quantizer, which results in the increased parasitic loading, and complicates the design of the last integrator. Furthermore, the multiplexing logic in the critical path, as shown in Fig 4(b), adds to the loop delay.

B. Proposed Digital ELD Compensation

As illustrated in Fig. 5(a) [12][35], rather than switching in or out comparators with fixed reference voltages [11], this work proposes to switch the reference voltages of a fixed set of comparators, which eliminates the following multiplexing as in [11]. A reference-switching matrix, digitally controlled by the pointer generation logic, replaces both the direct feedback path and the signal adder before the quantizer. Fig. 5(b) shows the details of the differential implementation of the reference-switching matrix. In this work, an ELD coefficient α of 0.5, shown in Fig. 3, was implemented. In Fig. 5(b), $\hat{V}_{refi}$ and $\hat{V}_{refi}{}'$ represent the differential threshold inputs to the i^{th} comparator in the quantizer. The full-scale quantization range is $V_{FS} \triangleq V_{refp} - V_{refn}$. The reference levels in the resistor string are shifted in the quantizer by an amount $\Delta V_{ref} \triangleq \hat{V}_{refi} - \hat{V}_{refi}{}'$, which is determined by the previous output sample D_{OP}/D_{ON} of the modulator. In other words, an equivalent summation is realized by shifting up or down the quantizer reference levels by ΔV_{ref} given by:

$$\Delta V_{ref} = \alpha \cdot \begin{bmatrix} -V_{FS} & -\frac{V_{FS}}{3} & \frac{V_{FS}}{3} & V_{FS} \end{bmatrix} \times \begin{bmatrix} B_{P1} \cdot B_{P0} \\ B_{P1} \cdot B_{N0} \\ B_{P0} \cdot B_{N1} \\ B_{N1} \cdot B_{N0} \end{bmatrix} \quad (1)$$

where α is the ELD compensation coefficient which here is equal to 0.5; $[-V_{FS} \; -\frac{V_{FS}}{3} \; \frac{V_{FS}}{3} \; V_{FS}]$ are the four quantization levels of the 2-bit quantizer. B_{Pi} and B_{Ni} are the converted

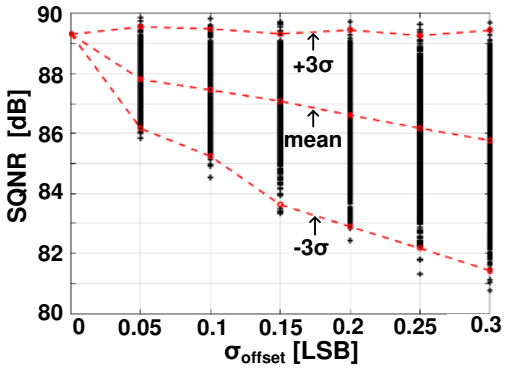


Fig. 6. Simulated SQNR as a function of comparator offsets with the line representing the mean SQNR and SQNR distributed within ±3σ.

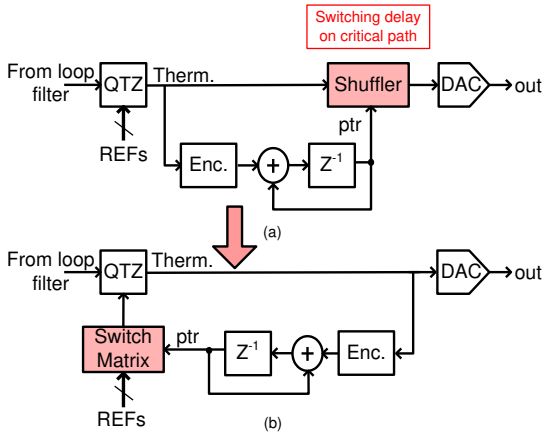


Fig. 7. Block diagram of (a) Conventional thermometer-code shuffling DWA (b) Reference shuffling DWA.

binary representation of the digitized sample; $B_{Pi} \cdot B_{Ni}$ are generated by the pointer generation logic, which involves a thermometer-to-binary conversion and an *AND* logic, as shown in the left part of Fig. 5(b); Fig. 5(c) gives all possible values of D_{OP}/D_{ON} and pointers $B_{Pi} \cdot B_{Ni}$; ΔV_{ref} corresponds to the shift in the reference levels. From (1), one shifted amount is selected out of the first vector for the next quantization based on the current quantized sample output in the second vector. Based on (1), it can further implement the ELD coefficient α other than 0.5 by changing ΔV_{ref} with appropriate design of the adjacent reference levels.

The operation of both the pointer generation logic and the reference-switching matrix is allocated half a clock period, so that the shifted reference voltages are able to settle within the other half a clock period for the next quantization. The unit resistor in the reference matrix, as shown in Fig. 5(b), is chosen to be 100 Ω, leading to around 420 μW of power dissipation. Care has to be taken in the routing so as to minimize the parasitics along the reference-switching path and the resulting settling requirement. The settling error in the reference-switching matrix is approximated by an offset in the quantizer and fortunately it can be suppressed by the preceding loop filter. This technique effectively reduces the number of comparators in the quantizer and as a result, it eliminates the multiplexing logic delay in the critical path.

In the described ELD compensation techniques, however, the swing of the loop filter output is increased in the presence of the direct ELD compensation feedback path. In order to allow the use of a power supply as low as 1 V, the loop filter was scaled down by a factor of 2. Accordingly, the reference voltages of the quantizer were also scaled by the same factor. This effectively scales up the quantizer gain so that the loop gain remains unaffected. This downscaling of the quantizer reference voltages may make the comparator offset requirements harder to meet. However, the number of the comparators used in the quantizer is low, and extensive simulations were made to guarantee that the comparator offset in the quantizer would not be a major source of error in the modulator. For each level of comparator offset, 1000 samples were simulated as shown in Fig. 6. The broken lines represent the mean SQNRs and the SQNRs distributed within ±3σ. It shows that in the quantizer with downscaled reference voltages, even with a 0.3 LSB 1-σ offset (12.5 mV), the achieved SQNR is above 80 dB, leaving a 6 dB margin above the target of 12-bit ENOB. Careful sizing of the comparator input pair and common centroid layout technique were used to guarantee minimal degradation of the performance due to the offset of the comparator.

C. *Reference Shuffling DWA*

The use of 2-bit feedback DAC requires data-weighting averaging (DWA) to shape the DAC element mismatch error. In the conventional DWA technique, as shown Fig. 7(a), the thermometer output code of the quantizer is encoded and generates a pointer to select the quantizer output. However, the shuffler functions in the main feedback path, and hence its switching delay contributes to the excess loop delay. At a clock rate of 1.2 GHz, the delay through such a shuffler is comparable to the clock period, and thus significantly reduces the regeneration time budget of the comparators.

The converter described in this work uses a reference-switching matrix to eliminate the element shuffler located in the feedback path [21][22], as shown in Fig. 7(b). Rather than shuffling the thermometer code of the quantizer output, the pointer generation logic follows the DWA rotation algorithm, and drives the switching matrix to shuffle the quantizer reference voltages and obtain the next quantizer output to be applied to the DAC. This technique effectively results in a delay-free path.

Similar to the proposed ELD compensation technique, the pointer generation logic is also employed to manipulate the quantizer reference matrix. Thus, these two reference-switching matrices are merged.

IV. Prototype CT ΔΣ ADC with FIR Feedback

Another design challenge in CT ΔΣ modulators comes from the error introduced by the jitter-affected clock applied to the feedback DAC. This error is referred to the input without being shaped by the loop filter, as demonstrated in Fig. 8(a). A modulator using multi-level feedback is less susceptible to

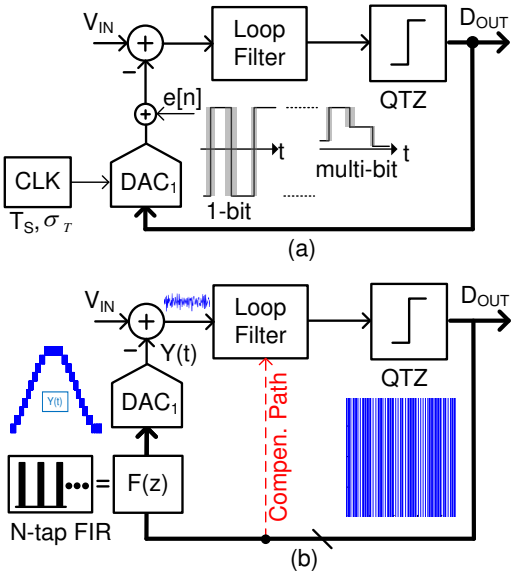


Fig. 8. Block diagram of (a) clock jitter induced error model (b) FIR feedback DAC, along with its compensation path.

clock jitter than a single-bit one due to the reduced step size in the DAC.

One technique to reduce the clock jitter sensitivity is the use of an FIR filter *F(z)* in the feedback path [15], as illustrated in Fig. 8(b). The in-band noise power *J* due to the clock jitter [16][17] with the FIR feedback path is:

$$J = \frac{\sigma_{jit}^2}{T_S^2}\frac{\sigma_{lsb}^2}{\pi OSR}\int_0^{\pi}\left|\left(1-e^{-j\omega}\right)NTF\left(e^{j\omega}\right)F\left(e^{j\omega}\right)\right|^2 d\omega \quad (2)$$

where σ_{jit}^2 is the variance of the clock jitter; σ_{lsb}^2 is the variance of the quantization noise of the internal quantizer; *OSR* is the oversampling ratio of the modulator; $NTF(e^{j\omega})$ is the noise transfer function of the modulator; and $F(e^{j\omega})$ is the transfer function of the FIR feedback path.

It is clear that the low-pass FIR filter *F(z)* attenuates the quantization noise at high frequency, and thus reduces the integrated noise power due to the clock jitter. In the time domain, the use of the FIR filter applied to the single-bit feedback DAC averages the adjacent samples, and reduces the step size from sample to sample, which simulates the benefits of the multi-level feedback. However, the introduction of the FIR feedback path necessitates a compensation path for the added delay and phase shift.

A. *Compensation of the FIR Feedback Delay*

Techniques for the compensation of the FIR feedback delay have been proposed in recent works [19][20][25]. In [19], an analog feedback compensation path is employed. This technique increases the complexity, and the implemented NTF is changed from the ideal one. Ref. [20] adopts another FIR path to compensate for the delay of the main FIR feedback. This compensation path is fed into the last-stage trans-impedance amplifier (TIA) output. Ref. [25] feeds the FIR compensation path to the input of the last stage integrator.

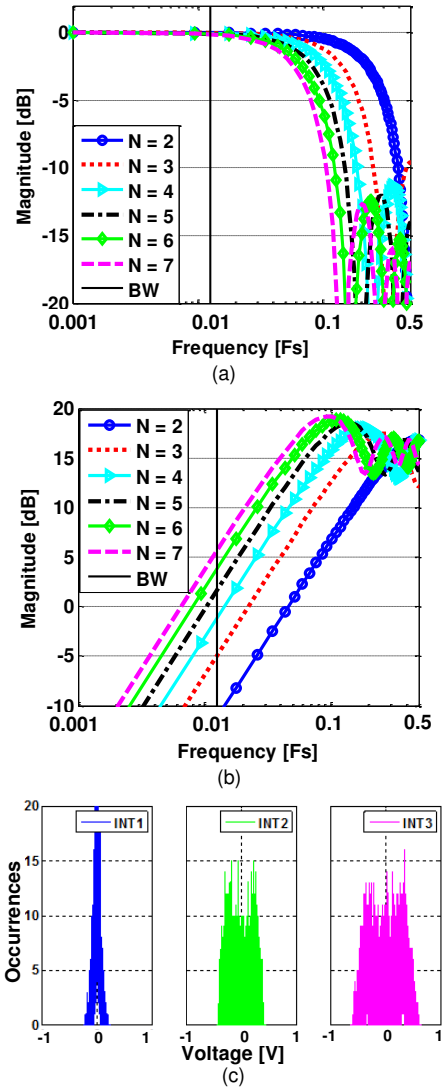


Fig. 9. (a) Frequency responses of FIR feedback path F(z). (b) Frequency responses of the FIR compensation path C(z) for different tap lengths N (c) Histograms of the each integrator output swing in the loop filter for tap length N = 3.

Both methods tend to increase the parasitic in the last stage integrator, which is problematic for a modulator running at 1.2 GHz.

This work, as shown in Fig. 2, uses a simple FIR feedback path *C(z)* to compensate the delay introduced by the main FIR feedback *F(z)*. As discussed in Section II, the last integrator implementing the fastest 1st-order path of the loop filter is in the high-speed path of the modulator loop. Additional feed-in paths to the last stage integrator will tend to create parasitic poles and result in increased delay. Hence, rather than connecting the compensation path to the last stage integrator, as in [20], the compensation path *C(z)* feeds into the input of the second integrator. Simulations shows that this simple change reduces the required unity gain bandwidth (UGBW) of the opamp of the last stage integrator from 1.6 times sampling frequency F_S to 1.2 F_S while maintaining the same performance.

One concern about the feedback compensation path *C(z)* is the increased output swing at the first-stage integrator output,

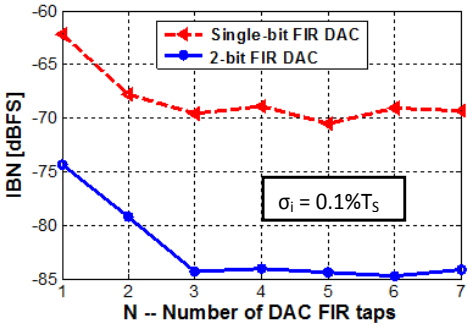


Fig. 10. In-band-noise due to a $\sigma_j = 0.1\%T_S$ clock jitter versus the FIR tap length N, for both single-bit and 2-bit FIR DAC.

due to the input signal content feeding into this node. However, the compensation path *C(z)* can have a high-pass profile, as shown in Fig. 9(b). This is because the added low-pass main FIR *F(z)* mainly affects the high-frequency response of the loop filter, and hence the compensation path *C(z)* only needs to compensate the medium- to high-frequency loop gain.

Thus, the signal content is further attenuated before feeding into this node, and the output swing at the first-stage integrator can be kept at a reasonable level, as shown in Fig. 9(c), which illustrates the histograms of the integrator output swings, normalized to the full scale of the quantization. Note that the low output swing of the first-stage integrator is mandatory for low-voltage design.

B. FIR Filter and Feedback DAC Design Considerations

Eq. (2) shows that the FIR feedback DAC reduces the sensitivity to clock jitter, due to its high frequency attenuation. This implies that increasing *N* must result in improved performance in terms of the sensitivity to the clock jitter, as more shaped quantization noise is filtered out. However, this holds true only for *F(z)* with a small number of tap *N*. As *N* increases, the main FIR feedback path *F(z)* exhibits better selectivity and higher stop-band attenuation, as shown in Fig. 9(a). In other words, *F(z)* with larger *N* results in larger attenuation in the medium-to-high frequency range. Therefore it requires a compensation path *C(z)* with higher out-of-band gain to stabilize the loop. This is illustrated in Fig. 9(b), where the frequency response of *C(z)* with different FIR lengths *N* is plotted. It is seen that *F(z)* with larger *N* leads to higher out-of-band-gain of *C(z)*.

From (2), the input-referred jitter-induced noise power *J'* due to *C(z)* can be found as:

$$J' = \int_0^{\frac{\pi}{OSR}} \frac{J_{C(z)}}{G_1(j\omega)} d\omega \tag{3}$$

$$J_{C(z)} = \frac{\sigma_{jit}^2}{T_S^2} \frac{\sigma_{lsb}^2}{\pi OSR} \int_0^{\pi} \left| \left(1 - e^{-j\omega}\right) NTF\left(e^{j\omega}\right) C\left(e^{j\omega}\right) \right|^2 d\omega \tag{4}$$

where $G_1(j\omega)$ is the frequency response of the first-stage integrator, and $J_{C(z)}$ is the noise power due to *C(z)*.

As (4) shows, higher out-of-band gain of *C(z)* tends to increase the jitter-induced noise power, and hence the input-referred noise power *J'* even with the in-band attenuation by the first integrator, as in (3). For high values of *N*, the compensation path *C(z)* may cancel the effects of *F(z)* in reducing the input-referred noise power due to the clock jitter.

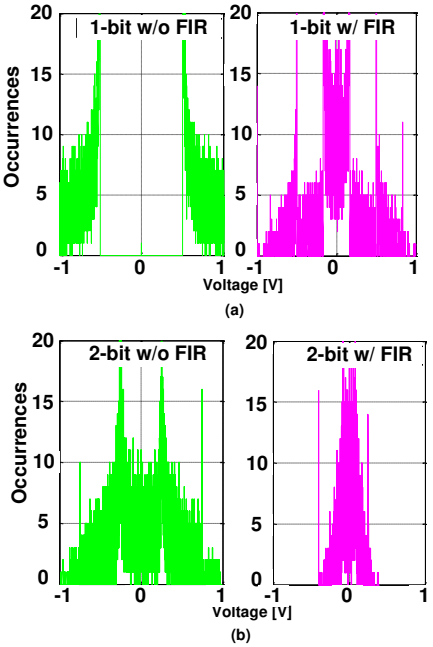


Fig. 11. Histograms of the loop filter input with or without FIR feedback for (a) 1-bit internal quantization (b) 2-bit internal quantization.

In the behavioural simulation, a 0.1% rms clock jitter was applied to the sampling clock period in the feedback path. The in-band-noise due to the clock jitter is plotted as a function of the FIR filter order *N* for both single-bit and 2-bit FIR feedback DACs. Fig. 10 compares the in-band noise power for single-bit and 2-bit internal resolutions as the FIR order *N* increases. An NTF with an out-of-band gain (OBG) is chosen to be 1.5 for a CTDSM with a single-bit quantizer, according to Lee's rule [36], and OBG = 2 for the one with a 2-bit quantizer. As Fig. 10 shows, for FIR tap length $N > 3$, the in-band noise power due to a 0.1% clock jitter saturates for both circuits.

Hence, this device uses a 3-tap FIR filter to achieve reduced clock jitter sensitivity while maintaining design simplicity. Fig. 11(a)(b) compares the histograms of the loop filter input with or without the FIR feedback path for both single-bit and 2-bit quantization, demonstrating the linearity advantage due to the introduction of the FIR feedback path. As shown in Fig. 11(b), the use of a 2-bit feedback achieves much smaller input swing compared to using a single-bit feedback. A 2-bit 3-tap FIR feedback branch was therefore adopted in our work.

V. Circuit Implementation

The overall schematic of the CT ΔΣ modulator is shown in Fig. 12. It includes a CT loop filter, a 2-bit flash quantizer, an FIR filtering feedback DAC *F(z)* with its compensation path *C(z)*, and the reference-switching matrix for ELD compensation and DWA. The key building blocks are described next.

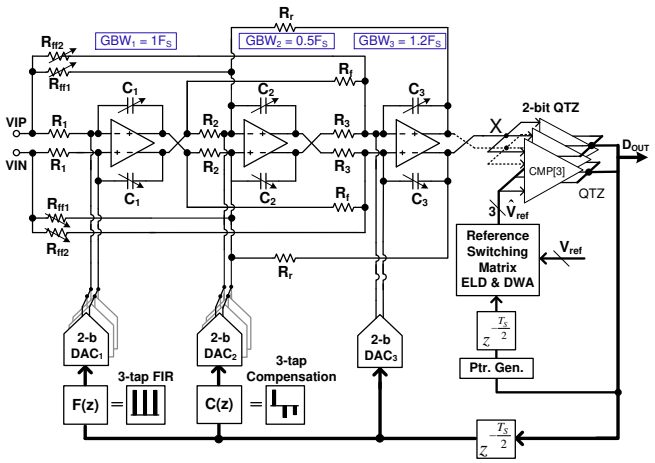


Fig. 12. Schematic of the overall continuous-time ΔΣ modulator [13].

A. *Loop Filter*

The circuit of the opamp used in the loop filter is a two-stage design that employs no capacitor feed-forward (NCFF) compensation rather than a Miller capacitor [13][23]. The single-end representation of the opamp block diagram is shown in Fig. 13. The feedforward path g_{mff} creates a zero to stabilize the two-stage opamp. Compared to a Miller-compensated design, this architecture is more power-efficient, since no extra power is spent on charging and discharging the Miller capacitors. Thanks to the FIR feedback DAC, the linearity requirement of the first integrator is greatly relaxed. All opamps used in the latter stages share the same topology.

The input resistance R_1 and capacitance C_1 of the first stage integrator are chosen to be 2.5 kΩ and 1.5 pF, respectively. Power reduction and linearity enhancement can be achieved by maximizing the R_1 up to the thermal noise limit [37], which is given by:

$$P_N = 8kTB_W\left[R_1 + R_{DAC}\frac{R_1^2}{R_{DAC}^2} + \frac{2}{3g_{m,OTA}}\left(1+\frac{R_1}{R_{DAC}}\right)^2\right] \quad (5)$$

where P_N is the input-referred thermal noise of the modulator and B_W is the signal bandwidth; R_{DAC} refers to the resistors used for feedback DAC, and $g_{m,OTA}$ represents the amplifier input transconductance.

Fig. 14 shows the simulated modulator output power spectrum density (PSD) with only quantization noise and with thermal noise also included. The quantization noise is designed to be well below the thermal noise and hence the modulator performance is limited by the thermal noise. It achieves an SQNR of 87dB and an SNR of 78 dB.

B. *FIR Feedback DAC*

Rather than using a current steering DAC, this work adopted a switched-resistor (SR) feedback DAC. This was because for low-voltage (1 V) implementation the SR DAC is less noisy than a current-steering DAC, whose noise performance is limited by the available voltage headroom. Also, the SR DAC can provide better matching performance than a current steering one with low headroom.

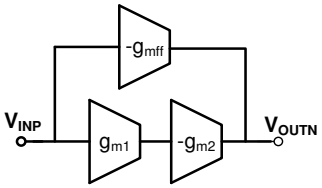


Fig. 13. Block diagram of the NCFF opamp.

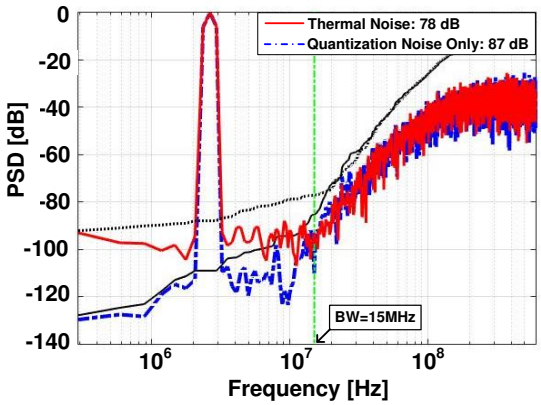


Fig. 14. Simulated power spectrum density with only quantization noise, and thermal noise also included.

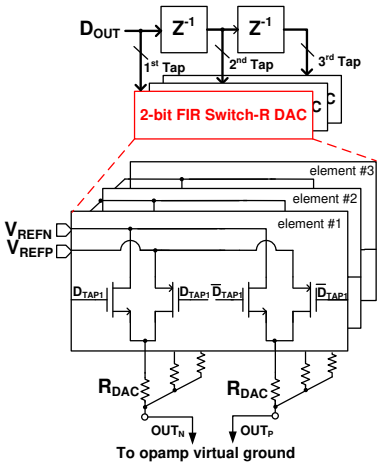


Fig. 15. Implemented 3-tap FIR DAC and its 2-bit switched-resistor elements.

The SR DAC has a non-return-to-zero (NRZ) output. As shown in Fig. 15, the switches are located at the reference levels, making the on-resistance of the switches unchanged with time. However, the distributed RC parasitics due to the resistor at the virtual ground of the loop filter may exacerbate the inter-symbol interference (ISI) effects, and add loop delay. Therefore great care has been taken in the sizing and routing of the SR feedback DAC.

The FIR feedback DAC is implemented by a semi-digital approach [24]. Equally weighted coefficients were chosen for the main FIR feedback path *F(z),* whereas the coefficients of the compensation path *C(z)* were determined by using the Impulse-Invariant-Transformation (IIT).

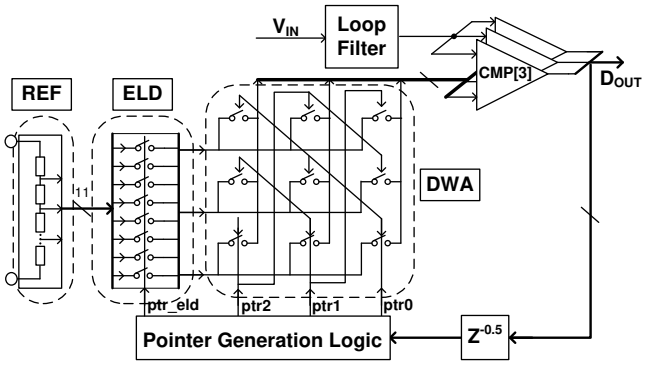


Fig. 16. The implemented reference-switching matrix for ELD and DWA.

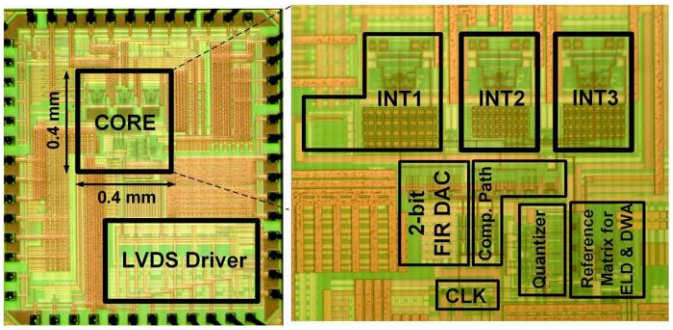


Fig. 17. Die microphotograph of the prototype [13].

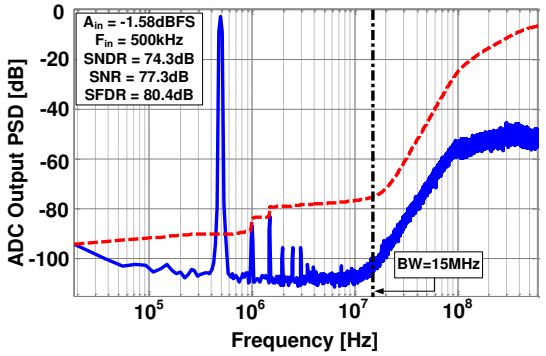


Fig. 18. Measured modulator output spectrum (65,536-point FFT with 15 averages) [13].

C. *Reference-switching Matrix for ELD and DWA*

The details of the reference-switching matrix for ELD compensation and DWA (Fig. 12) are shown in Fig. 16. The two switching matrices are merged, and controlled by their pointer generation logic.

Once an output sample of the modulator is generated, the pointer generator logic uses it to shift the reference voltage in the first matrix for ELD compensation. Then the shifted reference voltages are applied to the second matrix, and shuffled according to the pointer generated by the DWA algorithm. Both reference-switching operations are finished in a half clock period.

VI. Measurement Results

The prototype CTDSM was fabricated in a 65 nm CMOS process with MiM capacitors. It occupies an active core area of 0.16 mm^2. The chip microphotograph is shown in Fig. 17.

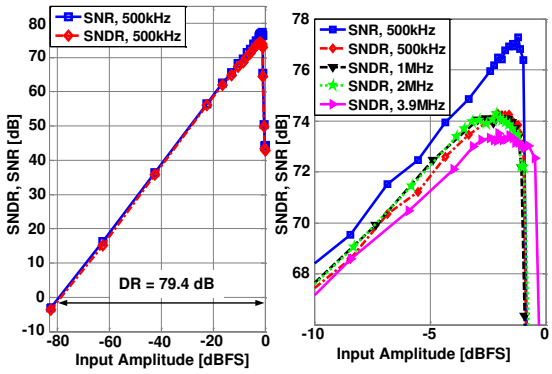


Fig. 19. Measured SNR/SNDR vs. input amplitude for (a) a 500 kHz input and (b) a magnified plot at high input amplitudes for four different input frequencies.

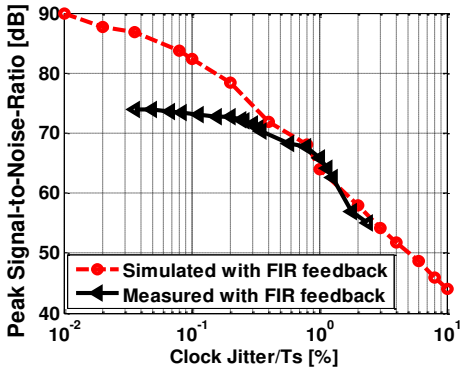


Fig. 20. Measured and simulated SNDR as functions of the clock jitter.

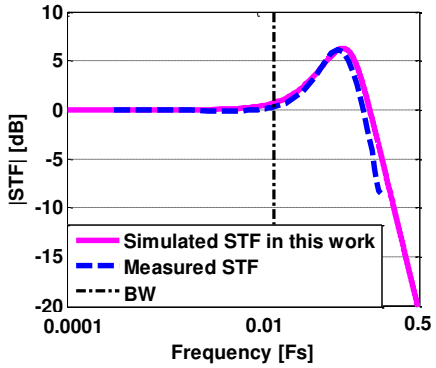


Fig. 21. Measured signal transfer function.

The die was packaged in a 40-pin QFN package.

A four-layer board is used to characterize the chip. The sine wave generated by the signal source (AWG710B) is applied to a passive band-pass filter (Allen Avionics) with a center frequency of 500 kHz, and then converted to a differential signal with a balun (Coilcraft PWB2010LB). An RF clock source (Agilent E4433B) is used to provide the clock signal of 1.2 GHz. The modulator output bit-stream, transmitted by a stubbed-series termination-logic (SSTL) interface, is captured by a logic analyzer (TLA7012), and post-processed to obtain the output spectrum.

Running at a 1.2 GHz sampling rate, the modulator dissipates 6.96 mW, of which 4.31 mW is consumed by the analog blocks, 2.17 mW by the digital blocks, and 0.47 mW

TABLE I
PERFORMANCE SUMMAY AND COMPARISON WITH PRIOR WORKS

Parameter	This Work			[8] ISSCC 2006	[26] JSSC 2011	[30] JSSC 2011	[19] JSSC 2012	[33] JSSC 2012	[31] JSSC 2012	[34] JSSC 2013	[11] ISSCC 2013	[28] JSSC 2014	[29] JSSC 2014	[32] JSSC 2015
Topology	FF-FB			FF-FB	CIFF	CIFF	FF-FB	CIFF	CIFF	CIFF	CIFF	FF-FB	MASH	CIFF
Adder required	No			No	No	Active	No	Active	Active	Active	No	No	Passive	No
ELD Comp.	R.S[7]			D.D[3]	D.D	D.F[4]	D.D	D.F	D.F	D.F	C.S[5]	PLR[6]	D.F	R.S
Technology(nm)	65			130	65	130	90	180	130	130	28	90	28	20
Area (mm^2)	0.16			1.2	0.15	1.17	0.12	0.68	0.38	1.3	0.08	0.225	45	0.1
V_{DD} (V)	1.0			1.2	1.2/1.3	1.2	1.2	1.8	1.3	1.2	1.2/1.5	1.2	0.9/1.8	1.2/1.5
F_S (MHz)	1200			640	250	640	3600	800	1000	185	640	500	3200	2184
Power (mW)	6.96	4.31 (Ana.) 2.18(Dig.) 0.47 (Ref.)		20	10.5	58	15	47.6	4	13.7	3.9	8.5	235	23
BW (MHz)	15			20	20	20	25	16	15.6	10	18	25	45	80
F_{IN} (MHz)	0.5	1	4	3.7	3.9	1	10	5	5	1	0.625	2	15	15
SNR (dB)	77.3	77.2	76.4	73.0	62.0	67.9	80.2	67	64.5	73.4	75.4	69.1	84.6	70
SNDR (dB)	74.3	74.1	73.7	74.0	60.0	63.9	73.3	65	59.8	71.9	73.6	67.5	72.6	67.5
DR (dB)	79.4	78.8	78.1	80.0	68.0	65.9	86.0	75	67.0	80	78.1	72.0	90	73
ENOB (bits)	12.0	12.0	12.0	12.0	9.7	10.3	11.9	10.5	9.7	11.7	11.9	11.8	11.8	10.9
FoM^1_{Walden} (fJ)	54.7	56.0	58.6	122.1	321.2	1110	79.4	1020	160	210	27.7	87.7	184	74.2
$FoM^2_{Schreier}$(dB)	172.7	172.1	171.4	170.0	160.8	151.1	178.2	160.3	162.9	168.6	174.7	162.2	172.9	168

1. FoM_{Walden} = Power/($2^{(SNDR-1.76)/6.02}$ x 2 x BW). 2. $FoM_{Schreier}$ = DR + 10 x $\log_{10}$(BW / P). 3. D.D: Discrete-time Differentiation as in [8]. 4. D.F: Direct Feedback as in [9].
5. C.S; Comparator Switching as in [11]. 6. PLR: Phase Lead Resistor as in [28]. 7. R.S: Reference-Switching as in this work.

by the reference voltage generators. Both the analog and digital blocks operate with 1 V supply voltages.

Fig. 18 gives the measured ADC output power spectrum density (PSD) for a -1.58 dBFS input tone at 500 kHz. (The full scale or 0 dBFS is 2 $V_{PP.}$) The sampling frequency was 1.2 GS/s. A 15-times averaged 65,536-point fast Fourier transform with a Hanning window was used for spectrum analysis. The ADC achieved a peak SNR of 77.3 dB, and an SNDR of 74.3 dB over a 15 MHz signal BW, resulting in an ENOB of 12. The measured SNR and SNDR are plotted for different input amplitudes in Fig. 19(a) for a 500 kHz input tone. A dynamic range of 79.4 dB was achieved. This validates the use of switched resistor feedback DAC with 1 V power supply. The SNDR curves for various input frequencies near the full-scale amplitude are plotted in Fig. 19(b). The peak SNDR is degraded by 0.6 dB over an input signal frequency range from 500 kHz to 4 MHz. The rms jitter of the applied clock source is around 300fs, or 0.1% of the sampling clock period.

To verify the effectiveness of the FIR feedback DAC, the measured and simulated SNDRs with FIR feedback path against the clock jitter are shown in Fig. 20. The clock jitter injection was obtained using the software interface to Agilent E4438C. The applied clock jitter is then characterized by the spectrum analyzer Agilent E4440A. It can be seen from Fig. 20 that the modulator achieves a measured SNDR larger than 70 dB when the applied rms clock jitter is less than 3 ps, which is 0.4% of the clock period. Within this range, the thermal noise contributed by the input-referred noise of the loop filter and switched-resistor feedback DAC dominates. In addition, even-order harmonic distortion is also found and contributes to the performance degradation due to the ISI effect in the feedback DAC. This results in a levelling of the noise in the measured result, which includes the thermal noise, the quantization error and the jitter-induced error. With the clock jitter larger than 0.6%T_S, the noise power induced by the clock jitter becomes dominant, and matches well with the simulated results.

The FIR feedback DAC will affect the signal transfer function (STF) of the modulator. A longer FIR filter results in a more out-of-band peaking of STF [25], which is not desirable when an out-of-band blocker is present. The measured STF, along with the simulated one is shown in Fig. 21. They coincide, and show a peaking around 6 dB, which is much lower than in prior work with FIR feedback path [19][25].

The performance of the ADC is summarized in Table I. It compares the performance of the state-of-the-art ADCs. It can be seen that the ADCs in which the active adder was eliminated achieved better power efficiency, as in [8][11][19] [29]. Furthermore, the ELD compensation without the conventional direct feedback path relaxes the requirements of the last integrator stage. This change helps to achieve an even better FoM, as in [11]. In our work, by removing the direct feedback path, the required UGBW of the opamp of the last integrator could be reduced from 1.6 F_S to 1.2 F_S. The proposed converter achieves a peak SNDR of 74.3 dB with 1 V power supply. The Walden and Schreier Figures of Merit are below 60 fJ/step and above 170 dB, respectively, which compare favorably with the state-of-the-art.

VII. Conclusion

A ΔΣ–based ultrasound beamforming receiver for biomedical imaging was described. It allows finer dynamic delay increments to achieve better image quality. A 3rd-order CT ΔΣ modulator clocked at 1.2 GHz and operating with a 1 V power supply, was described. A digital ELD compensation technique is proposed to eliminate the power-hungry adder used in earlier circuits. Also, the DWA logic is incorporated into the reference-switching matrix used in the digital ELD compensation, in order to minimize the delay in the critical path. Finally, a 2-bit 3-tap FIR filter is introduced in the feedback path, to make the modulator less susceptible to the

clock jitter. The effect of increasing the FIR tap length on the clock jitter sensitivity was analyzed. Fabricated in a 65 nm CMOS process, the prototype modulator achieves a 79.4 dB dynamic range, 77.3 dB SNR and 74.3 dB SNDR over a 15 MHz signal bandwidth, with a FoM of 58.6 fJ/conversion-step.

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