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Yung-Chou Lin, Wen-Hung Hsieh, Chung-Chih Hung

Institutions: National Chiao Tung University

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Topics: Integrator, Delta-sigma modulation, Jitter, Low-power electronics and Effective number of bits

A Continuous-Time Delta-Sigma Modulator Using Feedback Resistors

Yung-Chou Lin[1], Wen-Hung Hsieh[2], and Chung-Chih Hung[3]
Department of Communication Engineering
National Chiao Tung University
Hsinchu, Taiwan, R.O.C.

ABSTRACT

A third-order continuous-time delta–sigma comprised of Active-RC integrator and Gm-C integrator is presented. For the consideration of power, linearity and performance, the first integrator uses active-RC OpAmp and the others use Gm-C. To reduce the clock jitter sensitivity, we choose nonreturn-to-zero (NRZ) pulse shaping as our DAC type. For the realization of NTF zero optimization, we use resistors to reduce power consumption. The delta-sigma modulator is implemented in standard digital 0.18-μm CMOS process which achieves a 60-dB SNDR or 10-bits ENOB over a 1-MHz signal bandwidth at an OSR of 50. The power consumption of the continuous-time delta-sigma modulator itself is 13.7 mW from the 1.8-V supply.

Index Term — continuous-time, delta-sigma, modulator, Gm-C

INTRODUCTION

With the growth of wireless communication, there has been more focus on the analog-to-digital converter (ADC) for wireless applications. Among all ADCs, delta-sigma converters are preferable over flash and pipeline converters because they offer the most economic bandwidth and accuracy trade-off. Recently, continuous-time delta-sigma ADCs get growing interests in wireless applications for their lower power consumption and wider bandwidth as compared with the discrete-time counterparts. Because of the settling time requirement for the charge transfer between the switched-capacitor integrators, it boosts its power consumption. Therefore, they are used for low bandwidth applications. On the contrary, the sampling speed in CT isn't limited by any settling requirements. Besides, the sample-and-hold circuit in the front-end doesn't need and benefits from having inherent anti-aliasing filter. This leads to lower power consumption and less chip area. However, CT modulators suffer from the severe process-varying RC time constant, excess loop delay and clock jitter issues which require extra care. In this paper, the system level and circuit level design of this work is presented in detail, which includes the determination of the system level parameters. After that, the circuit blocks will be discussed, and the modulator is realized with a 0.18-μm CMOS technology and 1.8 V power supply voltage.

SYSTEM LEVEL DESIGN

A. System Level Parameters

First of all, to design the ΔΣ modulator is determining the system level parameters. For a CT ΔΣ modulator, the important specification is the clock jitter sensitivity. It will significantly affect the selection of the system level parameters. We usually assume that the modulator will be evaluated with a clock signal generated by the instrument. Therefore, the jitter value of the clock signal entering the modulator is determined by the quality of the instrument signal. In this work, the RMS value of the target jitter tolerance is 15 ps to satisfy the specification, as shown in Figure. 1.

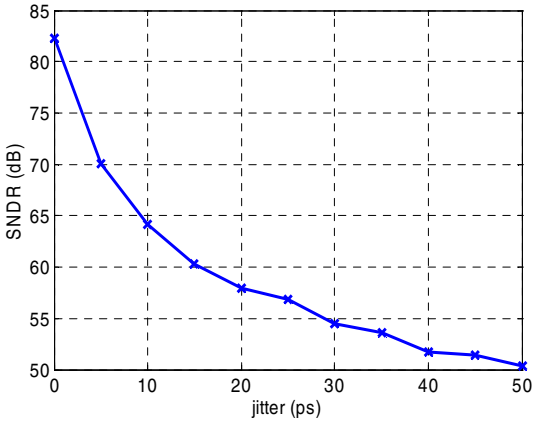

FIGURE. 1 SIMULATED SNDR AS A FUNCTION OF CLOCK JITTER

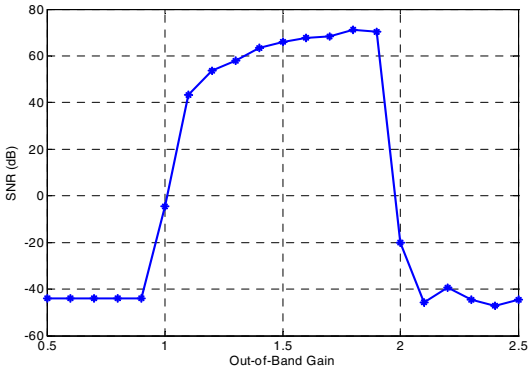

FIGURE. 2 SIMULATED SNR AS A FUNCTION OF OUT-OF-BAND GAIN FOR SINGLE BIT

Besides, the system level parameters include the oversampling ratio (OSR), the loop filter order (L), the number of the quantizer level (M) and the aggressiveness of the noise shaping which is

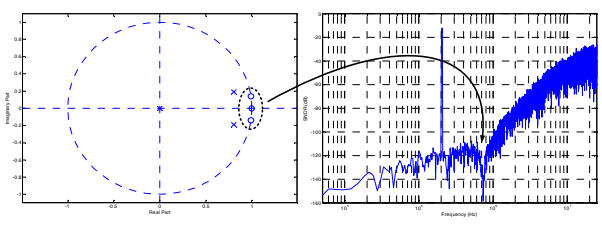

FIGURE. 3 OPTIMAL THIRD–ORDER NTF FOR OSR=50

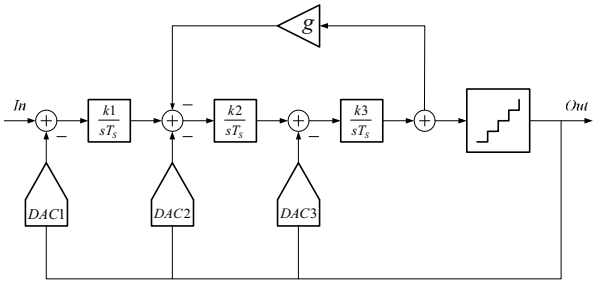

FIGURE. 4 THE SYTEM ARCHITECTURE OF THIS WORK

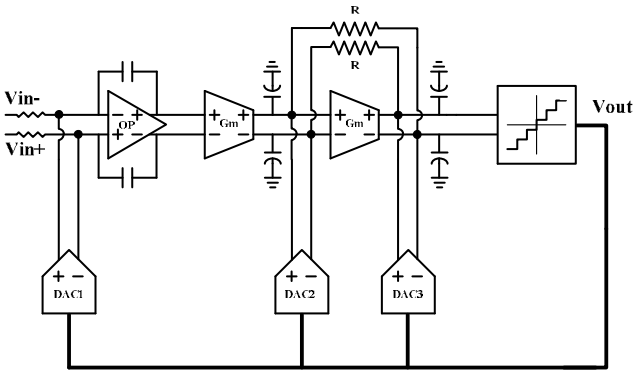

FIGURE. 5 SIMPLIFIED CIRCUIT BLOCK OF THIS WORK

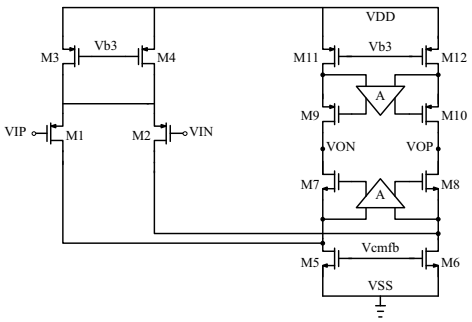

FIGURE. 6 SCHEMATIC OF GAIN-BOOSTING FOLDED-CASCODE OPAMP

determined by the maximum out-of-band quantization gain. Considering the gain-bandwidth requirement of the OpAmp with acceptable power consumption and the clock jitter sensitivity, we choose 50 as our OSR value. The power consumption of the quantizer increases proportionally to the number of quantization levels. Therefore, we determine the number of the quantizer be single. On the other hand, increasing the loop filter order is cheap, but the loop stability issue limits the loop order, so we choose 3 as our loop order. Besides, the aggressiveness of the noise shaping is also limited by the stability issue. After MATLAB Control System toolbox simulation, as shown in Figure. 2, we choose 1.6 as our out-of-band gain. Based on these requirements, a large amount of simulations were performed by using the MATLAB toolbox to explore the parameter space [1].

B. NTF Zero Optimization

When designing wide band ΔΣ modulator, a technique is usually used. That is separating zeros on the unit circle, which means it spreads over the signal range, as shown in Figure. 3. By shifting the two zeros from dc (ω = 0) to an optimized value, we can get the 8 dB SQNR improvement [2].

In Figure. 4, we show the architecture of CT ΔΣ modulator using feedback resistors. The loop filter architecture we use is general feedback structure.

CIRCUIT IMPLEMENTATION

A. Loop Filter

The third-order loop filter of this work design is implemented with CRFB architecture, as shown in Figure. 5. The first stage is an active-RC integrator and the following resonators are realized by Gm-C integrators and the resistor. The role of the resonators is to shift the poles of the loop filter to optimum non-zero frequencies in order to reduce in-band quantization noise and get better performance, as mentioned before. There are two types of commonly used continuous-time integrators: active-RC integrators and Gm-C integrators. In this design, the first stage uses an active-RC integrator rather than the Gm-C integrator for its superior linearity. Gm-C integrators are chosen for the two resonators to save power.

B. First Stage — Active-RC integrator

The OpAmp in the active-RC integrator uses a folded-cascode topology with a gain enhancement method by adding additional stages to increase DC gain. This method is called gain-boosting [3] [4]. Compared with the telescopic OpAmp and the two-stage OpAmp, the folded-cascode OpAmp achieve the tradeoff between the power consumption and output swing in this 0.18-μm CMOS design. Figure. 6 shows the schematic of the gain-boosting folded-cascode OpAmp used in this design.

C. Following Stage — Gm-C integrator

With the exception of the first stage integrator, the following two integrators are implemented with Gm-C integrators to save power. A folded-cascode architecture is used with source degeneration resistor, as shown in Figure. 7. It achieves the required linearity and it has wider output swing as well.

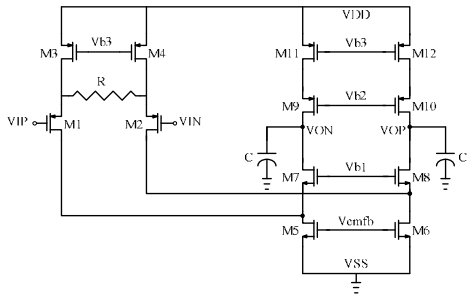

FIGURE. 7 SCHEMATIC OF GM WITH SOURCE DEGENERATION RESISTOR

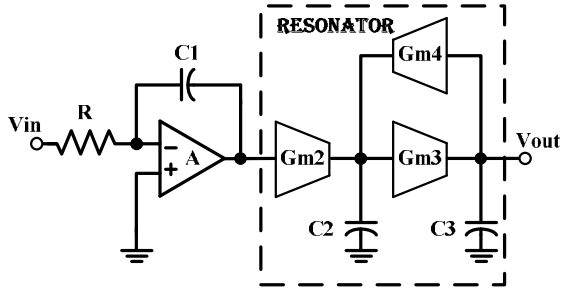

FIGURE. 8 THE SIMPLIFIED SCHEMATIC OF LOOP FILTER

D. Feedback Resistors

As previous section mentioned, the role of the resonators is to shift the poles of the loop filter to optimum non-zero frequencies in order to reduce in-band quantization noise and get more performance. In the circuit level, we simplify Figure. 4 as Figure. 8 to express. We can get the transfer function $\frac{V_{out}}{V_{in}} = -\frac{\frac{Gm_2Gm_3}{RC_1C_2C_3}}{s\left(s^2+\frac{Gm_3Gm_4}{C_2C_3}\right)}$. Therefore, we get three poles $s=0$ and $s^2+\frac{Gm_3Gm_4}{C_2C_3}=0$, and find the shift frequency $f_Z=\frac{1}{2\pi}\sqrt{\frac{Gm_3Gm_4}{C_2C_3}}$. In general, the implementation of Gm_4 is gm cell which is the active component. Considering the power consumption, we replace gm cell with the resistor, that is, $Gm=\frac{1}{R}$ to save power.

E. Tuning Circuit

The time constant shift due to process variations in practical continuous-time circuits can degrade system performance to an unacceptable level. For CT ΔΣ modulators, ±20% variation is more than enough to drive the modulator into unstable operation. To solute this issue, we apply a capacitor array tuning method to adjust the time constants, as shown in Figure. 9 [5]. The capacitors in the arrays are binary-sized except the always-in-use capacitors. This sizing method is to provide constant tuning step with the least number of capacitors and to ease layout. The 4-bit digital control codes are fed externally to choose which capacitors to use.

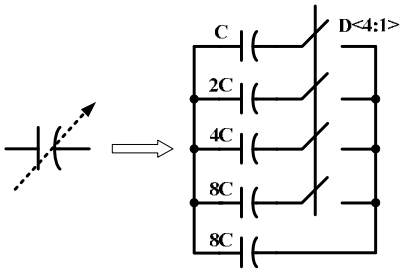

FIGURE. 9 TUNABLE CAPACITOR ARRAY

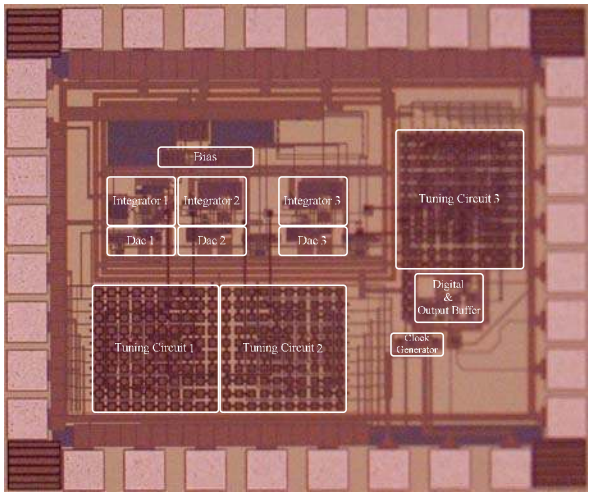

FIGURE. 10 DIE PHOTO OF THIS WORK

The total capacitor value in use is: $C_{in\ use}=8C+k\cdot C$, k = 0~15. The maximum available capacitance in the array is $C_{\max}=23C$, and the minimum available capacitance in the array is $C_{\min}=8C$. For normal operation, the capacitor value is $C_{normal}=16C$. Therefore, the tuning range of the integration capacitor arrays is $\frac{23C-16C}{23C}\sim\frac{8C-16C}{16C}$, that is, +43.75% ~ -50%, which suffices for the requirements of this modulator according to 20% capacitor process variations.

MEASURED RESULTS

The chip is fabricated in a 0.18-μm CMOS process. The die photo is shown in Figure. 10. The total area, including pad is 1.14 x 0.95 mm^2. The captured output digital data is windowed by a Hann window and a Fourier transformation is applied using Matlab. The measured peak SNDR is 60 dB as shown in Figure. 11. The measured SNDR versus the relative input amplitude is shown in Figure. 12. The power consumption measured with 100 MHz sampling frequency is 13.7 mW. The measured performance is summarized in Table I.

To quantitatively evaluate the efficiency among power dissipation, signal bandwidth, and SNDR. We use the formulas for the effective number of bits (ENOB) and the figure-of-merit (FOM) as described below,

TABLE I
PERFORMANCE COMPARISON BETWEEN REPORTED DESIGNS AND THIS WORK

Refs	*SNDR*	*Signal Bandwidth*	*OSR*	*Architecture*	*Process*	*Power Supply*	*Die Size*	*Power Dissipation*	*FOM (pJ/conv)*
1999 JSSC [6]	82 dB	1.1 MHz	24	MASH 2-1-1	0.5-µm CMOS	3.3 V	5.06 mm^2	200 mW	8.84
2000 JSSC [7]	79 dB	1.1 MHz	24	MASH 2-2-2	0.35-µm CMOS	3.3 V	4.3 mm^2	248 mW	15.48
This work simulation	67 dB	1 MHz	50	3^{rd}-order	0.18-µm CMOS	1.8 V	1.08 mm^2	13.6 mW	3.717
This work measured	60 dB	1 MHz	50	3^{rd}-order	0.18-µm CMOS	1.8 V	1.08 mm^2	13.7 mW	8.4

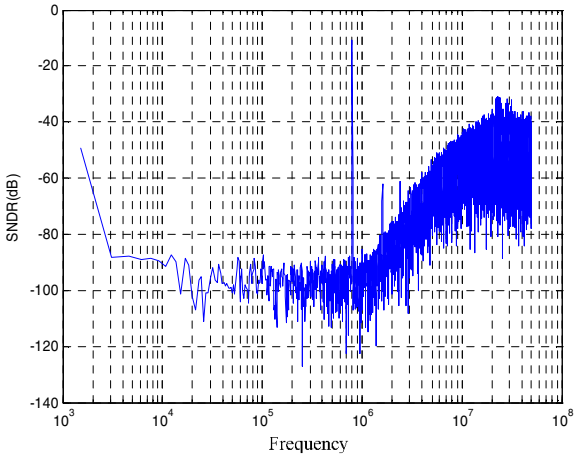

FIGURE. 11 OUT SPECTRUM OF THE MEASURED RESULT

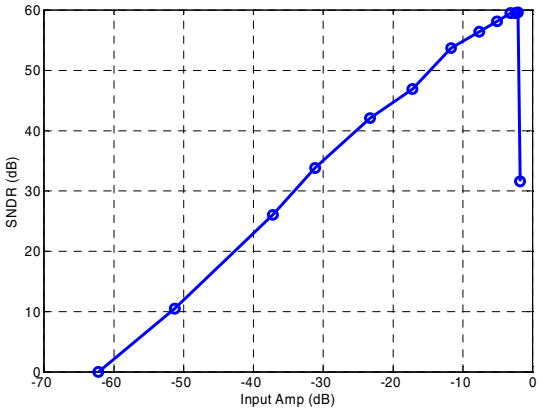

FIGURE. 12 SNDR VERSUS NORMALIZED INPUT AMPLITUDE

$$FOM = \frac{Power}{2 \times BW \times 2^{ENOB}} \quad (1)$$

and smaller FOM is better.

Table I lists previously reported SC delta-sigma modulators about 1 MHz signal bandwidth. Compared with them, the SNDR is not the best, but FOM is top. Therefore, we can find continuous-time delta-sigma get growing apply to wireless applications for their lower power consumption and wider bandwidths as compared with the discrete-time counterparts.

CONCLUSIONS

A continuous-time delta-sigma modulator using feedback resistors is presented. This work is designed using 0.18-µm CMOS technology in 1.8 V power supply voltage. With a 100 MHz clock, this modulator achieves 60 dB SNDR and 60 dB dynamic ranges with a 1MHz signal bandwidth. A technique of using feedback resistors is realized, the low jitter clock generator have the CT ΔΣ modulator not be sensitive to clock jitter, and tuning circuits are employed to calibrate the time constant shift due to process variations.

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