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# A Continuous-Time $\Sigma\Delta$ ADC With Increased Immunity to Interferers

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**Abstract**—Receivers are being digitized in a quest for flexibility. Analog filters and programmable gain stages are being exchanged for digital processing at the price of a very challenging ADC. This paper presents an alternative solution where the filter and programmable gain functionality is integrated into a  $\Sigma\Delta$  ADC. The novel filtering ADC is realized by adding a high-pass feedback path to a conventional  $\Sigma\Delta$  ADC while a compensating low-pass filter in the forward path maintains stability. As such, the ADC becomes highly immune to interferers even if they exceed the maximum allowable input level for the wanted channel. As a consequence, the ADC input range can be programmed dynamically to the level of the wanted signal only. This results in an input-referred dynamic range of 89 dB in 1-MHz bandwidth and an intentionally moderate output signal-to-noise-and-distortion ratio of 46–59 dB (depending on the programmed gain). The merged functionality enables a better overall power/performance balance for the receiver baseband. The design consumes less than 2 mW and active area is 0.14 mm<sup>2</sup> in a 0.18- $\mu$ m digital CMOS technology.

**Index Terms**—Analog-to-digital conversion, Bluetooth, channel filter, continuous time, digitization, IF conversion, interferer, receiver, sigma-delta ADC, sigma-delta modulator.

## I. INTRODUCTION

RECEIVERS for wireless communications are being digitized in the sense that analog selectivity is being exchanged for digital processing and the analog-to-digital converter (ADC) is gradually moving toward the antenna. Wireless interconnectivity (for example, Bluetooth, ZigBee, and IEEE802.11x), in particular, seems a prime candidate for adopting a full-digital implementation of the receiver baseband. Compared to mobile communication, sensitivity and interferer levels are moderate. At the same time, cost targets are so aggressive that full integration in a standard digital CMOS technology becomes a strong prerequisite.

A conventional highly analog Bluetooth receiver is depicted in Fig. 1(a). Bluetooth operates in the ISM band at 2.4 GHz with 1-MHz channels using GFSK modulation. A low-IF receiver with IF = 500 kHz is considered. The baseband part of the receiver consists of a cascade of filter sections and programmable gain amplifiers (PGAs). The latter limit the signal

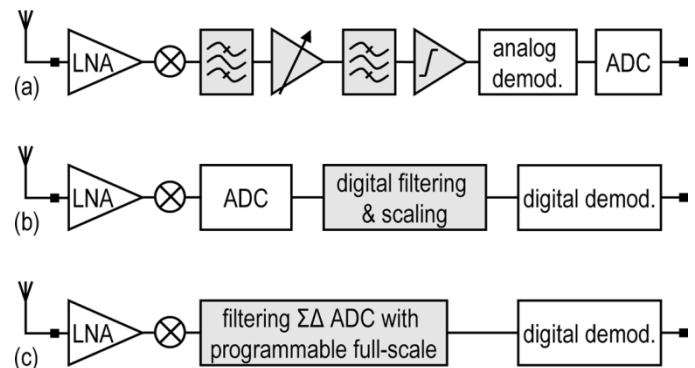


Fig. 1. Receiver with (a) full-analog, (b) full-digital, and (c) mixed-signal signal conditioning.

to a predefined level. The bits are recovered by further analog demodulation (for example, using a zero-crossing detector [1] or a frequency discriminator [2]) and by consecutive quantization. All analog stages add noise and distortion. Moreover, their offset and gain or phase error accumulates and many calibration and control loops are needed for correction. This increases design time, complexity, and risk.

Fig. 1(b) presents a full-digital receiver architecture [3]. No analog filters or (programmable) gain amplifiers are present. All signal conditioning (i.e., filtering and scaling of word lengths) and demodulation takes place in the digital domain. This receiver architecture is highly flexible and future proof; for instance, it can easily be adapted to accommodate extended modulation schemes or multistandard operation. In addition, it is ideally suited for integration in mass-production digital CMOS technology. The burden of this solution, however, is on the ADC. The absence of preceding channel filtering implies that the input signal of the ADC consists of both the wanted channel and, possibly, a wide spectrum of interferer channels. As a consequence, both the bandwidth and the dynamic range of the ADC need to be very high. More challenging still, the ADC must be extremely linear to prevent the risk of intermodulation distortion of large interferers corrupting the reception of a weak wanted channel. In a summary, a full-digital receiver results in a power-hungry ADC. Alternative ADC topologies are required to maintain a competitive power/performance balance while pursuing digitization.

In answer to this, this paper presents a  $\Sigma\Delta$  ADC with merged filtering and PGA [Fig. 1(c)]. It combines well-known features of a continuous-time  $\Sigma\Delta$  ADC, such as the anti-aliasing behavior and the low power consumption, with a filtering signal

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transfer function (STF). This filtering STF makes the ADC immune to interferers even if they exceed the maximum allowable input level for the wanted channel. The merged design is easier to implement than the conventional baseband of Fig. 1(a) while it provides the same functionality. Compared to the full-digital architecture of Fig. 1(b), it offers similar flexibility. Area and power consumption are less than those of the state-of-the-art implementations in Fig. 1(a) and (b).

Section II discusses the potential of a generic continuous-time  $\Sigma\Delta$  ADC for enabling a highly digital receiver, i.e., its capability for handling interferers is analyzed. The stable input range of the  $\Sigma\Delta$  ADC is identified as the dominant limitation on the allowable interferer level and on the power efficiency of the receiver baseband. It can be improved by proper design of the STF of the ADC. This is the subject of Section III. There, the novel concept of a filtering  $\Sigma\Delta$  ADC is introduced: instead of moving the analog selectivity [Fig. 1(a)] into the digital domain [Fig. 1(b)], it can be integrated in the ADC [Fig. 1(c)]. The implementation and circuit aspects are detailed in Section IV. In Section V, the experimental results are presented and it is shown that the filtering  $\Sigma\Delta$  ADC yields a better overall power/performance balance than the solutions of Fig. 1(a) and (b). Finally, in Section VI, conclusions are given.

## II. $\Sigma\Delta$ ADCs AND RECEIVER DIGITIZATION

As the ADC moves toward the antenna, it needs to handle a large signal range and bandwidth. Fig. 2(a) depicts the spectrum of an example input signal. It consists of a small wanted channel in the bandwidth of 0–1 MHz, a slightly stronger adjacent interferer channel, and two far-off interferer channels. The latter have been chosen at worst case frequencies; i.e., distortion components due to third-order intermodulation ( $IM_3$ ) fall into the wanted channel.

Single-bit continuous-time  $\Sigma\Delta$  ADCs are ideal candidates for handling this type of input spectrum and for enabling receiver digitization. First, these ADCs achieve a large dynamic range (DR) and excellent linearity while their power consumption remains at record low. This is demonstrated by the performance of various published designs [4]–[7]. Second, the  $\Sigma\Delta$  ADC uses oversampling. In consequence, a large bandwidth of interferers can be applied at its input without aliasing. At the output [Fig. 2(b)], the interferers are present together with the shaped quantization noise while the resolution within the wanted channel remains high. The key question is: “*How large may interferers grow before noise or distortion starts increasing in the bandwidth of the wanted channel?*” Various limitations on the allowable interferer level are discussed in Section II-A. Next, in Section II-B, an intuitive explanation of the consequences for the overall power/performance balance of the highly digitized receiver is given.

### A. Allowable Interferer Level for $\Sigma\Delta$ ADCs

In the above, it has been explained that interferers can be applied to the  $\Sigma\Delta$  ADC. As the interferers exceed a certain limit, though, they cause distortion, spurious tones, and an increase in noise in the wanted channel. This limit is due to various effects and can be frequency dependent.

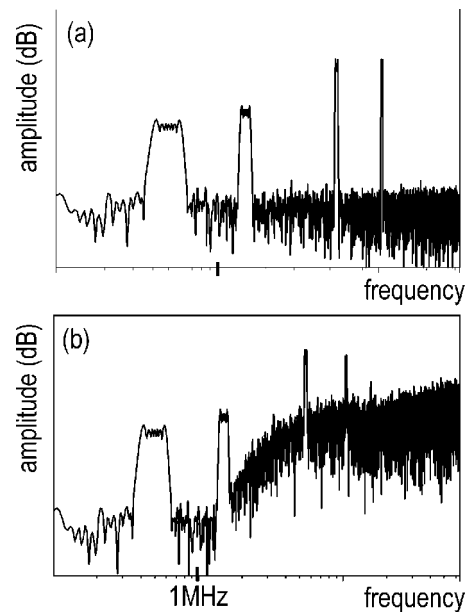


Fig. 2. (a) Example input spectrum and (b) corresponding output spectrum of the  $\Sigma\Delta$  ADC.

1) *Intermodulation Distortion*: As introduced above, large interferers may induce  $IM_3$  distortion in the bandwidth of interest. Similarly, intermodulation of interferers and shaped quantization noise causes an increase in the noise in this bandwidth. In a  $\Sigma\Delta$  ADC, the dominant nonlinearities are due to the feedback path and the input stage. In the feedback path, excellent linearity can be achieved using a single-bit DAC in combination with return-to-zero pulses. Distortion in the input stage of the ADC remains critical and normally requires a large bias current. This is further detailed in Section IV where the circuit design is discussed. Literature shows that  $IM_3$  distortion well below  $-80$  dBc should be feasible for a typical input swing (for example,  $0.5 V_{\text{rms}}$ ) [4]–[7]. Normally, the dominant nonlinearity (i.e., the transconductance of the input stage) is rather frequency independent and similar linearity is expected at the frequency of the interferers. Hence, in view of the quoted linearity, intermodulation distortion is not expected to be the main limitation on the allowable interferer level.

2) *Aliasing*: In a sampled-data system, aliasing occurs when interferers are applied at a frequency near the clock frequency. If the aliased components fall into the bandwidth of the wanted channel, the available DR deteriorates. Compared to ADCs sampled at the Nyquist rate, the aliasing problem is less severe for a  $\Sigma\Delta$  ADC; i.e., fewer frequency bands fold back into the bandwidth of interest because of the oversampling.

Continuous-time implementations, in particular, benefit from an additional characteristic. In these designs, sampling occurs inside of the loop. In consequence, the interferer is attenuated before being sampled. Moreover, the remaining low-frequency alias is counteracted by the preceding loop gain at this frequency. Because of the large low-frequency gain of the loop filter, aliasing should not be the dominant limitation on the allowable interferer level. A quantitative analysis of the anti-aliasing suppression in a continuous-time  $\Sigma\Delta$  ADC is conducted in [7].

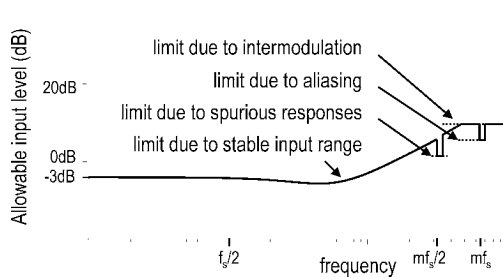


Fig. 3. Example curve of the allowable input level over frequency without causing an increase in noise or distortion in the wanted channel.

3) *Spurious Responses*: If a behavioral model of a  $\Sigma\Delta$  ADC is simulated, tones appear in the conversion bandwidth when specific interferers (especially near  $mf_s/2$ ,  $mf_s/4$ , etc.) are applied [8]. These tones are due to a strong correlation between the interferer signal and the  $\Sigma\Delta$  quantization noise and consequent intermodulation in the quantizer. If a small, preferably modulated, wanted signal or white noise is added—which is the case in an actual application—decorrelation occurs and the tones disappear. Also, the use of a high-order loop filter improves decorrelation.

4) *Stable Input Range*:  $\Sigma\Delta$  modulators suffer from large-signal instability: the digital-to-analog converter (DAC) cannot feed back a large enough signal in time to compensate for the input signal (i.e., the phase and the gain margin of the loop become too small). The error signal and the internal signals in the loop (i.e., the outputs of the various integrators) therefore grow and further reduce the gain and the phase margin, resulting in instability. For a further discussion on stability, the reader is referred to [9]–[11]. Well-designed single-bit modulators typically achieve a maximum modulation depth of about 70%, i.e.,  $-3$  dB below digital full-scale. This modulation depth represents a good compromise between aggressive noise shaping and stability. The input level  $V_{in,max}$  corresponding to this maximum DAC output of  $0.7 V_{DAC}$  is called the stable input range.  $V_{in,max}$  is frequency dependent and can be calculated if the STF of the modulator is known:

$$V_{in,max}(j\omega) = \frac{0.7 V_{DAC}}{STF(j\omega)}. \quad (1)$$

In many practical designs, the stable input range of the  $\Sigma\Delta$  ADC is the dominant limitation on the allowable interferer level. This is understood from the example graph of Fig. 3, which summarizes the above discussion. The curve indicates the allowable interferer level over frequency such that noise and distortion do not increase within the bandwidth of the wanted channel. The curve and the numbers are illustrative only. For most frequencies, the dominant limitation is due to large-signal instability. Far-off interferers are restricted by  $IM_3$  or aliasing considerations. Discrete-tone interferers near  $mf_s/2$  may cause spurious responses.

### B. Consequences for Receiver Digitization

The above indicates that a single-bit continuous-time  $\Sigma\Delta$  ADC can be used without preceding analog filters and PGAs and, therefore, is indeed a good candidate for enabling highly digitized receivers [4]–[7].

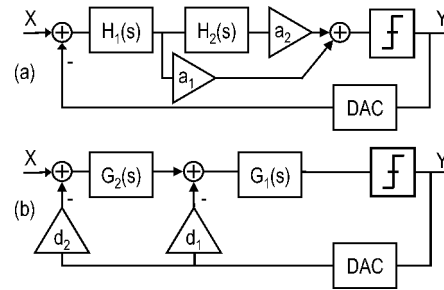


Fig. 4.  $\Sigma\Delta$  ADC with (a) feedforward and (b) feedback stability compensation (for  $N = 2$ ).

In a straightforward digitization approach, i.e., simply shifting the ADC to the antenna, the ADC is designed to handle the entire input signal, including interferers and, essentially, its bandwidth and DR are partly “wasted” to the interferers. Instead, we present a  $\Sigma\Delta$  ADC with increased interferer immunity. As a consequence, the input range of the ADC can be adapted dynamically to the wanted channel only. This yields a better overall power/performance balance for the receiver.

### III. STF DESIGN FOR INTERFERER IMMUNITY

Feedforward and feedback compensation [Fig. 4(a) and (b), respectively] are two common techniques for guaranteeing stability when implementing a high-order loop filter. The feedforward technique enables an inherently low-power modulator while feedback compensation results in a favorable STF in view of immunity to interferers. Sometimes, the combination of feedforward and feedback paths is implemented as a tradeoff. Here, the feedforward topology is modified to improve the STF while safeguarding the low power consumption. This results in a  $\Sigma\Delta$  ADC with explicit filtering, as presented at the end of this section.

#### A. $\Sigma\Delta$ ADC With Feedforward Compensation

Fig. 4(a) shows the use of an  $N$ th order loop filter (for  $N = 2$ ) with feedforward compensation. This topology is very common and was implicitly understood in Figs. 2 and 3. At high frequencies, the path  $a_1 H_1(s)$  overrules the other contribution and ensures stability. A second characteristic is the fact that only the error signal (i.e., the difference between input and output) is fed into the loop filter. This signal consists primarily of quantization noise and is rather small. This is an additional reason why  $H_1(s)$  can have high gain. As a consequence, the bias current of the consecutive stages can be low because, in a closed-loop configuration, their noise and distortion is suppressed by the preceding gain. Hence, the feedforward topology enables a low-power design.

The STF of this topology is depicted in Fig. 5. It is flat within the conversion bandwidth, shows some overshoot for adjacent channels, and features first-order filtering beyond the unity-gain frequency  $f_{ug}$  of the loop. The overshoot is due to the fast transition from  $N$ th-order to first-order behavior of the open loop gain. It implies that the adjacent channels are amplified toward the output. Considering that the allowable output modulation depth is fixed, this means that the stable input range for adjacent channels is smaller than that for the wanted channel.

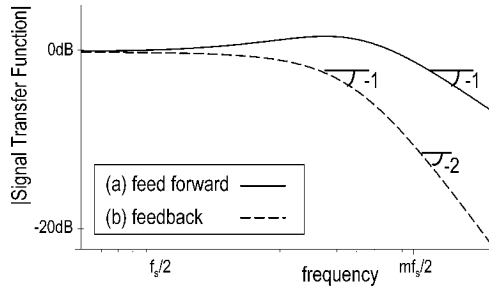


Fig. 5. Signal transfer function of a  $\Sigma\Delta$  ADC with (a) feedforward and (b) feedback stability compensation (for  $N = 2$ ).

### B. $\Sigma\Delta$ ADC With Feedback Compensation

In the feedback topology [Fig. 4(b)] stability is provided by the inner loop  $d_1 G_1(s)$ . First, it overrules the outer loops at high frequencies by having the highest gain. Second, the entire output signal, consisting of both the input signal and the quantization noise, is fed back to every internal node of the filter and each integrator must provide a strong compensating signal. In order to maintain an acceptable signal swing at the output nodes of the various integrators, the unity-gain frequencies must be scaled down. For the above two reasons, the input stage can only have moderate gain. As a consequence, the following stages in the loop filter do contribute to the overall noise and distortion and their bias current remains significant. This is especially true if a high-order loop filter is used; the unity-gain frequency of the first integrator can then be so low as to cause attenuation of the wanted signal.

Fig. 5 shows the STF of this topology. Again, the transfer is flat within the conversion bandwidth, but for adjacent channels it features filtering of order  $N - 1$  ( $N = 2$ ) and beyond  $f_{ug}$  filtering of order  $N$  results. The cut-off frequency of the STF depends on the loop filter design: it can only be shifted to a lower frequency at the expense of reduced noise shaping.

The filtering STF implies that large interferers can be applied without causing saturation of the DAC and consequent instability. Also, the feedback topology achieves a higher suppression of aliases and is less prone to spurious responses to a discrete tone interferer. This is intuitively understood from the fact that the interferer first passes through  $N$  filter sections and only then is it sampled in the quantizer, causing the alias or spurious problem. (In the feedforward case, a high-frequency input signal only passes through the first filter section before being sampled.) In conclusion, the feedback topology features good immunity to interferers at the price of significantly higher power consumption than a feedforward design.

### C. $\Sigma\Delta$ ADC With Explicit Filtering

The qualities of the feedforward and the feedback design are united in a  $\Sigma\Delta$  ADC with explicit filtering; i.e., this ADC combines a low power consumption with a good interferer immunity. The ADC is based on a feedforward implementation to which a low-pass filter  $H_{LPF}(s)$  and a compensating high-pass filter  $H_{HPF}(s)$  are added. Fig. 6(a) and (b), respectively, show the

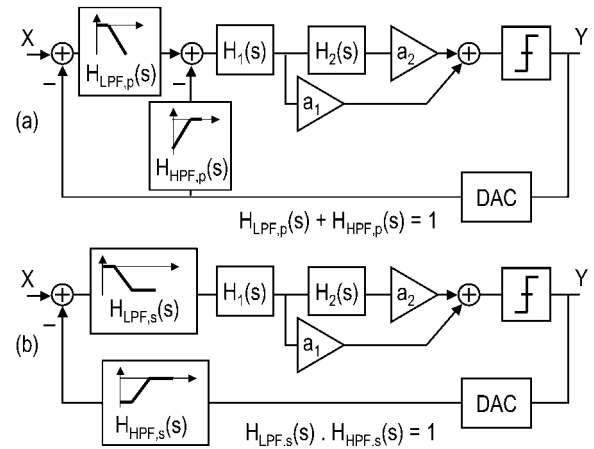


Fig. 6.  $\Sigma\Delta$  ADC designed for interferer immunity: (a) parallel and (b) series topology.

parallel and the series configuration for the added filters. The added filters are complementary in the sense that

$$H_{LPF,p}(s) + H_{HPF,p}(s) = 1 \quad (2)$$

and

$$H_{LPF,s}(s) \cdot H_{HPF,s}(s) = 1. \quad (3)$$

Ideally, the loop gain remains the same as for the conventional ADC, and the noise shaping and the stability are the same as well. In practice, a mismatch between both filters will affect the stability of the loop. A minor additional phase margin must be taken into account in the stability analysis but, for common mismatch values, this issue is not at all restricting. For example, it can be calculated that a mismatch of 5% would cause a phase shift of less than  $0.3^\circ$  at half the sample rate.

The STFs of the presented ADCs are calculated below.  $H(s)$  is the loop filter transfer of the conventional feedforward ADC; i.e., the transfer from the input of  $H1(s)$  to the input of the quantizer in Fig. 6(a) and (b). Coefficients  $c$  and  $d$  indicate the linearized quantizer and DAC gain, respectively.

$$\begin{aligned} \text{STF}_p(s) &= H_{LPF,p}(s) \frac{cH(s)}{1 + cd [H_{LPF,p}(s) + H_{HPF,p}(s)] H(s)} \\ &= H_{LPF,p}(s) \text{STF}_{\text{feedforwardADC}}(s) \end{aligned} \quad (4)$$

and

$$\begin{aligned} \text{STF}_s(s) &= H_{LPF,s}(s) \frac{cH(s)}{1 + cd H_{LPF,s}(s) \cdot H_{HPF,s}(s) H(s)} \\ &= H_{LPF,s}(s) \text{STF}_{\text{feedforwardADC}}(s). \end{aligned} \quad (5)$$

These ADCs add explicit low-pass filtering  $H_{LPF}(s)$  to the STF of the feedforward design. Unlike the feedback topology, the order and the cut-off frequency of the filtering STF can be chosen completely independently of the loop filter  $H(s)$ .

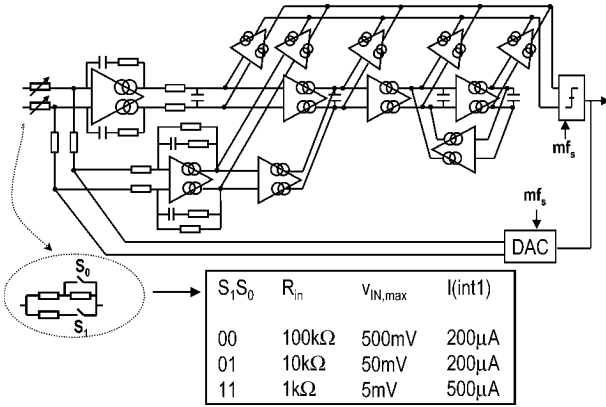


Fig. 7. Block schematic of the implemented filtering  $\Sigma\Delta$  ADC with programmable gain.

Hence, the STF can be optimized without compromising on the noise shaping. This is a key asset of this topology.

Compared to the original feedforward design, the integration of the additional filters also improves the suppression of aliases and the behavior in terms of spurious responses: the interferers are suppressed more before being sampled in the quantizer where the problems would originate. Hence, this filtering ADC design features good overall immunity to interferers.

The power consumption of the filtering ADC barely exceeds that of the feedforward ADC on which it is built. This is discussed in the next section along with some implementation aspects.

#### IV. IMPLEMENTATION OF THE FILTERING $\Sigma\Delta$ ADC

The above principle is applied to a fourth-order 1-bit continuous-time  $\Sigma\Delta$  ADC. First, the  $\Sigma\Delta$  architecture is described. Next, the circuit design is detailed. Finally, programmable gain control is added in order to exploit the filtering STF optimally.

##### A. Architecture

The implementation is built on a conventional design with a fourth-order loop filter and one notch at the edge of the 1-MHz conversion bandwidth. It is sampled at 64 MHz. A simple first-order low-pass filter with  $f_{-3dB} = 3$  MHz and the compensating high-pass filter are added (Fig. 7). Compared to Fig. 6(a), the first integrator stage of the loop filter is shifted in front of the summation point and is duplicated. Hence, a passive implementation of  $H_{LPF}(s)$  becomes possible. In the parallel feedback path, the cascade of the integrator and the high-pass filter equals a low-pass filter, resulting in an easy implementation. Notice that here an active implementation is preferred over a passive one: the active stage supplies the signal-dependent current to the integration capacitor while the DAC reference has a constant load. A passive implementation would pollute the DAC reference (which is being shared with other circuits) with a signal-dependent load.

##### B. Circuit Design

First, the building blocks belonging to the conventional design are presented. To a large extent, these are based on circuits

presented in [7]. Here we focus on the performance with respect to interferers. Next, the characteristics of the added filters are discussed.

1) *Conventional ADC*: In the design of the conventional  $\Sigma\Delta$  ADC in particular, the first stage is of utmost importance to the overall performance. It consists of an operational transconductance amplifier (OTA) in a negative feedback configuration. A large transconductance is favorable both for noise and distortion of the ADC. Based on [9], the  $IM_3$  can be calculated as a function of the input signal  $V_{IN}$ , of  $g_m$  and  $V_{GT}$  of the input transistors of this stage and of the resistances  $R_{in}$  and  $R_{FB}$  (see Fig. 7):

$$IM_3 = \frac{3}{16} \left( \frac{\hat{V}_{IN}}{V_{GT}} \right)^2 \frac{1}{g_m^3 R_{in}^3} \left( 1 + \frac{R_{in}}{R_{FB}} \right). \quad (6)$$

For a fixed bias current,  $IM_3$  improves quadratically with  $V_{GT}$  while it is cubic in  $g_m$ . Hence, the input transistor should be biased near weak inversion to achieve lowest distortion. In that case, the linear input range, i.e.,  $V_{GT}$ , decreases but  $g_m$  grows. A larger  $g_m$  results in a smaller error signal at the virtual ground input. Both effects are counteracting but the latter is dominant because of the cubic relation. Hence,  $g_m/I = 10$  is chosen (with the bias current  $I = 500 \mu A$ ).<sup>1</sup>

Beyond the unity gain frequency  $f_{ug}$  of the loop

$$IM_3 = \frac{3}{32} \left( \frac{\hat{v}_{IN}}{v_{GT}} \right)^2. \quad (7)$$

Hence,  $V_{GT}$  should not be too small either to prevent intermodulation of interferers at high frequencies from causing spurious components within the conversion bandwidth.

Furthermore, the input stage must provide a virtual ground node to sum the input current and the feedback current. The virtual ground node must be guaranteed over a wide bandwidth because interferers can be applied in about 80 MHz. (This is the Bluetooth band that passes through the antenna filter.) Also, the feedback signal contains a lot of energy at high frequencies. The bandwidth of the input stage must be large compared to that of the input signal and that of the feedback signal. This favors the use of single-stage solutions such as a telescopic or a folded cascode topology.

A folded cascode stage can accommodate a large output swing for the integration, while a telescopic cascode only takes a minimum number of current branches. Because the first stage dominates in the overall current consumption (due to the high  $g_m$ ), the latter argument prevails.

Fig. 8(a) shows the schematic of the first integrator in the loop filter. All current sources are cascoded to improve the output impedance and to decrease the influence of its nonlinearity. The NMOS current source is degenerated, with transistors in the triode region providing the output common-mode control. The control relies on matching with a replica bias circuit. The input common mode is set by the DAC output. Noticeably, a differential output swing of  $0.5 V_{DD}$  is possible even though many devices are stacked in the circuit.

<sup>1</sup>When biasing the input transistors in weak inversion  $V_{GT}$  should be replaced by  $nkT/q$  in the formulas.

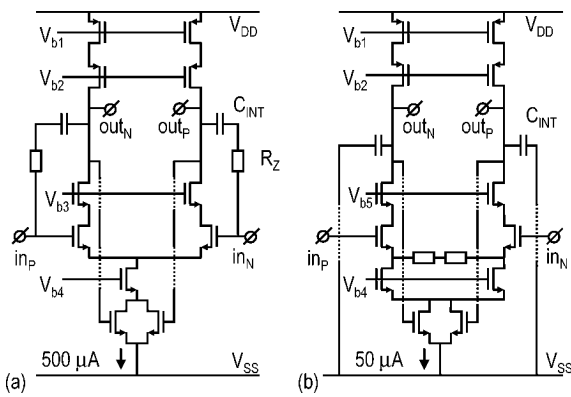


Fig. 8. Implementation of (a) first integrator and (b) following integrators.

The second and higher sections of the loop filter consist of a scaled-down copy of the first stage [Fig. 8(b)]. Because their noise and distortion is suppressed by the preceding gain in the loop, they can be biased at a current that is 10 times lower. Unlike in the first stage, the input of these OTAs is not a virtual ground node. Instead, there can be a large signal swing on the input node since it is connected to the output of the previous integrator. The transconductances are degenerated to increase their linear input range. As a consequence, all time constants of the loop filter are set by  $RC$  products and therefore match well.

The feedforward coefficients are based on degenerated differential pairs. These feed their output current directly into a current-mode latch that also serves as a summing node. The single-bit output code is fed back to the input by a resistive DAC: the resistor  $R_{fb}$  is connected to a positive or a negative reference voltage, depending on the output code. A return-to-zero scheme is applied to reduce inter-symbol interference [7].

2) *Additional Filters:* The added filters barely increase the overall power consumption of the ADC. The noise and distortion of the passive filter is suppressed by the preceding gain of the first integrator. The same is true for the OTA in the feedback path. Hence, this active stage can be biased at only 50  $\mu\text{A}$ .

C. PGA

The filtering STF of this ADC is exploited optimally in combination with programmable gain control of the input signal (Fig. 7). Depending on the amplitude of the input signal, the input resistance is switched between 1, 10, and 100  $\text{k}\Omega$ . As such, the stable input range for the wanted channel is scaled from 5 to 50 to 500 mV. Interferer channels may be applied at a higher level: the characteristic of the allowable input level over frequency (i.e., the inverse of the STF) can be tailored to accommodate optimally the expected worst case combination of a weak wanted channel with strong interferer channels. As mentioned, this is achieved by the choice of  $H_{LPF}(s)$  and, to a lesser extent, by the design of the STF of the conventional ADC.

Together with the input, the bias current of the first stage is adapted in order to scale this dominant noise source. The bias current equals 500  $\mu\text{A}$  for the smallest input range and otherwise 200  $\mu\text{A}$ . The lower limit on the bias current is set by a bandwidth limitation. The dynamic biasing lowers the average power consumption.

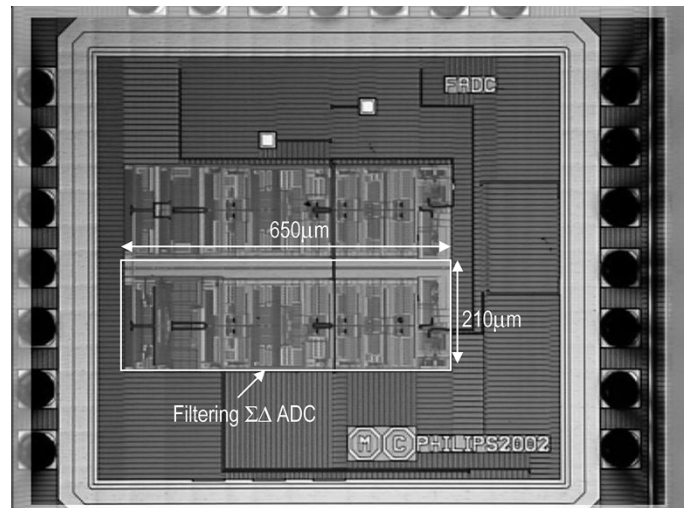


Fig. 9. Chip microphotograph.

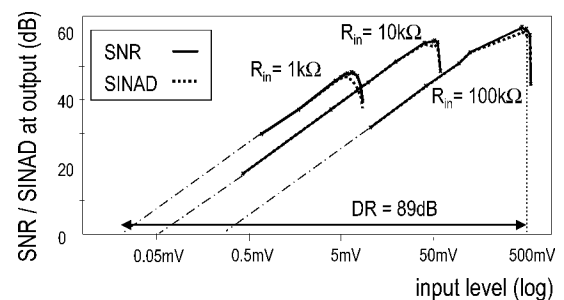


Fig. 10. SNR and SINAD versus input swing for the three gain settings.

V. EXPERIMENTAL RESULTS AND EVALUATION

The design presented has been processed in a digital 0.18- $\mu\text{m}$  CMOS technology (one poly and five aluminum layers). The active area of the ADC is 0.14  $\text{mm}^2$  (see the microphotograph in Fig. 9). The test IC includes a bandgap reference and a crystal oscillator operating at the third overtone frequency of 64 MHz. Differential low-swing output buffers are integrated for measurements.

A. Performance for Wanted Signals

Fig. 10 shows the measured signal-to-noise ratio (SNR) and the signal-to-noise-and-distortion ratio (SINAD) as a function of the input level for the three gain settings. An overall input-referred DR of 89 dB is achieved while the SNR and SINAD at the output remain moderate (resulting in the power and area advantages explained above). Note that the peak SNR and the DR differ per gain setting. This is due to the fact that the relative contribution of thermal noise—compared to quantization noise—differs for the various settings. For  $R_{in} = 100\text{k}\Omega$ , quantization noise is dominant. For  $R_{in} = 1\text{k}\Omega$ , the input signal is 100 times smaller, while the bias current of the first stage is only 2.5 times larger. As a consequence, the thermal noise associated with this stage is significantly larger than the quantization noise. As a second-order effect, the influence of the other stages of the loop filter also becomes more important: as  $R_{in}$  is smaller, their input-referred contribution scales as well. The quantization noise, though, remains the same for all gain settings because the loop parameters (i.e., the time constants) are unaltered.

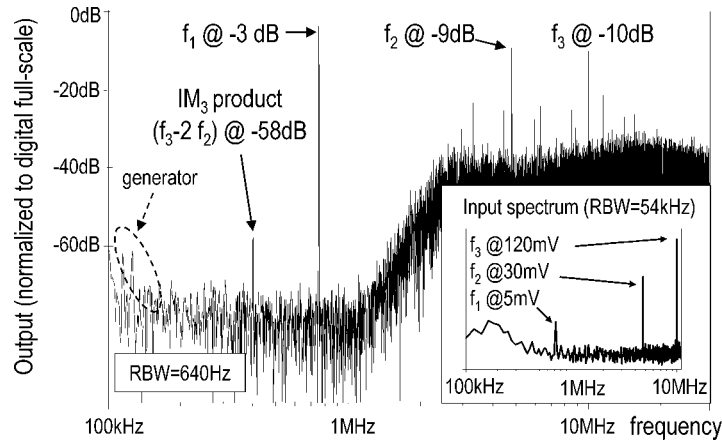


Fig. 11. Three-tone measurement ( $f_1 = 730$  kHz,  $f_2 = 4.8$  MHz,  $f_3 = 10$  MHz) proving filtering transfer and linearity.

### B. Performance for Interferer Signals

These measurements are especially illustrated for the setting where  $R_{in} = 1$  k $\Omega$  and the maximum wanted signal equals 5 mV. In the case of a small wanted level in particular, the interferers are likely to be larger. For the other settings, i.e.,  $R_{in} = 10$  k $\Omega$  and  $R_{in} = 100$  k $\Omega$ , the results for nearby interferers are similar or better. The allowable input level for far-off interferers, though, is limited to the supply voltage because of reliability issues.

The filtering behavior of the ADC is demonstrated in the three-tone test of Fig. 11: a small wanted signal of 5 mV at  $f_1 = 730$  kHz is applied as well as interferers of 30 mV and 120 mV at  $f_2 = 4.8$  MHz and  $f_3 = 10$  MHz, respectively. The input resistance is switched to 1 k $\Omega$  such that the wanted signal appears at  $-3$  dB of the digital full-scale output. The interferers though, are attenuated to  $-9$  dB and  $-10$  dB respectively. Within the conversion bandwidth of the ADC, the noise increases by only 1 dB due to spurious components from the generator. In addition to the filtering, this measurement also demonstrates the linearity with respect to interferers: even while the interferers are significantly larger than the wanted signal, the intermodulation tone at  $f_3 - 2f_2$  is 55 dB lower than the wanted signal.

The remaining aliasing (for a full-scale input near the sample frequency) is listed in Table I. It is larger than expected from (1). This discrepancy is probably due to the fact that the signal is mixed back into the signal band rather than by aliasing. Table I also summarizes the main performance indicators discussed before.

The problem of spurious responses was evaluated by applying various discrete tone inputs. For example, an input tone at 31.25 MHz with a (differential) amplitude of 0.1 V is applied while the maximum wanted signal is only 5 mV ( $R_{in} = 1$  k $\Omega$ ). For this and all other test inputs, the in-band aliases are at least 60 dB lower than the 5-mV wanted signal.

Finally, Fig. 12 plots the measured stable input range over frequency and indicates the improvement compared to a conventional fourth-order  $\Sigma\Delta$  ADC (i.e., without  $H_{LPF}(s)$  and  $H_{HPF}(s)$ ). For the filtering  $\Sigma\Delta$  ADC, nearby interferers can be as large as a full-scale wanted signal, and far-off interferers can be significantly larger while not causing overload.

TABLE I  
OVERVIEW OF MEASURED PERFORMANCE

ADC:	in [0-1MHz], at 64MHz sample rate		
Input amplitude	500mV	50mV	5mV
Dynamic range	65dB	59dB	49dB
SINAD	59dB	57dB	46dB
Suppression of aliases	69dB	67dB	76dB
Bias current (@1.8 V)	0.85mA	0.85mA	1.15mA
<b>Programmable gain:</b>	40dB in 3 settings		
<b>Equivalent filter:</b>	1 <sup>st</sup> order filter, $f_{3dB} = 3$ MHz		
<b>Overall:</b>	DR = 89dB, P < 2mW, area < 0.14 $\mu$ m <sup>2</sup>		

The above results demonstrate the immunity of the filtering  $\Sigma\Delta$  ADC to interferers:  $IM_3$  distortion, aliasing, and spurious components are very low, even when compared to a weak wanted signal, and the stable input range for interferers is significantly extended.

### C. Evaluation

The integration of PGA increases the input-referred DR of this ADC while the SINAD at the output of the ADC remains moderate. As such, the merged PGA-filter-ADC design provides the same functionality as the conventional cascade of filter and PGA stages that precede the ADC in a highly analog receiver [Fig. 1(a)]. In the merged design, though, a better power/performance balance can be achieved: because of the overall feedback, only the input stage of the loop and the overall feedback path are critical. The added filters are inside of the loop and, therefore, not critical in terms of noise or distortion. This is different in the analog receiver where all filters are in the path of the wanted signal.

Furthermore, the merged design performs better than the highly digitized receiver of Fig. 1(b) with the filtering and PGA in the digital domain after the ADC. In addition to the high-accuracy ADC, the references for the ADC need to be extremely clean, i.e., a low-jitter clock and a low-noise voltage reference are required. The decimation filter may also become large and power-hungry because of the required attenuation of quantization noise. In the merged design, only a moderate SINAD is present at the ADC output. As a consequence, less noise shaping is needed (i.e., less oversampling and a lower



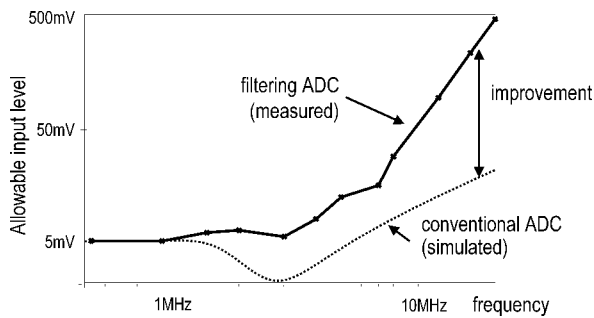


Fig. 12. Stable input range over frequency.

TABLE II  
COMPARISON OF THE QUADRATURE ADC OF [4] WITH TWO  
FILTERING  $\Sigma\Delta$  ADCs

	area	P	DR	SINAD	Allowed jitter
[4]	0.22mm <sup>2</sup>	4.4mW	76dB	75.5dB	<0.02%
this work (2 ADCs!)	0.28mm <sup>2</sup>	<4.1mW	92dB	>49dB	<0.4%

order loop filter can be used). Also, this ADC has a higher tolerance to jitter and noise on its references and, because of the lower quantization noise; the consecutive decimation filter may have less attenuation. The result is an overall power and area saving in the receiver. This is demonstrated in Table II, which compares the performance of the presented ADC to that of [4]. Since [4] presents a quadrature solution, the power, area and performance of two filtering ADCs are used in this comparison. Both designs target the same bandwidth, in the same technology and, to a large extent, use the same circuits. Nevertheless, the filtering ADC clearly outperforms.

## VI. CONCLUSION

A continuous-time fourth-order 1-bit  $\Sigma\Delta$  ADC with explicit filtering has been presented. The filtering signal transfer function provides immunity to interferers above full scale. The combination with passive, programmable gain enables an input-referred DR of 89 dB for a 1-MHz wanted channel while the output SINAD intentionally remains moderate (46–59 dB, depending on the programmed gain). Power consumption is less than 2 mW. The active area is 0.14 mm<sup>2</sup> in 0.18- $\mu$ m digital CMOS. The presented design with merged channel filter, PGA, and ADC functionality consumes less power and area than conventional baseband implementations [1], [2] and state-of-the-art ADC-only designs [4] for Bluetooth.

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integrated receivers

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