A Controller Architecture for High Bandwidth Active Power Filters

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***Abstract*—This paper presents a novel architecture for a unit-delay digital deadbeat current controller for a shunt active power filter (APF). The APF is based on a fixed frequency pulsewidth modulated voltage-sourced converter (VSC). The proposed controller increases the APF current-tracking bandwidth without increasing the VSC switching frequency. Previous APF digital deadbeat controllers have a current-tracking delay of two or more sample-periods. One delay is due to current controller computation, a second sample delay represents VSC actuation time. The paper presents a new controller architecture employing both asynchronous programmable logic and a small microprocessor. Current-tracking feedback control calculations are executed in asynchronous programmable logic to effectively eliminate the controller computation delay. The microprocessor executes fundamental frequency disturbance rejection computations and all other supervisory functions. The proposed architecture retains all high-level functions in the microprocessor to minimize controller development time without compromising APF performance.**

***Index Terms*—Active filter, current control, deadbeat control, digital control, disturbance rejection, programmable logic, unit-delay, VSC.**

I. Introduction

INDUSTRIAL arc welders and arc furnaces draw aperiodic currents, which pollute the distribution system. The rich harmonic content of such currents can create voltage distortion at their point of common coupling (PCC) to the distribution system. Voltage distortion may threaten the sound operation of power quality sensitive loads electrically near the PCC. Common problems caused by the harmonic polluting loads include incandescent lamp flicker [1], [2] and capacitor bank overheating [1].

Passive shunt filters installed at the polluted PCC are tuned to eliminate specific unwanted current harmonics. The most significant shortcomings of such filters are their poor dynamic performance, their susceptibility to resonance, and the large physical size of their capacitive and inductive elements.

Active power filters (APF) perform the same basic function as passive filters, but are based on power electronic devices. The shunt APF is a voltage-sourced converter (VSC), coupled to the PCC through inductive impedance. Fig. 1 shows a single-line diagram of a shunt APF with a load and an equivalent distribution system network.

Manuscript received January 25, 2002; revised October 3, 2002. Recommended by Associate Editor S. B. Leeb.

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Digital Object Identifier 10.1109/TPEL.2002.807101

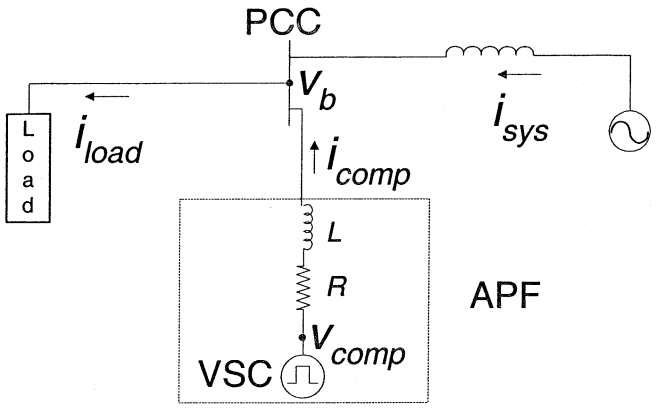

Fig. 1. Shunt APF with polluting load and a distribution system equivalent network.

The APF current feedback controller measures the polluting load current (i_{load}) and the APF output current (i_{comp}). A linear feedback controller [3] commands the VSC output voltage (v_{comp}) that drives the APF current to equal the polluting components of the load current. APF's with current feedback control can avoid resonance, and the sizes of their passive components can be greatly reduced compared to passive filters. The APF is also better suited to the compensation of time varying loads since it can eliminate a broad range of low frequency harmonics.

The reference-to-output transfer function characterizes one aspect of APF current controller performance. Since an inductor couples the VSC to the PCC, the voltage across the inductor is the difference between the VSC output voltage and the distribution system voltage. Thus, the distribution system voltage interferes with the VSC's lone influence over the APF current. This is why the distribution system bus voltage, v_b, is treated as an additive disturbance signal, $w = -v_b$, whose effect on the output current should be eliminated. Another measure of APF current controller performance is its disturbance-to-output transfer function. A block diagram of a discrete-time APF system, with a single controller $D(z)$, is given in Fig. 2.

A discrete-time system is described as deadbeat if its reference-to-output transfer function is a polynomial of finite order in z^{-1}. This amounts to a finite duration impulse response in the discrete-time domain. Practical deadbeat APF current control is characterized in the time-domain by a finite number of reference-to-output sample-period tracking delays. Established deadbeat APF current controller performance in the literature shows a two-delay reference-to-output tracking delay [4]. One delay is used for computing the necessary VSC voltage to drive the APF current to the reference value. Another delay is for applying that VSC voltage across the coupling inductor.

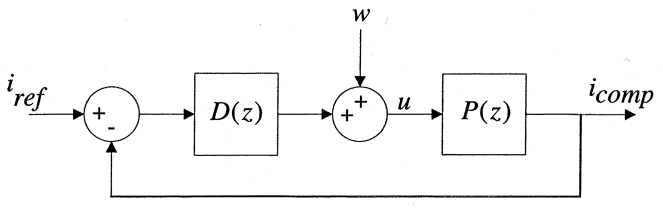

Fig. 2. Block diagram with a single controller for reference tracking and disturbance rejection.

High order controller computations, implemented in software, elapse over many digital clock cycles in microprocessors or DSPs. The appreciable computation time entails delaying the actuation of the control signal until the subsequent sample instant. This paper proposes a novel controller architecture that eliminates the reference-to-output controller computational delay for a single phase APF. This is achieved by implementing a low order current controller in programmable asynchronous digital logic. The advantage of asynchronous digital logic is that it allows the control signal computation to propagate without holding intermediate arithmetic results in clock-dependent memory elements. The elimination of the computation delay reduces the reference-to-output tracking delay from two sample periods to just one.

The consequences of the current-tracking delay of digital APF controllers is more clearly appreciated in terms of steady state phasor representation of the signals involved. Fig. 3 shows a comparison of the current error phasors for unit delay [Fig. 3(a)] and for two-delay [Fig. 3(b)] current-tracking controllers, assuming unity gain reference-to-output current magnitude tracking for both. The magnitude of the current error $|I_{\text{error}}|$ is related to the nth harmonic reference current of frequency f_n and magnitude $|I_{\text{reference}}|$, and the controller time delay T_d as

$$|I_{\text{error}}| = 2|I_{\text{reference}}|\sin(\pi f_n T_d). \tag{1}$$

The phasor diagrams of Fig. 3 distil the advantage of eliminating the current-tracking computational delay. For a given VSC switching frequency, the range of harmonic currents that can be compensated, within a given error tolerance, is significantly greater. In other words, elimination of one delay more than doubles the bandwidth of the APF without increasing the VSC switching frequency.

The desired unit-delay reference tracking is expressed by (2). Disturbance rejection is expressed by (3), where Ω_0 is the ac distribution system fundamental frequency

Reference-to-output:

$$\left.\frac{I_{comp}(z)}{I_{ref}(z)}\right|_{W(z)=0} = z^{-1}. \tag{2}$$

Disturbance-to-output:

$$\left.\frac{I_{comp}(z)}{W(z)}\right|_{I_{ref}(z)=0} = 0, \quad \forall\, w_k = W_0 \sin(\Omega_0 T k + \phi). \tag{3}$$

Equation (2) describes a very simple deadbeat impulse response, a unit-delayed impulse of unit amplitude.

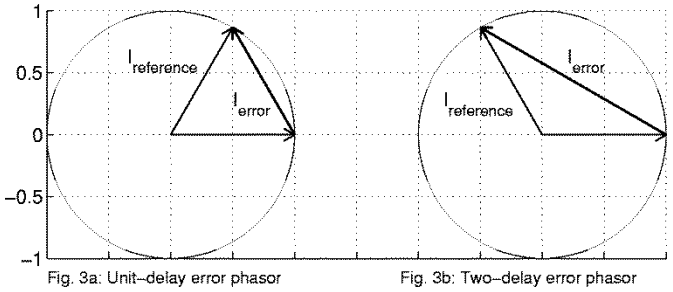

Fig. 3. Phasor diagram for unit-delay and two-delay reference tracking.

II. Digital Models

In order to design a discrete-time current controller, the APF is best described in terms of a z-domain model. The coupling inductor is modeled as a linear time-invariant inductive (L) admittance having effective series parasitic resistance (R). The continuous-time integral equation relating its terminal voltage (v) to its current (i) is used as the starting point for plant model discretization

$$i(t_2) = i(t_1)e^{-T/\tau} + \frac{1}{L}\int_{x=t_1}^{x=t_2} v(x)e^{-(1/\tau)(t_2-x)}\,dx \tag{4}$$

where $t_1 < t_2$, $\tau = L/R$, and T is the controller sample period. $u(kT)$ is defined as the average voltage across the coupling impedance, over each controller sample period (T)

$$u((k-1)T) \doteq \frac{1}{T}\int_{x=(k-1)T}^{x=kT} v(x)\,dx. \tag{5}$$

The currents and voltages are sampled synchronous to the controller sample period, T, to give a discrete-time difference equation

$$i_k = e^{-T/\tau} i_{k-1} + \frac{(1-e^{-T/\tau})}{R}\,u_{k-1} \tag{6}$$

where subscript k implies the sampled signal's value is taken at time $t = kT$. Equation (6) may be described by the equivalent discrete-time transfer function

$$P(z) = \frac{I(z)}{U(z)} = \frac{K_p}{z - e^{-T/\tau}} \tag{7}$$

where $K_p = (1 - e^{-T/\tau})/R$.

It is implicit in the plant model derivation that the VSC output voltage is taken to be its average over each sample period. Given the switched nature of the VSC output voltage, this does not account for the ripple of the VSC output voltage. The VSC in the experimental prototype is designed to use three-level voltage switching to reduce its output voltage ripple.

III. Partitioned APF Controller

In the course of choosing the final APF current controller, designing a single controller $D(z)$ in the form of Fig. 2, which simultaneously satisfies (2) and (3), is not practical for two reasons. First, it offered no means of directly limiting the maximum VSC current. Secondly, the complexity of $D(z)$is too high for efficient implementation in low cost programmable digital logic.

Thus the proposed configuration partitions the controller block into two distinct discrete-time control computers, as is illustrated in Fig. 4.

A. Fast Control Layer

The proportional controller, labeled $C(z)$, achieves the desired unit-delay reference-to-output tracking. Proportional control has minimal arithmetic complexity. Thus, it is well disposed to asynchronous programmable logic implementation. This feedback loop is termed to be the "fast control layer" because of its nearly instantaneous execution of control computations. The reference-to-output and disturbance-to-output z-domain transfer functions of the fast control layer (without the slow control layer signals) are given by

$$\frac{I_{comp}(z)}{I_x(z)} = z^{-1} \tag{8a}$$

$$\frac{I_{comp}(z)}{W(z)} = K_p z^{-1}. \tag{8b}$$

Equation (8a) matches the desired reference-to-output transfer function in (2). Equation (8b) shows that the natural disturbance rejection of the "fast" proportional controller is a scaled unit delay of significant amplitude. The value of K_p, associated with the system parameters of Table I, is 0.305 p.u. Hence, 1 per unit system voltage in Fig. 1 would result in 0.305 p.u. APF current. The desired current tracking is achieved but disturbance rejection is not satisfactory.

The second control computer is dedicated to supplementing the fast layer's disturbance rejection at frequency Ω_0. This disturbance rejection computer is named part of the "slow control layer" because its implementation uses a sample period to complete its computations. The slow control computer also performs other supervisory control functions, including DC voltage regulation for the VSC; and user interface.

High engineering design costs are associated with complex programmable logic device (CPLD) programming. These are minimized by designing only the fast control layer in custom logic, as this is the minimum logic necessary to achieve the increased APF bandwidth. Disturbance rejection, dc voltage regulation, user interface and other supervisory functions are programmed in a simple microprocessor using a high-level programming language. This avoids the exorbitant engineering and hardware cost of realizing complex supervisory features in low-level programmable logic. The computational delay associated with the microprocessor implementation affects only slowly changing signals and may therefore be compensated in software, without diminishing APF performance.

B. Slow Control Layer

A distribution system voltage can be nominally modeled as a 60 Hz oscillator and a linear observer is effectively used to estimate it [5], [6]. The observer uses the sampled APF reference and output currents, already required by the fast layer, to estimate the disturbance signal. Fig. 1 shows that the voltage across the APF coupling-reactor is the difference between the VSC output voltage and the distribution system voltage. Equation (9) expresses this as the sum of the time average VSC output voltage and the disturbance signal

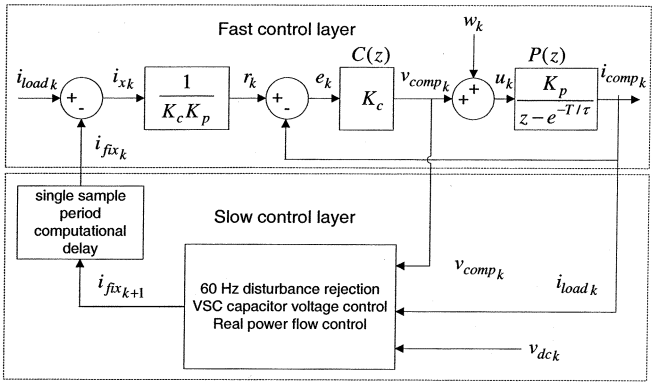

Fig. 4. Partitioned control block diagram. Fast control layer provides reference tracking. Slow control layer is responsible for disturbance rejection.

TABLE I
PLANT MODEL PARAMETERS AND BASE VALUES FOR SIMULATION

Shunt coupling resistance *(R)*	0.2 Ω
Shunt coupling inductance *(L)*	2.46 mH
Controller Sample Period *(T)*	100 μs
V_{base}	115 V_{rms}
I_{base}	15 A_{rms}
Z_{base}	7.67 Ω

$$u_k = \overline{v}_{comp_k} + w_k. \tag{9}$$

Recognizing that the current (i) through the coupling-reactor in (6) is the APF output current (i_{comp}), gives

$$i_{comp_{k+1}} = \Phi_{comp} i_{comp_k} + \Gamma_{comp} \overline{v}_{comp_k} + \Gamma_{comp} w_k \tag{10}$$

where $\Phi_{comp} = e^{-T/\tau}$ and $\Gamma_{comp} = (1 - e^{-T/\tau})/R$. A model for the disturbance is a pure oscillator, with discrete-time state equations

$$\begin{bmatrix} x_{osc1} \\ x_{osc2} \end{bmatrix}_{k+1} = \begin{bmatrix} 0 & 1 \\ -1 & 2\cos\omega_0 \end{bmatrix} \begin{bmatrix} x_{osc1} \\ x_{osc2} \end{bmatrix}_k \tag{11a}$$

$$w = x_{osc1} \tag{11b}$$

where $\omega_0 = \Omega_0 T$, $\Omega_0 = 2\pi \cdot 60$ rad/s, the frequency of the disturbance oscillator model. Expressing (10) and (11) together gives the state space form in

$$\begin{aligned} x_{k+1} &= A_1 x_k + B_1 \overline{v}_{comp_k} \\ i_{comp_k} &= C_1 x_k \\ w_{k+1} &= C_w x_{k+1} \end{aligned} \tag{12}$$

where

$$x_k = \begin{bmatrix} i_{comp} \\ x_{osc1} \\ x_{osc2} \end{bmatrix}_k, \quad A_1 = \begin{bmatrix} \Phi_{comp} & \Gamma_{comp} & 0 \\ 0 & 0 & 1 \\ 0 & -1 & 2\cos\omega_0 \end{bmatrix},$$

$$B_1 = \begin{bmatrix} \Gamma_{comp} \\ 0 \\ 0 \end{bmatrix}, \quad C_1 = [1 \quad 0 \quad 0], \quad \text{and} \quad C_w = [0 \quad 1 \quad 0].$$

Let $\hat{x}_k$ denote the estimate of the true state vector x_k, and similarly for other signals. A linear observer is used to compute $\hat{x}_k$, which asymptotically tracks x_k, by feeding back the APF current estimate error

$$\hat{x}_{k+1} = A_1\hat{x}_k + B_1\overline{v}_{comp_k} + F(\hat{i}_{comp_k} - i_{comp_k}) \quad (13)$$

where the observer gain matrix is $F \in \Re^{3\times 1}$. Substituting $\hat{i}_{comp_k} = C_1\hat{x}_k$ into (13) gives the final form of the observer

$$\begin{aligned}\hat{x}_{k+1} &= (A_1 + FC_1)\hat{x}_k + [\,B_1 \quad -F\,]\begin{bmatrix}\overline{v}_{comp_k}\\ i_{comp_k}\end{bmatrix}\\ \hat{w}_{k+1} &= C_w\hat{x}_{k+1}.\end{aligned} \quad (14)$$

The observer error is defined by $e_k = \hat{x}_k - x_k$. Subtracting (12) from (13) gives

$$e_{k+1} = (A_1 + FC_1)e_k. \quad (15)$$

Thus F is chosen to stabilize the eigenvalues of the observer error [7], to guarantee that e_k asymptotically decays to zero. The stable placement of the observer error poles is done such that the disturbance estimate error decays to 5% of its initial value within a 60 Hz cycle. The use of linear simulation tools can be used off-line to numerically refine the observer performance.

The disturbance rejection algorithm block diagram is included in Fig. 5, which shows details of the slow control layer. The term i_{wk} in Fig. 5 adjusts the fast-layer reference signal to reject the disturbance. The observer has a relatively extensive arithmetic requirement, but its response time is slow relative to the sampling period. It may therefore be included in the slow layer controller and implemented using C-code programming of the microprocessor. The predictive nature of the observer has the necessary phase advance of the estimated disturbance. This compensates the computational delay caused by using the low-cost microprocessor. The slow control layer has other functions that complement the unit-delay reference tracking of the fast layer: regulating the voltage of the VSC capacitor; limiting power flow to and from the APF.

A simple PI-controller is used to maintain the VSC capacitor voltage (V_{dc}) [8]. Fig. 5 indicates how the capacitor voltage regulator controls the real average APF power that is exchanged with the distribution system. A contribution, i_{dc}, to the APF reference current is introduced that is in-phase with the distribution system voltage. This gives VSC capacitor voltage regulation at unity power factor.

The slow control layer also regulates the steady-state power exchange between the VSC and the distribution system. The slow layer's power control contribution to the reference current is i_{60} (Fig. 5). The mechanism selectively eliminates the 60 Hz fundamental frequency component of the load current to ensure the APF supplies only the non-60 Hz components of the load current. This allows the APF to limit its real average power exchange with the load. Modification of this loop can permit 60 Hz reactive power compensation of the load, if required. The loop relies on a moving window discrete Fourier transform (DFT) to measure the fundamental frequency component of the load current. The moving window DFT synthesis block reconstructs the 60 Hz fundamental frequency discrete-time signal with a sample-period phase advance. This compensates the single sample-period computational delay incurred by the microprocessor.

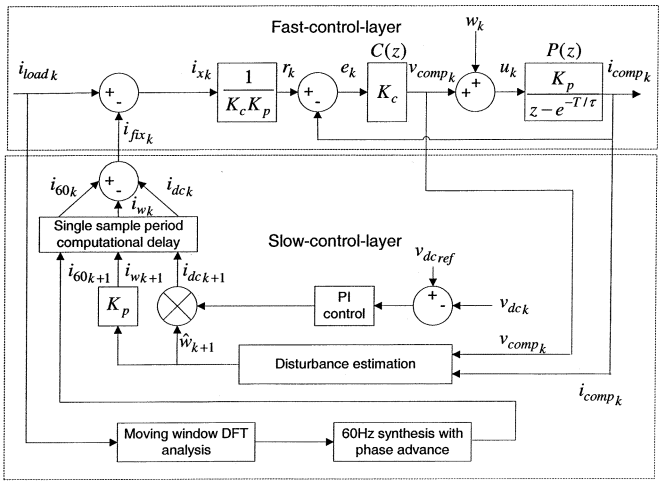

Fig. 5. Detailed block diagram of partitioned APF controller.

IV. Robustness Analysis and Simulation

Robustness analysis of the current control system is relevant to choosing the final APF design. The plant parameters, R and L, are expected to vary with frequency and magnitude of the APF current. Magnetic core effects and switch losses are causes of such plant model nonlinearity. With this parameter uncertainty, the closed-loop pole of the reference-to-output transfer function moves along the real axis of the z-plane, away from the origin. The robustness of the system to variations in the true plant parameters R and L is therefore evaluated.

Let L_0 and R_0 represent the model parameters used for controller synthesis. Equation (17) shows how mismatch between controller and true plant parameters influence the reference-to-output current transfer function

$$\frac{I(z)}{I_{ref}(z)} = \frac{\frac{1-e^{-T/\tau}}{1-e^{-T/\tau_0}}\frac{R_0}{R}}{z - e^{-T/\tau} + e^{-T/\tau_0}\left(\frac{1-e^{-T/\tau}}{1-e^{-T/\tau_0}}\frac{R_0}{R}\right)} \quad (16)$$

$$\text{where } \tau = L/R, \quad \text{and} \quad \tau_0 = L_0/R_0. \quad (17)$$

Fig. 6 presents a sensitivity analysis that examines the location of the closed-loop fast-layer pole (along the real axis of the z-domain) with changes in the error of plant model parameters R and L. Mismatch between L_0 and L dominates the error of the closed-loop pole location.

The impulse response ceases to be deadbeat with plant model parametric error. The impulse response decays with an exponential envelope, which is an infinite duration impulse response. Time-domain step response simulations for the extremes of the sensitivity analysis are shown in Fig. 7. A +5% model error in L translates into about 5% undershoot in the time-domain step response. The sensitivity to model error in R is secondary. These demonstrate tolerable theoretical robustness of the reference-to-output performance of the controller.

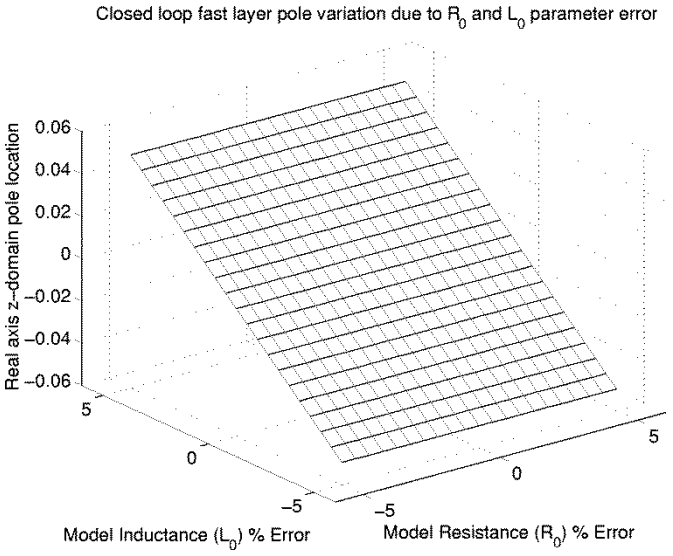

Fig. 6. Fast-layer pole sensitivity analysis for variation in plant parameters R and L.

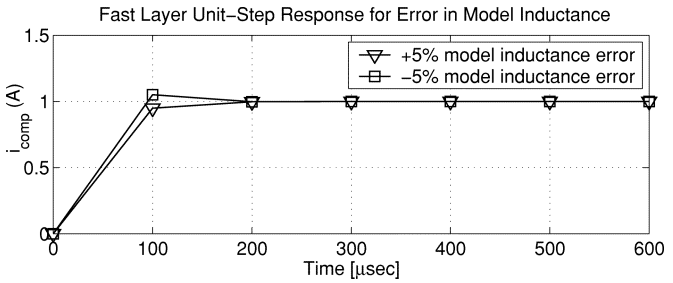

Fig. 7. Fast control layer step responses for error in model parameter L.

V. Experimental Prototype

The subsystems of the APF digital control system are realized in three separate printed circuit boards, as per Fig. 8. These boards hold the CPLD, where the control computations are executed; the data-acquisition circuits; and the level-shifting circuits for driving the VSC switches.

The most complex board holds the CPLD. This commercial board is part of the ALTERA *Excalibur Development Kit*. A single CPLD is used to implement the slow-layer and fast-layer digital controllers, the analog to digital converter (ADC) interface, and the digital pulsewidth modulator (PWM). The data-acquisition circuits sense and digitize relevant signals for the current control computers.

The fast-layer controller is implemented using VHDL-1993, a digital hardware description language [9]. The basic block diagram of the fast control computer implementation in digital hardware of Fig. 9 follows Fig. 4. Input signals are the measured load current, i_{load}, the measured APF output current, i_{comp}, and the current adjustment from the slow control layer, i_{fix}. The desired VSC output voltage ("DV") computed by the fast control layer is passed to the PWM stage.

A cascade of fixed-point arithmetic blocks has 12-b APF current and reference current samples as registered inputs, shown in Fig. 9. The arithmetic circuits execute two multiplications and one subtraction, only registering the final 16-b result for use by the PWM stage. The timing signal, "loadixicomp," loads the

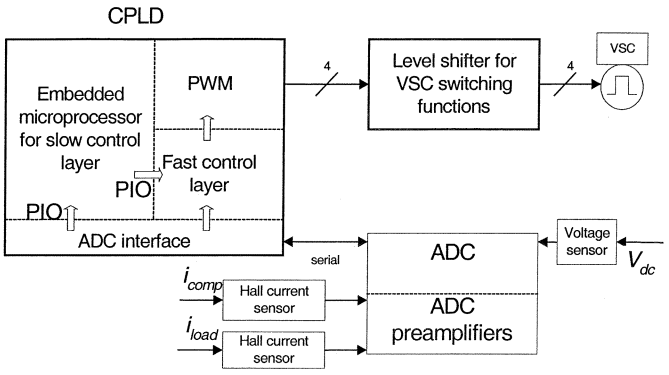

Fig. 8. Control hardware circuit board interconnections. Parallel input–output (PIO) channels transfer data between the embedded microprocessor and other internal logic circuits.

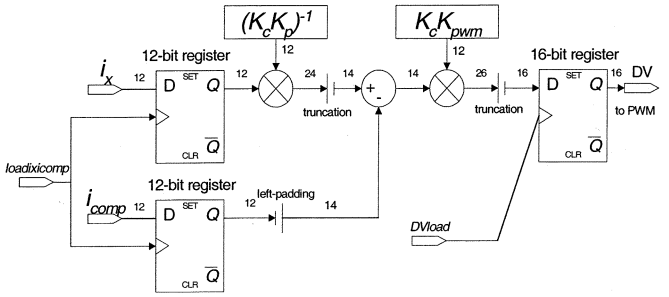

Fig. 9. Schematic of fast control layer digital hardware architecture.

ADC conversion results, i_x and i_{comp}, to the arithmetic circuit of the fast-layer proportional controller. "DVload" stores the fast-layer result into input registers used by the PWM stage. The fast-layer computation time measures 100 ns, from the rising edge of "loadixicomp" to the rising edge of "DVload."

Controllers implemented in microprocessors and DSP's exhibit a calculation delay that represents an appreciable fraction of the sample period. This requires the control signal to be held over and only implemented in the next sampling period. In contrast, the asynchronous architecture in Fig. 9 achieves an input to output delay of only 2 CPLD clock cycles, where the clock frequency is 20 MHz. This avoids the lapse of a full 100 μs controller sample period before the control signal is actuated. This represents the effectively negligible delay from the moment of sample data availability to the computation of the fast-layer control signal. Herein is the primary advantage of this novel controller configuration over conventional microprocessor or DSP implementations.

The slow control layer computer is responsible for computing several sequences of fixed-point arithmetic as discussed below. The implementation of these mathematical operations is performed in an ALTERA NIOS soft-core 33-MHz 32-b microprocessor. This processor is loaded into the same CPLD as the fast control layer computer. The processor may be repeatedly modified and reloaded into the CPLD using ALTERA *Quartus* software tools. This configuration tremendously simplifies the interfacing demands between the microprocessor and the digital hardware of the fast control layer. The particular feature of the NIOS microprocessor that provides this flexibility is the parallel input–output (PIO) block. Numerous PIOs are used to quickly

TABLE II
SUMMARY OF EXPERIMENTAL PARAMETERS

Parasitic coupling resistance *(R)*	0.2 Ω
Shunt coupling inductance *(L)*	2.46 mH
Controller sample period *(T)*	100 μs
PWM switching frequency (f_{sw})	5 kHz
Choke inductance (L_{choke})	0.5 mH
Rectifier load inductance (L_{rect})	15 mH
Rectifier load resistance(R_{rect})	4.42 Ω
VSC DC-side capacitor (C_{dc})	4800 μF
VSC DC-side voltage (V_{dc})	220 V
Distribution system equivalent Inductance (L_{sys})	0.66 mH
Distribution system voltage (V_{sys})	100 V_{rms}

exchange multi-bit data between the NIOS processor and other logic circuits within the CPLD (Fig. 8).

The NIOS processor executes a C-program to compute the slow control layer signals. It requires 55 μs to complete the slow-layer computations, which is over half of each 100 μs controller sample period. The output from the slow layer is used in the subsequent sample period by the fast layer.

VI. EXPERIMENTAL RESULTS

This section describes experimental results from tests performed on individual APF subsystems, as well as on the fully integrated APF system. Table II specifies all experimental parameter values, which are used in the ensuing test circuits.

A. Fast Layer Testing

The experimental testing of the fast-layer reference-to-output transfer function is presented here. The fast-layer proportional controller is tested in the absence of the distribution system voltage ($w = 0$), as shown in Fig. 10, with relevant circuit parameters from Table II. This configuration uses a function generator to provide reference signals to the current controller. In all of the isolated fast-layer experimental tests, a dc generator regulates the VSC capacitor voltage (V_{dc}).

Testing the fast control layer with pure tone sinusoidal signals for a variety of frequencies is summarized in the reference-to-output bode plot of Fig. 11. These confirm unit-delay current tracking of the fast control layer as designed in (2). Theoretical results are derived from the relation

$$\left.\frac{I_{comp}(e^{j2\pi Tf})}{I_{ref}(e^{j2\pi Tf})}\right|_{W(e^{j2\pi Tf})=0} = e^{-j2\pi Tf} \qquad (18)$$

where f is the frequency of interest in *Hz*.

The experimental and theoretical bode plots in Fig. 11 are in close agreement, from fundamental frequency to 1.6 kHz. This is near the practical bandwidth of the APF, which is limited by the phase lag characteristic. Deviations from the theoretical results are caused by high frequency effects in the iron core 60 Hz coupling inductor.

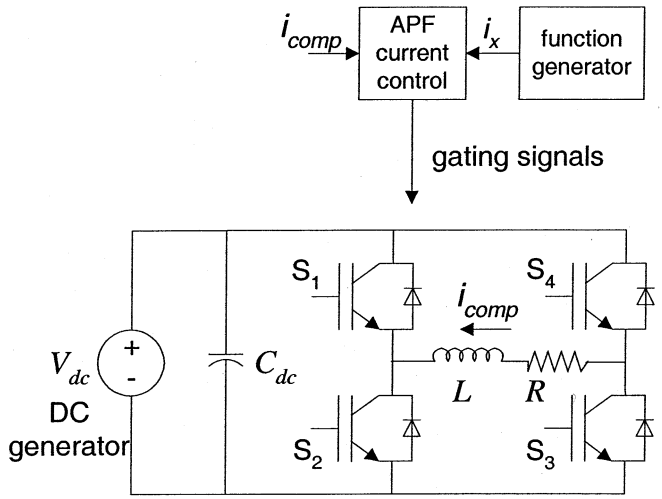

Fig. 10. Circuit for testing APF fast control layer, without disturbance signal.

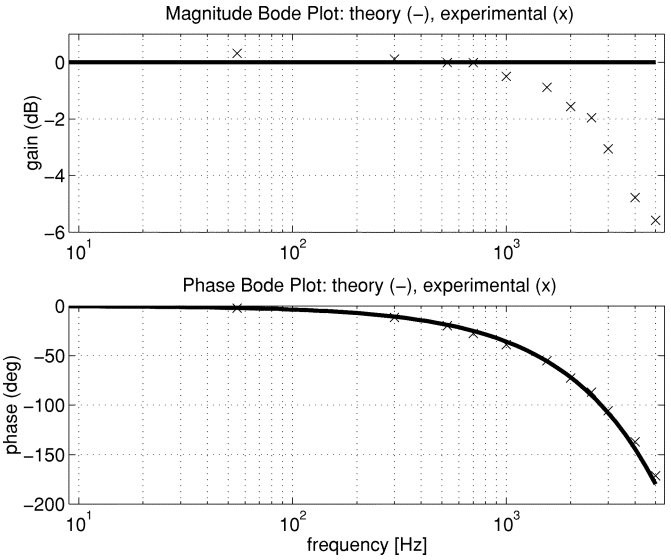

Fig. 11. Bode plot of fast control layer reference-to-output current gain. Theoretical (solid) and experimental (x) magnitude and phase bode plots are shown.

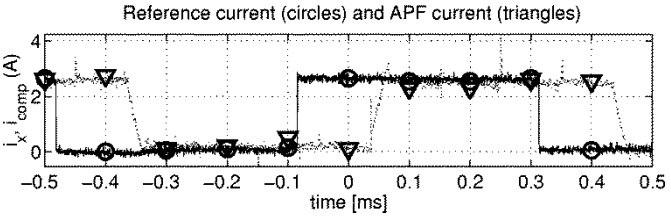

Fig. 12. Experimental step reference current (1.8 A) and APF output current. Controller sampling instants occur at times 0 ms, ± 0.1 ms, ± 0.2 ms · · · ± 0.5 ms.

Dynamic testing of the fast layer is done using step reference signals. Fig. 12 presents a 2.5 A step reference with the corresponding experimental APF output current. The rising edge of the step reference input occurs between the sampling instants at −0.1 ms and 0 ms. The discrete-time fast-layer controller only detects the change in reference at the 0 ms sampling instant. As

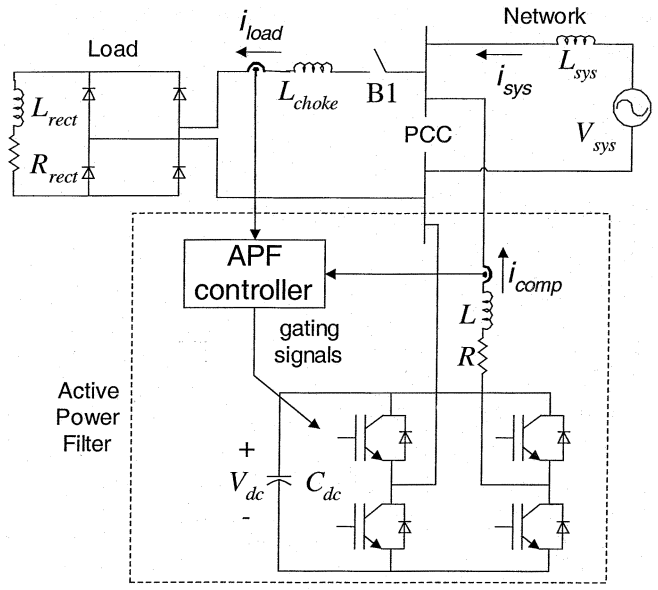

Fig. 13. APF test circuit without load (B1 open) and with load (B1 closed). Parameter values as specified in Table II.

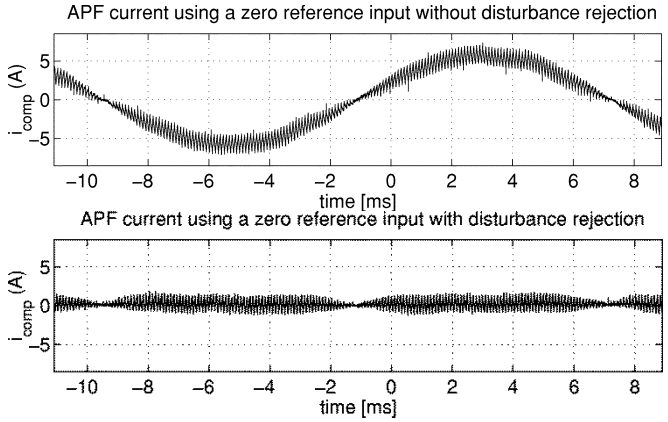

Fig. 14. APF current injected into the PCC: (upper trace) without disturbance rejection; (lower trace) with disturbance rejection.

anticipated, the APF current tracks the reference in a single time step.

B. Steady State Disturbance Rejection Test

The circuit of Fig. 13 is used in the no load configuration to test the disturbance rejection subsystem. Switch B1 is kept open and the parameter values of Table II apply. A reference current of zero is requested from the APF. Fig. 14 shows the resulting APF current without and with disturbance rejection enabled. When disturbance rejection is included, the APF system successfully tracks the zero reference current. This demonstrates the desired experimental behavior of the disturbance rejection system.

C. Steady State APF Testing

All the coordinated subsystems of the fast layer and slow layer of the APF current controller are tested using a full bridge rectifier load, with switch B1 closed in Fig. 13 and with parameter values from Table II. The rectifier has an RL-load connected to its output terminals, in order to create a load current with high

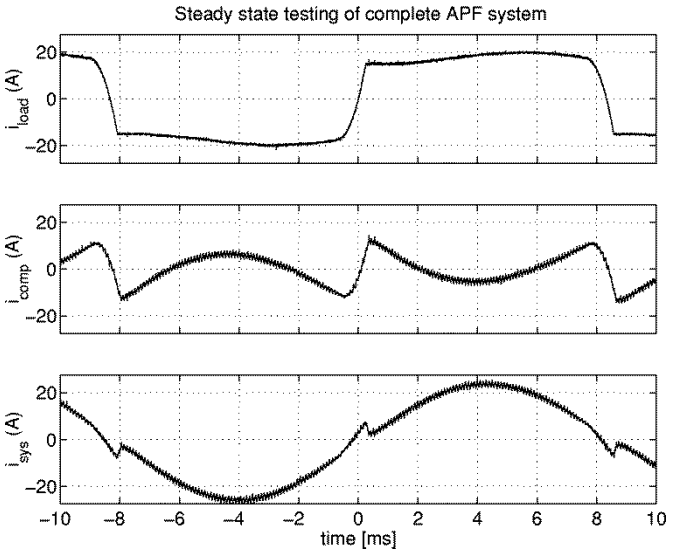

Fig. 15. Steady state current waveforms: (upper) load current; (center) APF current; (bottom) distribution system current.

harmonic content. Fig. 15 shows the experimentally measured steady state load current, APF current and distribution system current. The 60 Hz component of the distribution system current exceeds that of the load current. This reflects the real power supplied to the APF for capacitor voltage regulation.

Table III gives the magnitudes of the current harmonics in the load and distribution system. The harmonics in the distribution system current represent the APF tracking error. Also shown is the expected unit-delay current-tracking error calculated as in (1)

$$|I_{\mathrm{error}_n}| = 2|I_{\mathrm{load}_n}|\sin(\pi f_n T_d) \tag{19}$$

for positive integers n, where $f_n = 60n$ Hz, and $T_d = 100$ μs. The measured distribution current harmonics can be directly compared to the theoretical unit-delay APF current tracking error.

The fundamental frequency component of the expected unit-delay current tracking error is not included in Table III because it is a function of the APF power losses. The fundamental frequency data reveals that the distribution current magnitude exceeds the load current magnitude in order to supply the VSC with enough real power to support its capacitor voltage. The real power delivered to the VSC capacitor primarily compensates for VSC IGBT conduction and switching losses.

D. Dynamic APF Testing

Testing the dynamic response of the APF current controller is done using Fig. 13. A rectifier load is kept online for the duration of the test with switch B1 closed (Fig. 13). The relevant circuit parameters are found in Table II, except that a step reduction in the rectifier load (R_{rect}) resistance is made from 115 Ω to 4.42 Ω. The load current, APF current and distribution system currents are given in Fig. 16.

The step reduction in rectifier load resistance at $t = -10$ ms causes an increase in load current. The APF supplies nearly the entire load current until time, $t = 0$ ms. The 60 Hz component of the load current is measured using a moving window DFT

TABLE III
SUMMARY OF ANTICIPATED AND EXPERIMENTALLY MEASURED TRACKING ERRORS

Frequency	Load Current	Distribution System Current	Theoretical Unit-delay Tracking Error
[Hz]	[A rms]	[A rms]	[A rms]
60	16.26	17.36	-
180	4.48	0.60	0.51
300	2.59	0.54	0.49
420	1.69	0.48	0.45
540	1.18	0.42	0.40
660	0.83	0.35	0.34
780	0.60	0.28	0.29
900	0.42	0.23	0.23
1020	0.31	0.18	0.19
1140	0.22	0.15	0.16

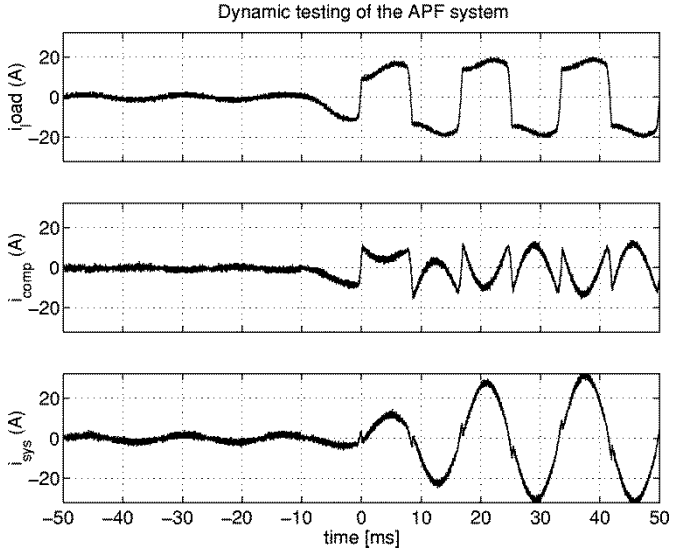

Fig. 16. APF dynamic testing current waveforms: (upper) load current; (center) APF current; (bottom) distribution system current.

over 16.6 ms, by the slow control layer. As the moving window captures the rising load current, the APF supplies less of the fundamental frequency component of the load current. This corresponds to the increasing envelope of the distribution system current. The APF continues to supply the load current harmonics while allowing the distribution system to increasingly provide the 60 Hz component of the load current.

The load current transient occurs between $t = -10$ ms and $t = +10$ ms. The APF effectively helps the distribution system current remain sinusoidal. Equipping the VSC with greater capacitive energy storage and increasing the duration of the moving window DFT would allow the APF to change the amplitude of the distribution system current more gradually.

E. Distribution System Voltage

The analysis of the complete APF experimental performance is concluded by investigating its ability to compensate a rectifier with *RL* load as shown in Fig. 13. Switch B1 is closed

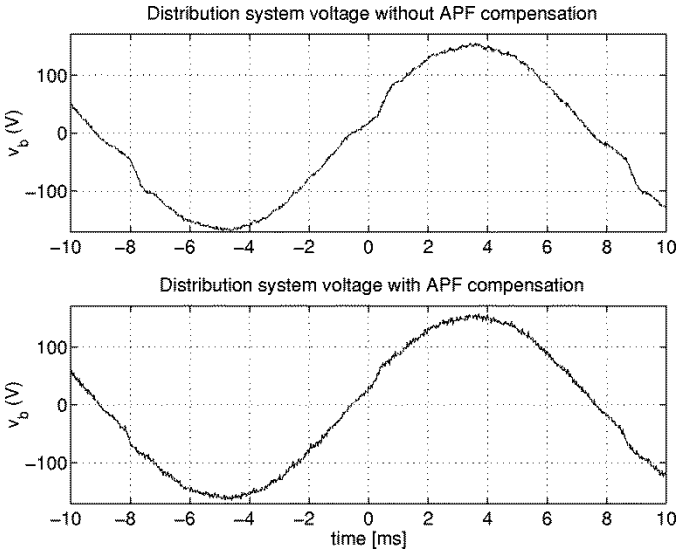

Fig. 17. Distribution bus voltage at the PCC: without and with APF compensating the rectifier load.

TABLE IV
HARMONIC VOLTAGE DISTORTION AT THE POINT OF COMMON COUPLING

Frequency	Distribution System Voltage Harmonics	
[Hz]	With APF	Without APF
	[V rms]	[V rms]
60	96.18	96.61
180	0.43	1.89
300	0.99	2.34
420	0.55	1.56
540	0.52	1.37
660	1.06	1.67
780	0.68	1.19
900	0.61	0.60
1020	0.54	0.54
1140	0.43	0.39
% THD	*2.04%*	*4.28%*

and the parameters are given in Table II. The *RL* loaded rectifier draws a heavily distorted current from the system. The harmonic spectrum of the system current and the PCC voltage is measured in the presence and absence of the APF. The steady state PCC voltage with and without the APF in operation is shown in Fig. 17. Although the waveforms of Fig. 17 look similar due to the large fundamental frequency component of the bus voltage, harmonic analysis of the voltage highlights some significant differences. Harmonic voltage analysis results are presented in Table IV. These show an improvement of total harmonic distortion (THD) from 4.28%, without APF compensation, to 2.04%. Given a typical voltage THD limit of 5%, the APF clearly increases the operating margin significantly. It should be noted that even in the absence of any distorted load the voltage THD on the bus is over 1%. The APF is incapable of reducing the components of the THD that are not attributed to the load current harmonics.

VII. Conclusion

A new digital controller architecture is proposed for an APF operating with fixed frequency PWM. The novel architecture exploits the strengths of both digital hardware and microprocessor computational resources to achieve unit-delay current tracking. The main advantage derived from this architecture is improved current-tracking bandwidth over the two-delay deadbeat current controllers implemented with conventional DSP or microprocessor hardware. This gain comes without increasing the VSC switching frequency or ratings.

Steady state and dynamic performance is experimentally established, with less than 10% magnitude error tracking, within the 1.6 kHz bandwidth of the APF, and phase-lag consistent with a single sample-period tracking delay. A test case, where the APF compensates a highly distorted rectifier load verifies complete APF operation. Third harmonic distortion in the distribution system current is reduced by 87%. Analysis of the distribution voltage total harmonic distortion shows a reduction from 4.28% to 2.04% with the APF current compensation.

The experimental controller implementation uses a hybrid of application specific digital hardware and a microprocessor within a single commercial CPLD. This provides a new template for increased power electronic control system integration. As with DSP-based solutions, the proposed hybrid architecture maintains a user-friendly programming environment, with high-level C-programming used to implement all complex control functions. By excluding the processor from the current control loop, the need for a high cost, high performance DSP is avoided. Modification or upgrading of the current controller is also possible and may be accomplished through reprogramming of the CPLD.

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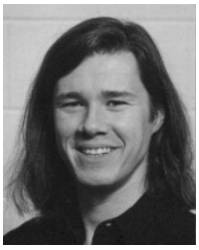

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