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A Converter-level On-state Voltage Measurement Method for Power Semiconductor Devices

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***Abstract*—This letter proposes a converter-level method for measuring the on-state voltages of all power semiconductors in a single-phase inverter by using a single circuit only. The proposed circuit distinguishes itself by connecting to the middle-point of each phase-leg, instead of the two power-terminals of individual devices as conventional methods do. It has the advantages of reduced circuit complexity, size, cost, and ease of connection. The principle and theoretical analysis of the proposed converter-level method are discussed. A case study on a single-phase full-bridge inverter is demonstrated to prove the concept.**

***Index terms*—** Power semiconductor, power converter, converter-level, on-state voltage.

I. Introduction

The on-state voltages of power semiconductor devices are the most widely reported temperature sensitive electrical parameters [1] or health indicator [2], including the $V_{\mathrm{CE,sat}}$ of IGBT, V_{DSon} of MOSFET, and V_{F} of diode. Many efforts have been made to measuring this low-voltage (i.e., in the range from sub-volt to few volts) at mV resolution from the off-state voltage up to few kV.

A review of the hardware-based on-state voltage measurement methods has been included in [3], which summarizes the low-frequency measurement through relay-switch/zener-diode [4], and the high-frequency measurement through fast recovery diode/MOSFET [2, 5, 6]. These methods can measure the voltage drop across the two power terminals of a single device, meanwhile, block the high-voltage when the device is in the off-state. Nevertheless, the common practical challenges of these methods are: 1) It is of high complexity and cost as each switching device needs a measurement circuit; 2) It requires to connect the power terminals of individual switches as shown in Fig.1, which may be not always feasible due to the accessibility and safety concern for practical converters; and 3) It has multiple floating grounds, i.e., the middle-point of each phase-leg, if it requires to measure the on-state voltages of all devices in a single-phase or three-phase inverter. Another category of method is algorithm based without additional hardware, such as the digital-twin based approach applied for a Buck DC-DC converter in [7]. However, this method is highly dependent on the architecture of the power converters in terms of topology and control. The complexity in modeling and computation burden is likely to increase for converters with more components, such as a single-phase inverter or three-phase inverter system.

To address the above challenges, this letter proposes a measurement circuit connected to the middle-point of phase-legs as shown in Fig. 1. By leveraging the rich information of the single-phase inverter modulation, the voltage across the inverter output terminals contains the on-stage voltage information of all the IGBT switches T_1-T_4, and diodes D_1-D_4. The main features of the proposed method are: 1) it uses one circuit only to measure the on-state voltages (e.g., $V_{\mathrm{CE,sat}}$ of IGBT and V_{F} of diode) of all power semiconductor switches in the inverter, leading to reduced complexity, size, and cost; 2) it has better accessibility because of converter-level implementation; 3) the isolation stage with the proposed circuit can be simplified as it has one reference ground and two output signals only for a single-phase inverter monitoring. Therefore, a simpler galvanic isolation from the inverter stage can be implemented compared to component-level methods [4], by adding an isolation stage at the output side of the proposed measurement circuit. The initial concept of the study has been presented in a previous conference publication [8]. In this letter, the circuit implementation and the inverter demonstrator have been re-designed with improved performance in terms of noise, response speed, setting time, and accuracy level. The theoretical analyses of the limitations and applications are added. The reminder of the letter is as below: Section II presents the principle of the proposed method with a case study; Section III gives the proof-of-concept of the method based on experimental testing, followed by a conclusion in Section IV.

II. Concept and Implementation of The Measurement Circuit

A. Operation Principle of the Proposed Circuit

The proposed converter-level on-state voltage measurement circuit is shown in Fig.2. There is one reference ground only in the circuit, which simplifies the implementation. The circuit includes two symmetric parts with the ability to extract on-state voltages from the bipolar v_{ab}. The first part is composed of a signal depletion MOSFET M_1, fast-recovery diodes D_{a1} and D_{a2}, and a reference voltage source $V_{\mathrm{ref+}}$. The function of this part is to block any negative voltage and high positive voltage from v_{ab}, and to pass low positive voltage only. The second part composed of M_2, D_{a3}, D_{a4}, $V_{\mathrm{ref-}}$, has similar function, except for that it is used to block any positive voltage and high negative voltage, and pass low negative voltage from v_{ab}. If

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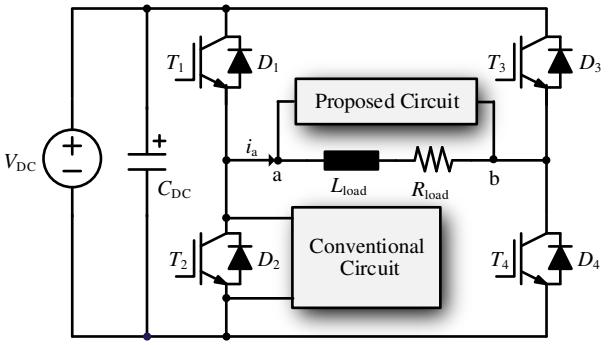

Fig. 1. Comparison of the proposed on-state voltage measurement method and conventional methods in terms of connection points to an inverter.

the gate-source voltage of M_1, for example, is zero, it is in on-state. If there is current flowing through M_1, the voltage drop in R_1 makes M_1 operates in linear mode. In addition, due to the negligible parasitic inductances, capacitances, and operation current (e.g., 1-4 mA in this case study) of the proposed circuit, the operation of the inverter is not impacted.

The operation modes of the first part are given in Fig.3 and discussed below.

- Model 1 (Fig.3(a)): if $v_{\rm ab}$ is negative, $D_{\rm a1}$ is blocked, $D_{\rm a2}$ is conducted, and M_1 is in the linear mode. The positive output $v_{\rm out+}$ is:

$$v_{\rm out+} = \frac{R_1}{R_1+R_2}\left(V_{\rm ref+} - V_{\rm Da2} - V_{\rm M1}\right) + V_{\rm Da2} + V_{\rm M1} \quad (1)$$

  R_1 is selected with a much smaller resistance than R_2, leading to a small $v_{\rm out+}$ (e.g., 1 V) at this model.
- Model 2 (Fig.3(b)): if $v_{\rm ab}$ is positively higher than $V_{\rm ref+}$, $D_{\rm a1}$ is conducted, $D_{\rm a2}$ is blocked, and M_1 is in the linear mode. Then, $v_{\rm out+}$ equals to the reference voltage $V_{\rm ref+}$.

$$v_{\rm out+} = V_{\rm ref+} \quad (2)$$

- Model 3 (Fig.3(c)): if $v_{\rm ab}$ is within 0 and $V_{\rm ref+}$, both $D_{\rm a1}$ and $D_{\rm a2}$ are conducted, M_1 is in linear mode as shown in Fig.3(c). It is noted that the voltage across M_1 and R_1 ($V_{\rm M1}$+$V_{\rm R1}$) must be as low as possible to make sure $D_{\rm a1}$ is conducted at this model, which is controlled by adjusting R_1 and R_2. Then, $v_{\rm out+}$ can be described as:

$$v_{out+} = v_{\rm ab} - V_{\rm Da1} + V_{\rm Da2} \quad (3)$$

In practice, $V_{\rm Da1}$ and $V_{\rm Da2}$ can be canceled with each other substantially under even temperature [6]. Thus, it is reasonable to assume that $v_{\rm out+}$ is equal to $v_{\rm ab}$. In addition, the impact of the used resistances caused by different temperatures can be neglected due to their negligible temperature coefficient (e.g., less than $\pm 100 {\rm ppm/K}$). Likewise, the second part of the circuit can measure the negative low-voltage from $v_{\rm ab}$. In conclusion, when the input signal $v_{\rm ab}$ is within the range of $V_{\rm ref-}$ and $V_{\rm ref+}$, the output voltage of the proposed circuit equals to $v_{\rm ab}$. Otherwise, the output voltage of the proposed circuit is clamped to $V_{\rm ref-}$ or $V_{\rm ref+}$. It is worth mentioning that the isolation is a common requirement for both component-level methods and proposed method in practical applications. In this letter, since the focus is to present the proof-of-concept of the proposed method, the isolation implementation is not demonstrated.

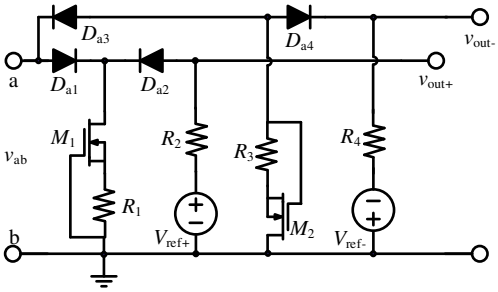

Fig. 2. Topology of the proposed on-state voltage measurement circuit.

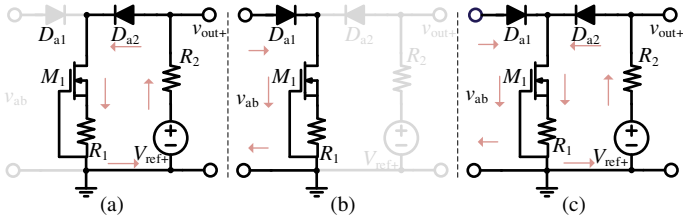

Fig. 3. Operation modes of half of the proposed measurement circuit (the $2^{\rm th}$ half is similar in operation modes): (a) when $v_{\rm ab}$ is negative voltage; (b) when $v_{\rm ab}$ is higher than $V_{\rm ref+}$; (c) when $v_{\rm ab}$ is between zero and $V_{\rm ref+}$.

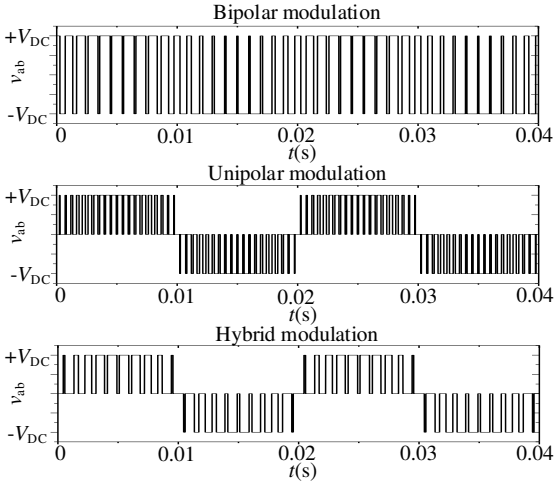

Fig. 4. Output voltage waveforms of full-bridge inverter with different modulations.

B. A Case Study of a Single-phase Full-bridge Inverter

The output voltage between the middle points of the phase legs varies with modulation schemes, as shown in Fig.4 [9]. Among them, the proposed method does not apply to the inverter with bipolar modulation only due to the absence of current freewheeling states. Nevertheless, this modulation is relatively less used compared to the other two due to lower efficiency and higher filter requirements [9]. An alternative

TABLE I
OPERATION STATES OF CONVERTER WITH UNIPOLAR SPWM MODULATION AND CORRESPONDING OUTPUT VOLTAGES OF THE PROPOSED CIRCUIT

States	v_{ab}	v_{out+}	v_{out-}
(a)	V_{DC}+V_{F1}+V_{F4}	V_{ref+}	-1 V
(b)	-$V_{CE,sat1}$-V_{F3}	+1 V	-$V_{CE,sat1}$-V_{F3}
(c)	V_{DC}-$V_{CE,sat1}$+$V_{CE,sat4}$	V_{ref+}	-1 V
(d)	-$V_{CE,sat4}$-V_{F2}	+1 V	-$V_{CE,sat4}$-V_{F2}
(e)	-V_{DC}+V_{F3}+V_{F2}	+1 V	V_{ref-}
(f)	$V_{CE,sat3}$+V_{F1}	$V_{CE,sat3}$+V_{F1}	-1 V
(g)	-V_{DC}+$V_{CE,sat3}$+$V_{CE,sat2}$	+1 V	V_{ref-}
(h)	$V_{CE,sat2}$+V_{F4}	$V_{CE,sat2}$+V_{F4}	-1 V

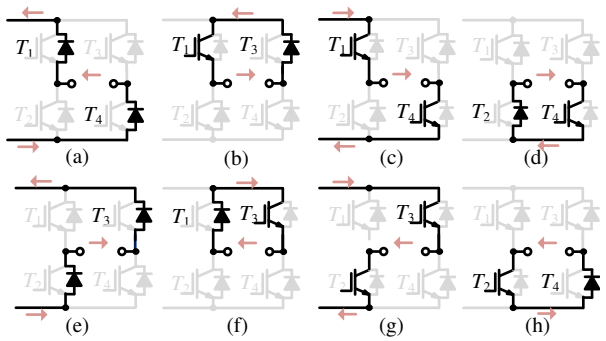

Fig. 5. Operation states of the full-bridge inverter with unipolar SPWM modulation.

solution for single-phase inverters with bipolar SPWM is to intentionally operate it under unipolar or hybrid modulation for short period of time for the on-state voltage measurement purpose. Therefore, from this perspective, the proposed method has a wide range of applications.

The corresponding eight operation states of the inverter with unipolar SPWM modulation are shown in Fig.5. Table I gives the v_{ab} for each operation state. V_{DC} is the dc-link voltage, $V_{CE,sat1}$-$V_{CE,sat4}$ denote the on-state voltage of T_1-T_4 respectively, and V_{F1}-V_{F4} denote the forward voltage of D_1-D_4, respectively.

It can be seen from Table I that the critical indicators $V_{CE,sat}$ and V_F of all IGBTs and diodes are included in v_{ab}. Then, the v_{ab} waveform over one fundamental period is drawn as shown in Fig.6(a). With the proposed circuit, the high DC-link voltages in v_{ab} are clamped to the positive and negative reference voltages, respectively, whereas the sum of $V_{CE,sat}$ and V_F is retained, as shown in Fig.6(b) and Fig.6(c). The specifications of v_{ab}, v_{out+}, and v_{out-} are listed in Table I. Then, the obtained sum of the on-state voltage of one IGBT and one diode could be useful for health monitoring. As the increase of the sum value or its change rate under a given condition indicates at least one of them degrades. In practice, any one or more of the IGBTs and diodes in one power module reaches the end-of-life implies the failure of the whole power module. Therefore, it is not necessary to separate the on-state voltage of the IGBT and the diode for health monitoring.

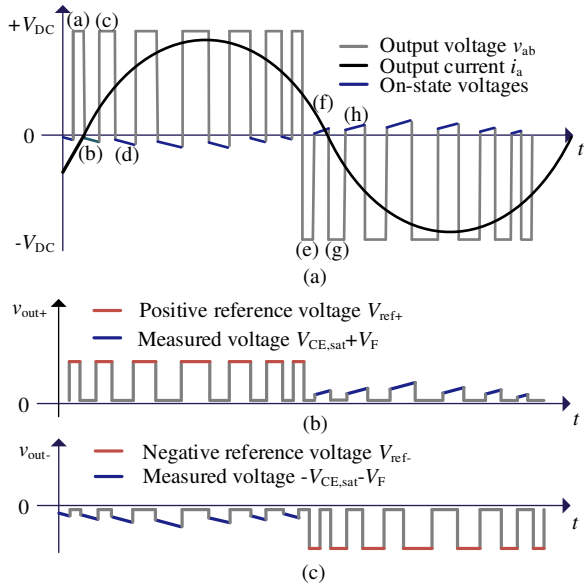

Fig. 6. Output voltage waveforms of the full-bridge inverter v_{ab} with unipolar SPWM modulation.

III. EXPERIMENTAL VERIFICATION

A full-bridge inverter is built with a 400 V DC-link voltage and 10 kHz switching frequency. A prototype of the proposed measurement circuit is developed and connected with the output terminals of the inverter, as shown in Fig.7. The rating of the used MOSFETs is 600 V/ 17 mA. R_1, R_3, and R_2, R_4 are SMD resistor with 200 Ω and 6.8 kΩ, respectively.

A commercial component-level on-state voltage measurement product is used for comparison purpose [10]. Fig.8(a) compares the measured $V_{CE,sat2}$, indicating that the proposed circuit has a comparable accuracy-level with this product. Fig.8(b) gives the dynamic response of the proposed circuit with a step-change of v_{ab} from -7.5 V to 6.5 V. When the input voltage is negative, the circuit operates in Model 1 as shown in Fig.3(a) and v_{out+} is 1 V. Once the input voltage increases to 6.5 V, the output voltage follows it with a fast dynamic response.

Fig.9(a) shows the measured waveforms of v_{ab}, v_{out+}, and v_{out-}. It demonstrates that both of the high positive and negative voltages of v_{ab} are clamped to the reference voltages, while the $V_{CE,sat}$ and V_F are detectable. Fig.9(b) and Fig.9(c) show the zoom-in waveforms of v_{out+} and v_{out-}, respectively. The sum of the on-state voltage of one IGBT and the corresponding diode shown in Table 1 can be obtained. The voltage spikes in Fig.9 are mainly attributed to the parasitic inductances of the module terminals, bus-bar, and the connecting wires between the inverter and the proposed circuit during the current commutation transient. they can be reduced by well designing the inverter and shorting the connecting wires, and do not impact the accuracy as only the steady-value is required during the data analysis step.

Only one point of each pulse in Fig.9(b) and Fig.9(c) is

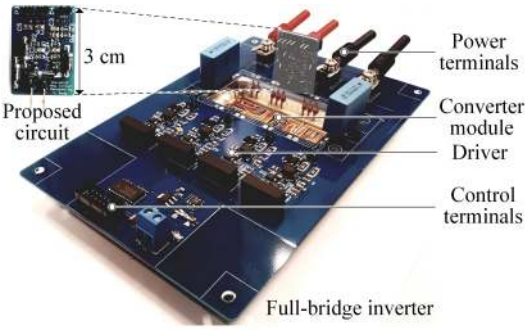

Fig. 7. Experimental prototypes of the full-bridge inverter and the proposed circuit.

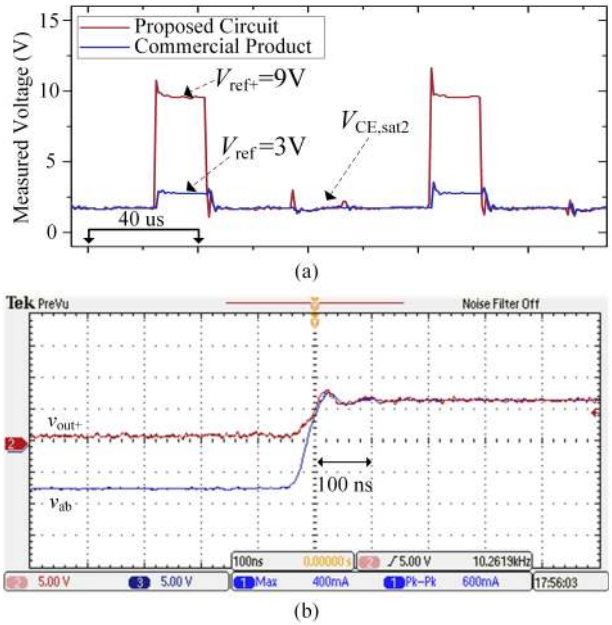

Fig. 8. Performance testing of the proposed circuit: (a) comparison with a commercial product [10]; (b) dynamic response with a step-change of v_{ab} from -7.5 V to 6.5 V.

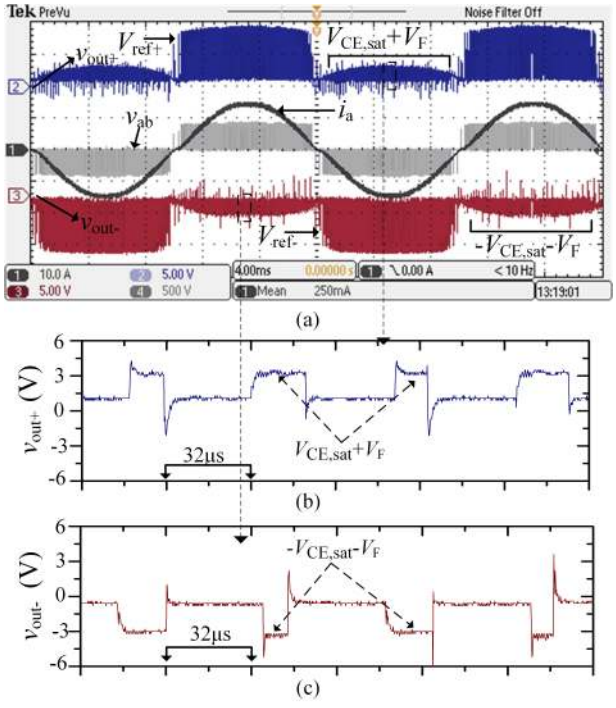

Fig. 9. Experimental results: (a) waveforms of the full-bridge inverter and the proposed measurement circuit (b) zoom-in $v_{\mathrm{out}+}$ (c) zoom in $v_{\mathrm{out}-}$.

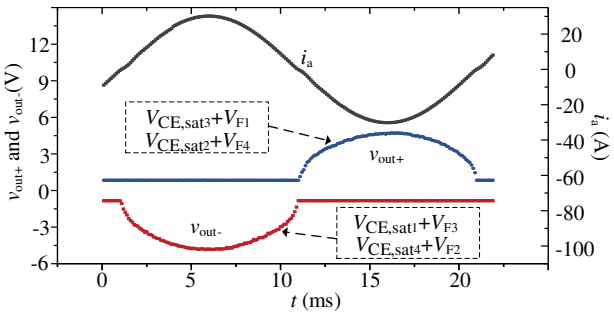

Fig. 10. Extracted on-state voltages during one fundamental period.

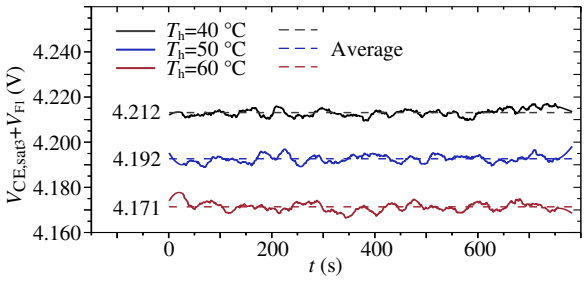

Fig. 11. Extracted $V_{\mathrm{CE,sat3}}$+V_{F1} when the instantaneous output current of inverter is within -20.5 A and -19.5 A at three heatsink temperature levels.

extracted with a sampling frequency double of the switching frequency as shown in Fig.10. The measured on-state voltages change with the current stresses within one fundamental period, which proves the proposed circuit can sense the change of $V_{\mathrm{CE,sat}}$ and V_{F}. Among them, $V_{\mathrm{CE,sat3}}$+V_{F1} and $V_{\mathrm{CE,sat2}}$+V_{F4} are included in $v_{\mathrm{out}+}$, $V_{\mathrm{CE,sat1}}$+V_{F3} and $V_{\mathrm{CE,sat4}}$+V_{F2} are included in $v_{\mathrm{out}-}$. They can be separated based on the operational states as listed in Table.I. The $V_{\mathrm{CE,sat3}}$+V_{F1} is sampled one time per fundamental period when the output current i_{a} is within -20.5 A and -19.5 A at three different levels of heatsink temperature T_{h}. Then, the sampled results over 1 s are averaged as shown in Fig.11, indicating the proposed method can detect the change of on-state voltage by 2 mV/°C.

IV. Conclusions

In this letter, the output voltage v_{ab} of a single-phase inverter is analyzed with different modulations and it is found that for the single-phase inverters with unipolar and hybrid modulations, the on-state voltages of all power semiconductors appear at v_{ab} during the current freewheeling states. Therefore, a converter-level circuit is proposed to extract the on-state

voltages of all power semiconductors from v_{ab}, which is verified theoretically and experimentally in this letter. This circuit achieves reduced complexity, size, cost, easy connection, and non-invasive measurement compared to existing solutions. In addition, the proposed circuit can follow the input voltage with a fast dynamic response. In principle, the proposed method is applicable to many converters composed of one or more phase legs.

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