A Cost-Effective Solution to Power the Gate Drivers of Multilevel Inverters using the Bootstrap Power Supply Technique

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***Abstract*–Multilevel inverters are traditionally seen as a step forward in DC/AC conversion, providing more output voltage levels, better quality of the generated waveform and lower switching losses than the two-level and can process higher voltages with a given forced commutated switch technology. There are also drawbacks associated with this technology: more switching devices and associated gate driver circuitry, more complex modulation and control of the DC-link capacitor voltage sharing etc, which as of now limit its application to the high voltage/power range. This paper proposes a cost-effective solution to implement the power supply needed for powering the gate drivers based on the bootstrap supply technology, which will not need isolated DC/DC supplies for each gate driver, reducing the overall cost of a multilevel assembly and making it more appealing for lower power applications.**

I. Introduction

Multilevel inverters [1]-[6] have been developed to cover the need for operation at high voltage/power ratings, where the IGBT switches have reached their technological limitation and putting devices in series would have posed dynamic voltage sharing problems. Three topologies are already student textbook material [7]: the cascaded H-bridge inverters having each isolated DC-links, the diode clamped and the flying capacitor multilevel inverters. Lately, hybrid multilevel structures have also been proposed [8]. Also, manufacturers of standard frequency converters [9] are starting to extend their product range with three-level inverter drives from the medium into the low power (kW) range. The reason of using multilevel topologies is that they offer better voltage quality and reduced switching voltage stress which is beneficial to increase the switching frequency (or operate at a given switching frequency with devices that have poorer switching behavior), minimize the size of filters and the effect of EMI/bearing currents in motors caused by common mode voltage. However, there are also some shortcomings: the need for additional components (isolated DC sources, DC-link capacitors or clamping diodes, gate drivers and their associated power supplies), increased complexity of the circuit/modulation/control (dc-voltage balancing or optimizing the power flow from the various DC sources used).

This paper proposes a low-cost solution to power the gate drivers for multilevel inverters (diode clamped and flying capacitors), which could be beneficial especially in the low power range (i.e. UPS), where the cost of the control electronics tends to be a limiting factor especially in situations where a large number of switching devices are needed [10].

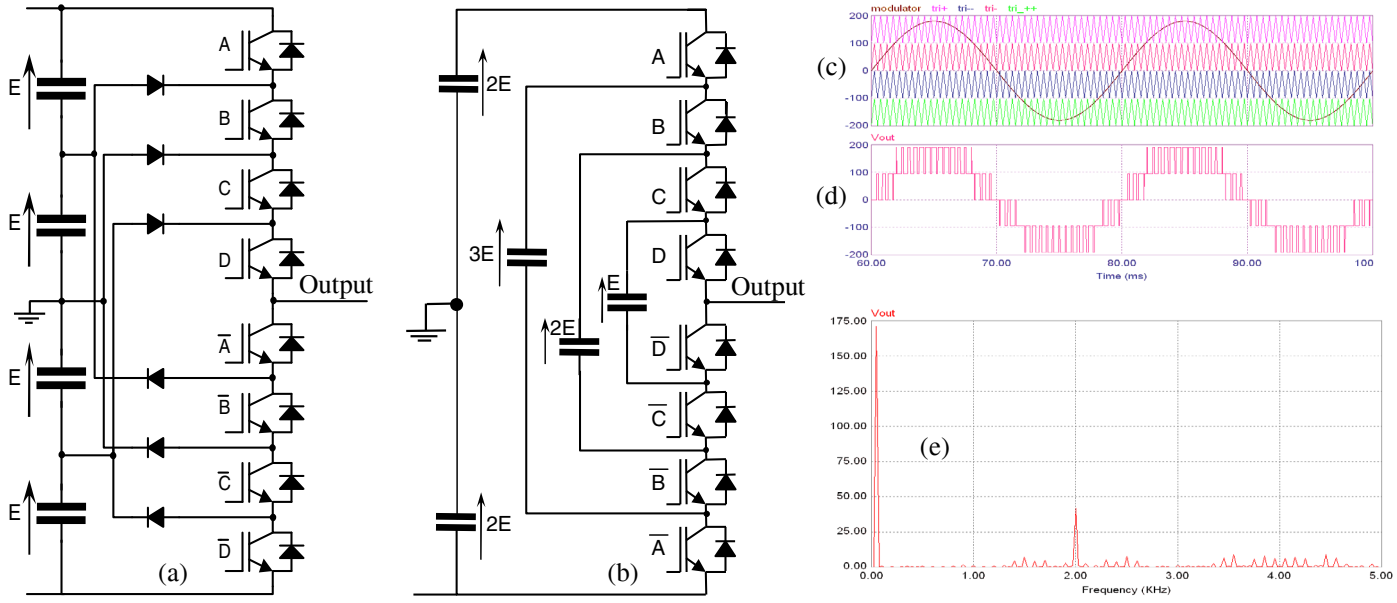

Fig. 1. Five-level voltage source inverters: (a) diode clamped topology; b) flying capacitor topology; c) carrier based multilevel modulation; d) output phase to supply midpoint voltage and; e) its corresponding FFT.

II. The Principle of Gate Driver Bootstrap Supply

Most of the power semiconductor devices used in building power electronic systems in the low-power range (hundreds W – few kW) are IGBTs or MOSFETs, which are devices that have a high impedance capacitive input and are voltage controlled. The gate drivers [10]-[14] normally have to be able to source/sink a large current only during the transition from off-to-on/off-to-on state, whilst during steady state (on or off) the current/power consumed is negligible. The voltage level that needs to be supplied to the gate via the gate resistor during the turn on is normally +15V, whilst applying 0V or even negative voltage (-15V) on the gate makes the switching device to turn off [13]. Negative voltage is normally used to speed up the turn-off process by removing much faster the stored charge in the gate-emitter/source capacitance. Also, applying negative bias voltage during the off state may reduce the leakage collector current. However, in the low power range, using a negative turn-off gate voltage is not providing as many benefits as in the medium/high power range, and this is why, it is very common to use 0V as turn off voltage on the gate.

The other aspect that is important when designing a power electronic system is the cost, which does not consist only of the power stage active and passive components, but also have to include the transducers, the digital control platform, the gate drivers and the power supplies necessary to provide the power to control the power semiconductor devices. Since the control is more or less the same, independent on the power level, it means that at low power level, where the cost of the power components is low, it is very important to find solutions to decrease the cost of any of these auxiliary components, and using 0V to turn off the power semiconductors, in conjunction to cost-effective ways of implementing the power supplies for some of the gate drivers may facilitate this.

Fig. 2 shows the topology of a three-phase two-level VSI having bootstrap power supplies to feed the gate drivers of the upper IGBTs. The operation is very simple: the gate driver supply that can feed directly with unipolar voltage the gate drivers of the bottom three switches, will charge the bootstrap capacitors C_1, C_2, C_3 via the bootstrap diodes D_1, D_2, D_3 every time the corresponding bottom switch Q_4, Q_5, Q_6 is turned on that causes the voltage drop across their collector-emitter to drop to a negligible level voltage, making the negative terminal of the bootstrap capacitor to be connected to the negative terminal of the isolated gate driver supply for the bottom switch. When the switches turn off, the negative terminal of the bootstrap capacitor is disconnected from the gate driver supply, and since this terminal is connected to the emitter of the upper switch, it provides a unipolar floating supply to its gate driver. This solution has the advantage of being very simple, but there are also some drawbacks: the commutation of the bottom switches is always needed to charge the bootstrap capacitors which may cause an undesired switching state to be applied to the output (especially at startup); since the bootstrap supply is unipolar, it does not allow the use of negative gate voltage to speed up the turn off process, with direct impact on having higher switching losses and limiting the power range where this solution can be used to low power (up to a few kW).

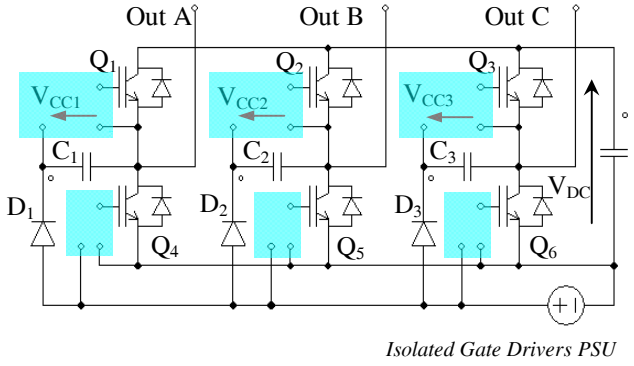

Fig. 2. Illustration of the way the bootstrap supplies are implemented in a three-phase two-level voltage source inverter.

III. The Proposed Multilevel Gate Driver Supply

In Fig. 1a and b, it can be seen that the topology of a multilevel diode clamped /flying capacitor inverter leg consists of series connected IGBTs. The principle of the bootstrap supply technique is based on charging the capacitor that would feed the gate driver of the upper switch in a two-level inverter from the gate driver supply of the switch underneath. Since one of the major drawbacks of the multilevel inverters is the large number of switches/gate drivers and power supplies for these gate drivers, applying the bootstrap supply solution to the multilevel inverter may solve at least the problem related to the large number of gate driver supplies.

The resulting topology of a multilevel inverter leg is shown in Fig. 3. Here, the additional components (clamping diodes or flying capacitors) have been omitted in order to suggest that the solution can be applied potentially to both multilevel topologies. However, it can be seen that when Q_1 is turned on, the bootstrap capacitor that can feed the gate driver of Q_2, C_1 is charged via the bootstrap diode D_1. Assuming that in the next step, Q_2 is then turned on, the bootstrap capacitor that can feed the gate driver of Q_3, C_2 is charged via the bootstrap diode D_2. Assuming that this sequence can be repeated successfully until Q_7, it can be seen that all capacitors that feed the gate drivers of the semiconductor switches in this inverter leg have now been charged. Even though this solution is very cheap and simple, a few disadvantages pointed also on the case of the two-level VSI, will appear: this strategy will always be limited to modulation schemes/modulation range where the bottom switches are frequently turned on; also since the voltage drop across the ON-state switch is small, but not negligible, having a large number of devices in series (7 in the case of a five level inverter) may decrease the voltage available to the gate driver of the upper switch at an unacceptably low level. In the following subsections, the correlation between the permitted switching states and the charging of the bootstrap capacitors will be derived in order to reveal any limitations related to the use of these multilevel inverter topologies.

A. Gate Driver Bootstrap Supply for Diode Clamped Inverters

Table I shows the permitted switching states and the corresponding output voltage for a five-level diode clamped inverter leg (Fig. 1a). The correlation between the switching

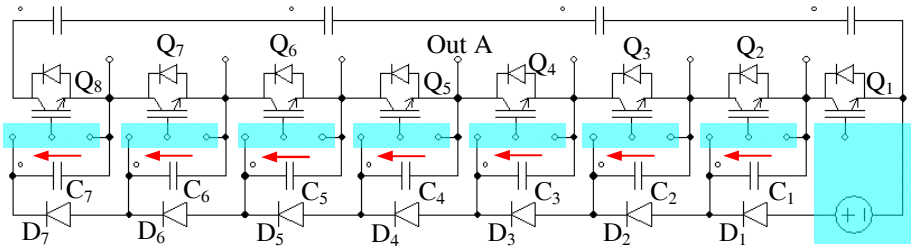

Fig. 3. Illustration of the way the bootstrap supplies can be used in a five-level diode clamped/flying capacitor voltage source inverter.

state and the charging of bootstrap capacitors (which one and from which source) is also revealed. Since there are only five permitted switching states in a five-level diode clamped inverter leg, it is clear that there are serious restrictions not only in producing the desired output voltage, but also in being able to properly charge all the bootstrap capacitors. For example, when the converter needs to deliver low level output voltages (i.e. driving a motor at low speed), using only the switching states that would produce the three smaller output voltages (-E; 0; +E) would be needed. However, the use of only these corresponding switching states will restrict the energy flow from the bottom gate driver supply $\overline{D}$ to the next one $\overline{C}$ which means that there will be no power to drive the corresponding gate drivers of the upper switches.

TABLE II
SWITCHING STATE, OUTPUT VOLTAGE AND CHARGED BOOTSTRAP SUPPLY FOR A 5-LEVEL DIODE CLAMPED INVERTER

ABCD	Vout	Charging bootstrap supply of	From bootstrap supply of
0000	-2E	$\overline{C}\ \ \overline{B}\ \ \overline{A}\ \ D$	$\overline{D}$
0001	-E	$\overline{B}\ \ \overline{A}\ \ D\ \ C$	$\overline{C}$
0011	0	$\overline{A}\ \ D\ \ C\ \ B$	$\overline{B}$
0111	+E	$D\ \ C\ \ B\ \ A$	$\overline{A}$
1111	+2E	$C\ \ B\ \ A$	D

This may not be a problem in applications where the modulation index always remains high (UPS) and where over a period of the modulating wave, all five switching states are used. This problem may also be overcome in three-phase applications where the load has a floating neutral (motor drives) and where redundant switching states that can easily allow the charging of the bottom bootstrap supplies whilst producing smaller voltages on the output side are available (i.e. selection of a zero voltage state that consist of connecting all load terminals to the most negative DC-link terminal).

The other possible solution is that instead of using a single DC/DC converter to feed the bottom power supply, two independent power supplies (for $\overline{D}$ and $\overline{C}$ gate drivers) are used whilst the rest are still fed using the bootstrap technique.

B. Gate Driver Bootstrap Supply for Flying Capacitor Inverters

Table II shows the permitted switching states, the corresponding output voltage and the correlation between the switching state and the charging of bootstrap capacitors (which one and from which source) for a five-level flying capacitor inverter leg (Fig. 1b). When comparing the number of available switching states and the possible ways of charging the bootstrap supplies with the diode clamped inverter topology, it can be concluded that the flying capacitor topology offers many more alternatives: four redundant switching states to synthesize the minor voltage level (-E/+E) and six redundant switching states to produce the zero voltage state.

TABLE II
SWITCHING STATE, OUTPUT VOLTAGE AND CHARGED BOOTSTRAP SUPPLY FOR A 5-LEVEL FLYING CAPACITOR INVERTER

ABCD	Vout	Charging bootstrap supply of	From bootstrap supply of
0000	-2E	$\overline{B}\ \ \overline{C}\ \ \overline{D}\ \ D$	$\overline{A}$
0001	-E	$\overline{C}\ \ \overline{D}\ \ D\ \ C$	$\overline{B}$
0010		$\left\{\overline{B}\ \ \overline{C}\right\}_1; B_2$	$\overline{A}_1; C_2$
0100		$\left\{\overline{D}\ \ D\right\}_1; A_2; \overline{B_3}$	$\overline{C}_1; B_2; \overline{A}_3$
1000		$\overline{C}\ \ \overline{D}\ \ D$	$\overline{B}$
0011	0	$\left\{\overline{B}\ \ \overline{C}\right\}_1; \{C\ \ B\}_2$	$\overline{A}_1; D_2$
0110		$\overline{B}_1; A_2; D_3$	$A_1; C_2; \overline{D}_3$
0101		$\overline{B}_1; A_2; \overline{D}_3; C_4$	$\overline{A}_1; B_2; \overline{C}_3; D_4$
1001		$\left\{\overline{C}\ \ \overline{D}\right\}_1; C_2$	$\overline{B}_1; D_2$
1100		$\left\{\overline{D}\ \ D\right\}_1; A_2$	$\overline{C}_1; B_2$
1010		$\overline{C}_1; B_2; D_3$	$\overline{B}_1; C_2; \overline{D}_3$
0111	+E	$\overline{B}_1; \{A\ \ B\ \ C\}_2$	$\overline{A}_1; D_2$
1011		$\overline{C}_1; \{B\ \ C\}_2$	$\overline{B}_1; D_2$
1101		$A_1; \overline{D}_2; C_3$	$B_1; \overline{C}_2; \overline{D}_3$
1110		$\{A\ \ B\}_1; D_2$	$C_1; \overline{D}_2$
1111	+2E	$A\ \ B\ \ C$	D

However, the multitude of redundant switching states is not available to satisfy only the need to provide charging of the bootstrap capacitors; since each inverter leg has its own flying capacitors, balancing their corresponding voltages to E/2E/3E levels can only be achieved by directing the load current with

positive/negative direction through the flying capacitors using an appropriate switching state succession. This means that the increased flexibility compared to a diode clamped counterpart, comes at the cost of increased control complexity.

The other interesting aspect is that if the converter has a high number of level, and is aimed at producing a voltage compatible with a 110/240Vrms AC voltage (i.e. the case of a UPS that delivers true sinusoidal output voltage, where in order to reduce the size of the switching current filter, a multilevel inverter topology is adopted), the level of the inner flying capacitor voltage (E) may be at a similar level to what is normally used for supplying gate drivers, therefore, the inner flying capacitor can be also used to provide power for switch $\overline{D}$ gate driver (Fig. 1b).

C. Designing the Bootstrap Circuit

The most important component in the bootstrap circuit is the bootstrap capacitor. This needs to be sized such that it can provide the current for its corresponding gate driver *k* but also the gate drivers that feed the upper switches (*k*+1 to *n*), during the maximum time, the lower switch that normally supplies power to it (Q_k in Fig. 3) is not gated. During all this time ($\Delta t_{nopulse-k}$), the allowed voltage discharge needs not only to cover the minimum voltage that the upper gate driver (*n*) needs to operate properly $V_{GD\min-n}$ but also the collector-emitter voltage drops across the switches in the whole string:

$$C_k \geq \frac{\left(i_k + \sum_{j=k+1}^{n} i_j\right)\cdot \Delta t_{nopulse-k}}{\left(V_{GD-1} - k\cdot\Delta V_{CEsat}\right) - \left(V_{GD\min-n} + \left(n-\left(k+1\right)\right)\cdot\Delta V_{CEsat}\right)} \quad (1)$$

Where V_{GD-1} is the voltage delivered by the common isolated DC/DC supply to the bottom switch gate driver. Since the voltage difference between charged/discharged state is more or less constant to all the bootstrap supplies and the current level decreases, the higher the switch is placed in the string, it means that the same will be true with the size of the bootstrap capacitors: the lower the device is placed in the string, the larger the size and its voltage rating; and vice versa for devices placed higher in the string. However, since the voltage to which the capacitor charges/discharges will decrease, the higher in the string the device is placed, a Zenner diode and a resistor need to be placed between the gate driver supply terminals and the corresponding bootstrap capacitor.

IV. Experimental Results

Two low-power laboratory prototypes of a diode clamped and a flying capacitor single-phase five-level voltage source inverters have been built as part of the second author's final year BEng in Electrical and Electronic Engineering project.

The generation of the PWM pulses needed by the five level multilevel converters depicted in Fig. 1a and 1b were generated using a microcontroller. Two different patterns, one for the low modulation index shown in Fig. 4a and one for high modulation index shown in Fig. 4b, were generated. These

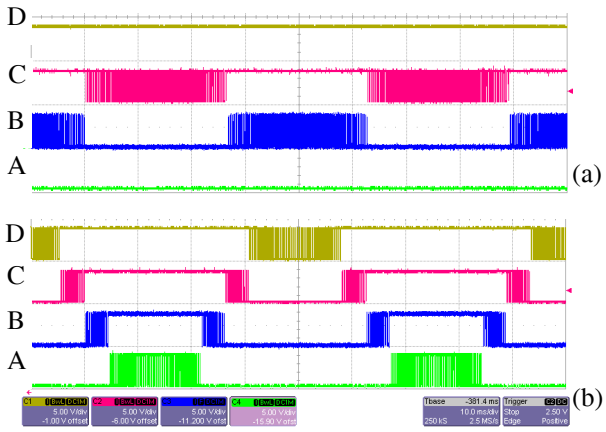

Fig. 4. The gate signals generated by the microcontroller: a) low modulation index; b) high modulation index.

pulses were then passed through a dead-time generation module, implemented in a CPLD device (XC95108) that also produced the gate signals for the opposite switches.

A. Evaluation of the Five-Level Diode Clamped Inverter

Fig. 5 shows the experimental results of the load voltage and current for the five-level diode clamped inverter operating with high modulation index. The voltage waveform is similar to typical multilevel voltage generation and since the load current is sinusoidal, it proves that the PWM modulation is properly implemented. Operation at low modulation index (m<0.5) was not possible (not possible to charge the bootstrap supplies).

Fig. 6 shows the evolution of the gate driver supply voltages for the upper switches (top side) and the lower switches (bottom side). These two sets of results were not acquired simultaneously, due to the fact that the oscilloscope had only four channels available. During this test, the DC-link voltage was applied first; also the PWM signals were available from the microcontroller. Then, the power supply for the bottom switch (bottom trace on the left plot) was applied. There is a delay between this moment and the moment when the voltage appears on the next bootstrap capacitors, due to the fact that the gate drivers have an undervoltage protection and also, that the bottom switch Q_1 (in Fig. 3) is turned on only when the modulating signal exceeds a given level.

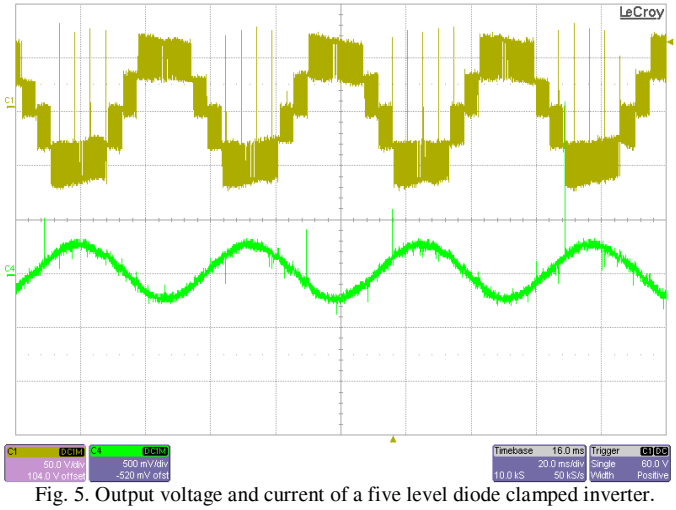

Fig. 5. Output voltage and current of a five level diode clamped inverter.

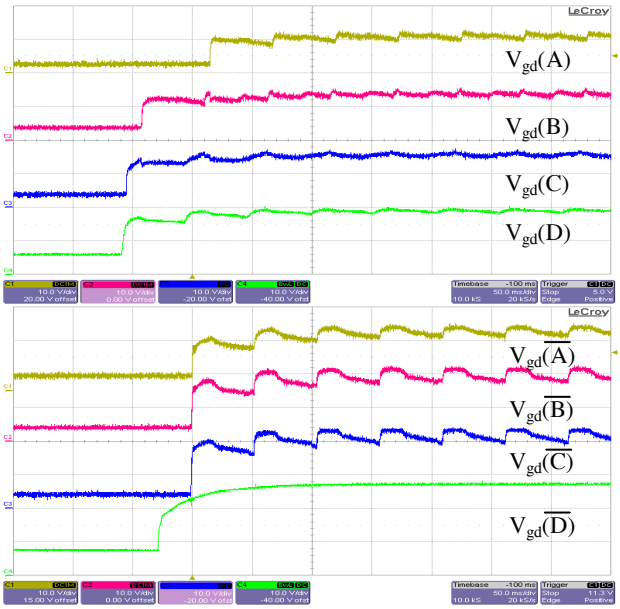

Fig. 6. Voltage seen across the bootstrap capacitors of the top (upper plot) and bottom (bottom) four switches of a five-level diode clamped inverter.

The loss in amplitude for the capacitor voltage is clear: from approx 20 V available for the bottom switch to approx 12 V for the forth switch from bottom. The delay noticed in the appearance of the bootstrap supply for the upper switch in the upper plot is also due to the delay in gating the switch Q_7 (in Fig. 3) compared to Q_6.

B. Evaluation of the Five-Level Flying Capacitor Inverter

The experimental evaluation of the five flying capacitor inverter using bootstrap power supplies was performed in two different situations: (standard mode) by using the same gate signals as shown in Fig. 4 a and 4b, and (swapped mode) by using some of the redundant switching states available, which were obtained by swapping the gate signals A with B and C with D every four/eight switching periods (see Fig. 7a and b). In this way, a simple method to test the effect of using redundant switching states on the operation of the bootstrap supplies is implemented. It should be noted that no attention has been paid to implement voltage balancing of the flying capacitors; all flying capacitors have been powered from isolated rectifiers.

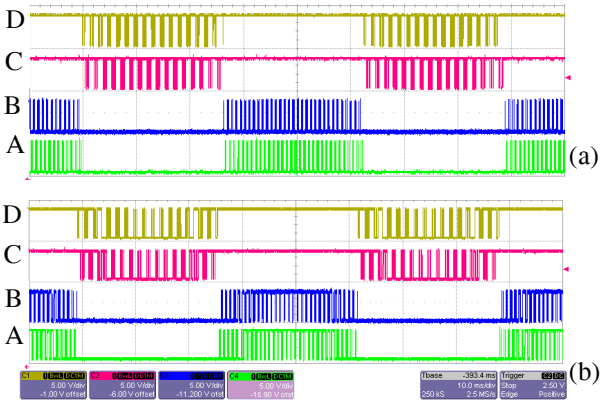

Fig. 7. The gate signals supplied to the flying capacitor switches in swap mode at: a) low modulation index; b) high modulation index.

Fig. 8 shows the output voltage and current of the five level flying capacitor operating at high modulation index, using the standard gating sequence presented in Fig. 4.

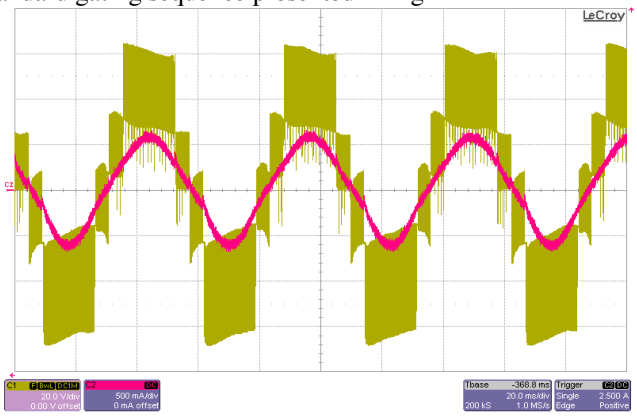

Fig. 8. Output voltage and current of a five level flying capacitor inverter operating at high modulation index with standard gating signals (Fig. 4b).

Operation at low modulation index was not possible and the reason is visible in Fig. 9, where the bootstrap supplies of the upper four devices for low (left side) and high (right side) modulation index, are shown.

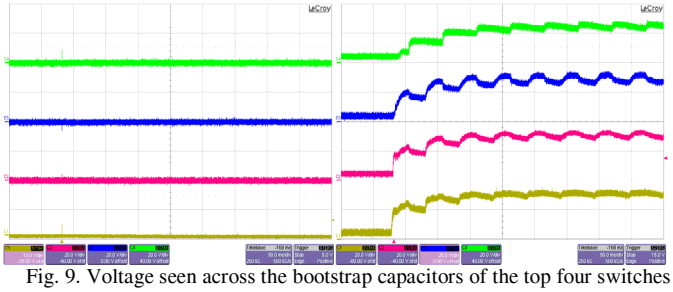

Fig. 9. Voltage seen across the bootstrap capacitors of the top four switches of a five-level diode clamped inverter at low (left side) and high (right side) modulation index for standard gate signal generation.

When the swapped gating generation signal is enabled, as expected, there is voltage available for all upper bootstrap capacitors, at both the low and the high modulation index, as shown in Fig. 10.

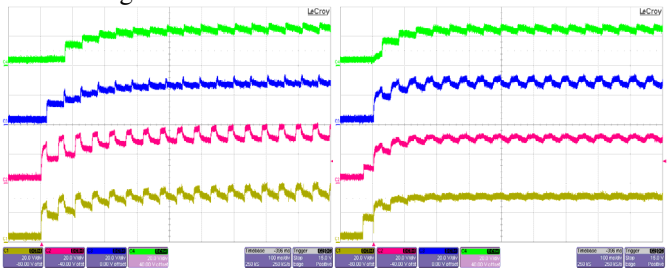

Fig. 10. Voltage seen across the bootstrap capacitors of the top four switches of a five-level diode clamped inverter at low (left side) and high (right side) modulation index for swapped gating signal generation.

The load voltage and current produced by the five level flying capacitor inverter operating at low and high modulation index is revealed in Fig. 11 and 12. At low modulation index, the zero voltage level is slightly distorted due to the fact that the load AC current was causing deviation of the mid point DC-link potential.

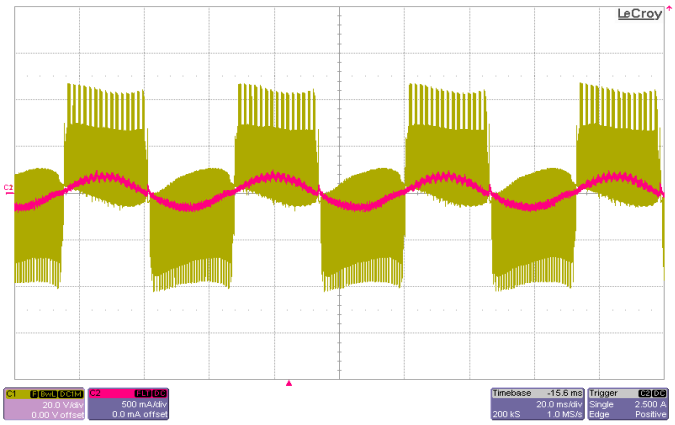

Fig. 11. Output voltage and current of a five level flying capacitor inverter operating at high modulation index with swapped gating signals (Fig. 7a).

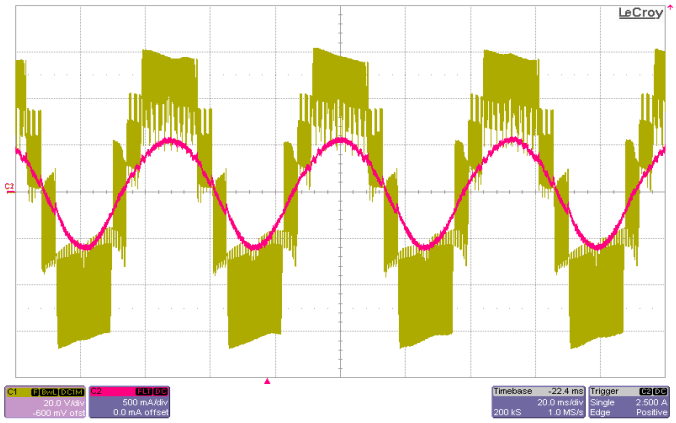

Fig. 12. Output voltage and current of a five level flying capacitor inverter operating at high modulation index with swapped gating signals (Fig. 7b).

Also, because there was no mechanism in place to balance the flying capacitor voltages to E/2E/3E voltages, there is a slight voltage ripple at the swapping frequency, caused by the fact that due to slight imbalance in the flying capacitor voltages, redundant switching states were not producing identical output voltages. However, this does not have a major effect on the output current.

The last test was to investigate the response of both, the standard and the swapped gating schemes to a repetitive low-high-low modulation index transient. Fig. 13a and 13b show the voltage across the upper four bootstrap capacitors that correspond to the standard and swapped operation mode. It can be seen that for the standard mode, the bootstrap supplies periodically rise and fall, depending on whether the modulation index is higher or lower than 0.5. For the swapped mode, once the bootstrap capacitor voltages rise, they remain steady. Fig. 14a and 14b show the effect on the output voltage and currents of the same test. For the standard gating mode, the output voltage is still present during the low modulation index; however there is a large imbalance between the positive and negative half waves, that reveals that the generated voltage is not symmetrical, caused probably by the fact that some of the upper devices in the inverter leg stop responding to the gate commands. The cause is that most gate drivers have a threshold voltage level below which the operation of the gate driver is inhibited for protection purposes.

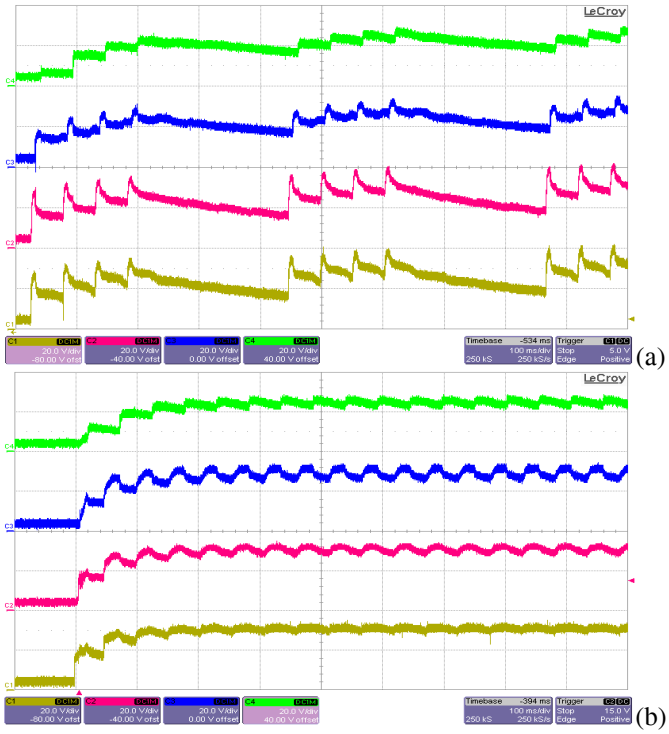

Fig. 13 Voltage seen across the bootstrap capacitors of the top four switches of a five-level flying capacitor inverter operating in a) standard and b) swapped gating mode during a periodical low-high modulation index transient.

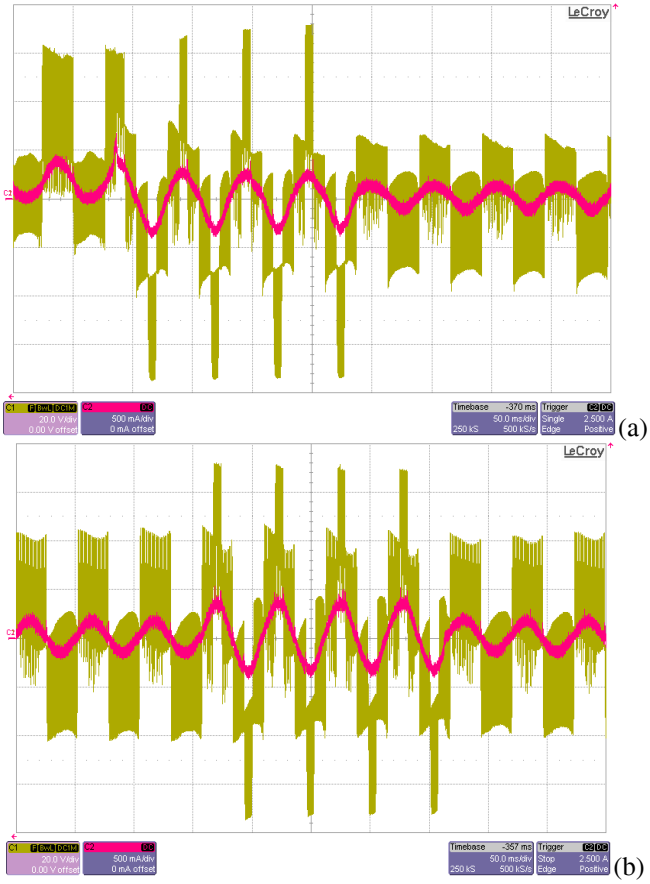

Fig. 14. Output voltage and current of a five level flying capacitor inverter operating with a) standard and b) swapped gating signals during a periodic low-high modulation index transient.

For the swapped mode, the waveform generated by the five-level flying capacitor inverter remains steady and symmetrical, which also proves that the gate drivers remain properly fed.

V. CONCLUSIONS

This paper proposes the use of the bootstrap supply technique to power the gate drivers for the switches of a multilevel inverter in a very cost effective way. An analysis of the impact of the switching states on the potential to charge the various bootstrap capacitors is carried out, that reveals the limitations of the diode clamped topology. It also reveals that the flying capacitor topology has plenty of alternatives to provide charging of the bootstrap capacitors. A design procedure for the size of the bootstrap capacitors is given.

Both five-level inverter topologies are practically implemented at a low power level in order to experimentally demonstrate via steady-state and transient testing, the viability of the proposed solution. In order to fully analyze the proposed solution, a swapped mode of the gating signals, which was possible only for the flying capacitor inverter, is proposed, proving that even though both converters use the same PWM signals, the flying capacitor inverter is superior and able to operate in the whole modulation index range when having its gate drivers powered from bootstrap supplies.

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