A Current-based Method for Short Circuit Power Calculation under Noisy Input Waveforms*

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ABSTRACT

An accurate model is presented to calculate the short circuit energy dissipation of logic cells. The short circuit current is highly dependent on the input and output voltage values. Therefore the actual shape of the voltage signal waveforms at the input and output of the cell should be considered in order to precisely calculate the short circuit energy dissipation. Previous approaches such as the approximation of the crosstalk induced noisy waveforms with saturated ramps can lead to short circuit energy estimation errors as high as an order of magnitude for a minimum sized inverter. To resolve this shortcoming, a current-based logic cell model is utilized, which constructs the output voltage waveform for a given noisy input waveform. The input and output voltage waveforms are then used to calculate the short circuit current, and hence, short circuit energy dissipation. A characterization process is executed for each logic cell in the standard cell library to model the relevant electrical parameters e.g., the parasitic capacitances and nonlinear current sources. Additionally, our model is capable of calculating the short circuit energy dissipation caused by glitches in VLSI circuits, which in some cases can be a key contributor to the total circuit energy dissipation. Experimental results show an average error of about 1% and a maximum error of 3% compared to SPICE for different types of logic cells under noisy input waveforms including glitches while the runtime speedup is up to a factor of 16,000.

1. INTRODUCTION

Accurate power estimation is a critical step in the analysis and design of CMOS circuits in nanometer process technologies. The difficulty is mostly due to (a) input pattern dependence i.e., accurate power calculation requires knowledge of a "typical" or "expected" input stream, and (b) variability of the shape of the input signal waveform due to variations in key physical and electrical characteristics of CMOS logic cells and interconnects and/or different sources of noise, such as DC drop on supply lines and crosstalk noise on signal lines. While the first issue has been addressed in the past by developing various statistical or probabilistic power estimation methodologies [1][2], the latter issue has not received much attention by the low power design community. To partially address this shortcoming, the present paper seeks to develop a short circuit power calculation method under noisy signal waveforms.

Power consumption in CMOS VLSI circuits comprises of three components: switching, short circuit (SC), and leakage. The switching component of power dissipation refers to the power consumed to cause a gate output transition and follows the well-known $P_{sw} = 0.5 C_L V_{dd}^2 f \alpha$ where f is the clock frequency and α is the expected number of output transitions per clock cycle. For a detailed treatment, the reader may refer to [3]. The next component is the SC (or rush-through) power dissipation. The SC power is consumed by the current flow between the power rails (i.e., power supply to ground) through a direct current path which is temporarily established during an output transition. Therefore, the SC current at each time instance depends on the operation region of the transistors in the logic cell, which means that it is dependent on both the input and output voltage values. A well-known equation for time-averaged SC power dissipation is [4]: $P_{sc} = \frac{1}{12} k \tau_{in} (V_{dd} - 2V_T)^3 f \alpha$ where τ_{in} is the input transition time, V_T is the threshold voltage of transistors, and k is the effective transconductance parameter of the logic gate. The leakage component of power dissipation (which is rising very fast compared to the switching component due to lower V_T values and thinner gate oxides) accounts for the subthreshold current conduction, gate oxide tunneling currents, and reverse-biased p-n junction currents. For a detailed treatment, the reader may refer to [5].

The focus of this paper is on the SC energy dissipation.[1] For years, it has been stated and generally accepted that the SC current can be made small (say less than 10% of the switching power) by following a few simple design guidelines e.g., do not overdrive a load and do not allow the transition time (inverse of the slew rate) of the intermediate signals in a circuit to become too long. We will show in this paper that the SC energy dissipation can be comparable to other sources of energy dissipation even for a well-designed circuit in current CMOS designs (e.g., refer to Figure 4(a) and (b) in section 4.) This is mostly due to the increasing effect of noise, primarily crosstalk noise and its impact on the shape of the voltage signal waveforms inside the circuit. The increase in the transistor packing density as well as the clock frequency of the VLSI circuits increases the effect of capacitive crosstalk noise; the interconnect lines get thicker and narrower (and longer in case of global interconnects,) which result in the aggravation of crosstalk noise amplitude. This phenomenon in turn results in more distorted voltage signal waveforms and tends to increase the effective transition time of the signal waveforms that are subjected to crosstalk noise.

The remainder of this paper is arranged as follows. Next section brings a review of the previous SC power calculation techniques. In section 3 our current-based logic cell circuit model for SC power calculation is described. Section 4 presents our

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[1] Since the operation frequency of the circuit, f, is assumed to be fixed during the analysis and optimization steps that we consider in this paper and recalling $P = E \cdot f$ relation, we alternately use "energy calculation" and "power calculation" in this paper.

experimental results for different types of input waveforms as well as logic cells. Finally, section 5 provides a description of our future work and conclusions.

2. BACKGROUND

Most of the previous work on SC power has mostly focused on the development of closed-form analytical expressions [4],[6]-[10]. These approaches, which generally attempt to solve a set of differential equations for a switching inverter loaded with an effective capacitive load, lack accuracy due to their dependence on simple device models and assumptions made regarding the device operation during signal transitions.

Another group of approaches pre-characterize the average SC current with respect to the input signal transition time and capacitive output load. This method is very similar to the one used in static timing analysis (STA) tools, where the logic cell delay and output voltage signal transition time are characterized as a function of the input transition time and capacitive output load. One such technique is the work by Dartu et al in [11], which pre-characterizes the SC energy for a logic cell as follows:

$$E_{sc} = V_{dd} \int_0^\infty i_{sc}(t)dt = g(t_{in}, C_L) \qquad (1)$$

where i_{sc}(t) and E_{sc} denote the SC current and energy dissipation for one output signal transition, respectively. E_{sc} is empirically characterized in terms of k-factor type equations. The resulting pre-characterized lookup tables, $g(t_{in},C_L)$ are inherently incompatible with arbitrary waveform shapes, and thus, fall apart when processing noisy inputs such as crosstalk-induced noisy waveforms (c.f. Figure 4.b for a comparison between the k-factor based lookup tables and the proposed current-based method.)

More recently, Acar et al in [12] proposed a practical methodology that finds the maximum SC current in the linear and saturation regions of the device operation, and then utilizes triangular waveform approximation based on those peak current values to predict the SC energy dissipation during an output transition of a CMOS logic cell. This methodology uses timing rules of the conventional STA tools, where cell behaviors are pre-characterized as a function of the input slew and output load capacitance. Unfortunately, these models are not well-suited to deal with crosstalk-induced noisy waveforms. More generally, this technique suffers from the fact that SC current waveform cannot be well-modeled by a triangular shape, which is especially true when crosstalk-induced noisy waveforms are considered (cf. Figure 4.)

The major shortcomings of the previous modeling techniques in both cell output voltage and SC current calculation are summarized as follows: a) the impact of the shape of the input voltage waveform is ignored, b) the Miller effect in output voltage calculation is ignored, and c) the output load is approximated by an effective capacitance.

Current-based modeling has proven to be a highly effective approach for delay calculation in STA tools [13]-[17]. Croix et al in [13] proposed a model in which a pre-characterized current source is utilized to capture the non-linear behavior of the logic cell with respect to the input and output voltage values. The computed output voltage waveform is time shifted by a pre-characterized value to compensate for a timing offset with respect to SPICE results. Unfortunately, the parasitic effects (e.g., the Miller parasitic effect) are not modeled accurately in this work. Keller et al in [14] presented a more accurate model by considering a Miller capacitance. In their work, a pre-characterized current source similar to that of [13] is used. The parasitic components, namely the Miller and the output capacitances, are assumed to be fixed regardless of the input and output voltage values. Based on our analysis and simulation data, these parasitic capacitances can vary by orders of magnitude depending on cell input and output voltage values. The assumption of constant values can thus create significant inaccuracy especially for complex cells.

In [15] this weakness is resolved by introducing a nonlinear output capacitance model. The nonlinearity of the input of the logic cell is captured by a two-stage RC section. The current source model in [16] models each input and output pin of the cell with a nonlinear resistor and nonlinear capacitor, each of which is dependent on all the input voltage values and the output voltage. Since the complexity of the model is exponential in the number of inputs, the proposed model becomes very complex for logic cells with more than two inputs and this can make the model impractical for a STA tool. Finally this model does not address the effect of process variations on cell delay analysis. We presented a statistical STA technique in [17] to resolve the shortcomings of [13]-[16]. Interested reader may refer to the paper for details. We point out that none of the above-mentioned current based approaches (including [17]) have been developed for or applied to the SC power analysis.

The goal of this paper is to devise an accurate SC power calculation method. The aforesaid weaknesses of the previous techniques are all resolved by our current-based model, which considers the parasitic effects of a logic cell, including the Miller effect. It can process input voltage waveforms of arbitrary shapes, and hence, construct the exact output voltage waveform. The output voltage can be found for an arbitrary load, i.e., there is no need for an effective capacitance approximation. The nonlinear behavior of the SC current is captured by generating, during a pre-characterization step, a lookup table for each cell with the input and output voltage values as its keys and the SC power as the returned value.

We use the term *hazard* to refer to an unwanted full-rail spurious transition on a signal line. Hazards give rise to both switching and SC power dissipations. A *glitch*, on the other hand, refers to an incomplete spurious transition (half-rail swing) on a signal line. Although these glitches can give rise to switching power dissipation, their impact on the circuit power is mostly in the form of the SC power dissipation. It is easy to construct an input glitch for a CMOS inverter that will create a DC path between the power and ground rails at the output of the inverter over a long period of time, thus resulting in a significant amount of SC power dissipation that far exceeds any switching power dissipation (even for the case that the input glitch is passed on to the output.) Glitches are thus an important contributor to circuit power dissipation. Modeling the glitch SC current as a function of the glitch characteristics such as its shape is a difficult task. Furthermore, signal glitches are usually ignored by the timing analysis tools when they do not lead to the circuit delay change while these glitches can significantly increase the amount of SC power dissipation in the circuit, and hence, cannot and should not be ignored by the power analysis tool. Our current-based model can accept any type of glitches at the input of the logic cell and create the corresponding output voltage waveform to accurately construct the respective SC current waveform.

To the best of our knowledge, our model is the only one that can construct actual shape of the SC current waveform for any type of input voltage waveform, including glitches. The accuracy improvement by our model over the existing approaches is significant. It is worth mentioning that our current-based

approach utilizes the cell parasitic and current data that are pre-characterized for timing analysis purposes, and hence, there is no extra complexity for the pre-characterization step.

3. A CURRENT-BASED MODEL FOR SHORT CIRCUIT POWER

This section describes our current-based logic cell model for the purpose of SC energy calculation (which we shall call CSPC for *Current-based Short circuit Power Calculator*.) Our model accurately computes the output voltage waveform given the input voltage waveform by using a current-based model. The SC current value at each time instance may be obtained by using a pre-characterized lookup table with the input and output voltage values of the cell as the keys to the table.

3.1 Current-based Circuit Model to Calculate the Output Voltage Waveform

As mentioned earlier, accurate consideration of the shape of the voltage waveforms at the input and output of a logic cell is crucial for calculating its SC current. We enhance the current-based circuit model of [17] to calculate the output voltage waveform (c.f. Figure 1.) The model consists of two main components, namely, parasitic capacitances to model the loading at input and output nodes of the cell and the Miller effect between the two nodes, as well as a current source at the output node to model the nonlinear behavior of the logic cell. Each component is in turn a function of the input and output voltage values. As a result, our proposed cell model is represented by the following KCL equation, which essentially models the current at the output pin of the cell during switching:

$$i_o + I_o(V_i,V_o) + (C_o(V_i,V_o) + C_M(V_i,V_o))\frac{\Delta V_o}{\Delta t} - C_M(V_i,V_o)\frac{\Delta V_i}{\Delta t} = 0 \qquad (2)$$

where the Miller capacitance $C_M(V_i,V_o)$ and output capacitance $C_o(V_i,V_o)$ values are pre-characterized through a series of SPICE-based transient simulations, in which saturated ramp input and output voltages are applied to input and/or output nodes while the output current is monitored. Two-D lookup tables are used to store $C_M(V_i,V_o)$ and $C_o(V_i,V_o)$ values.

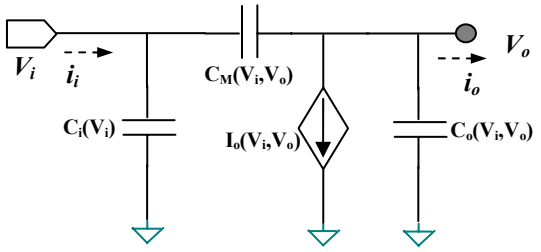


Figure 1. Our current-based circuit model for a logic cell.

The amount of current sourced by a logic cell in response to DC voltage levels on the input and output pins of interest, $I_o(V_i,V_o)$, is also determined for each logic cell by sweeping the DC values of input and output voltages and measuring the current sourced by the cell output pin in SPICE. As a result, to model the nonlinear behavior of a logic cell with respect to input and output voltage values, a two-D lookup table is created to store the values of $I_o(V_i,V_o)$.

Precise estimation of output load is critical for accurate output voltage calculation of a cell. The output node of a cell is usually connected to several fanout cells through some interconnect. The input capacitances of fan-out cells should hence be considered as part of the load for output voltage calculation of the driver cell. The following equation is used to characterize the input capacitance seen at the input of a cell:

$$i_i = \{C_i(V_i) + C_M(V_i,V_o)\}\frac{\Delta V_i}{\Delta t} - C_M(V_i,V_o)\frac{\Delta V_o}{\Delta t} \qquad (3)$$

A SPICE-based transient analysis is used to determine C_i. In this analysis, a saturated ramp is applied to the input, while the output node is connected to a DC voltage source, and the input current, i_i, is measured. Although the input capacitance, C_i, is a function of the input and output voltage values, in practice, an input-voltage-dependent C_i is all that can be efficiently utilized. This is because when calculating the output voltage waveform of a logic cell, the output voltage values of its fanout cells are unknown, and therefore, calculation of C_i values of the fanout cells cannot make use of any information about the output voltage levels of these fanout cells. That is why making C_i dependent on V_o is not useful in practice. Note that Equation (2) is sufficient for calculating the output voltage waveform, while Equation (3) is used to characterize C_i.

The logic cell pre-characterization steps of our model are load-independent, because the model components are characterized as a function of the input and voltage values rather than the input slew and output effective capacitance. Therefore the output voltage waveform can be constructed for a given input voltage waveform in the presence of an arbitrary load. Note that the current drawn by the load can always be written as a function of the output voltage of the logic cell and the load components. To do so, it is convenient to derive this equation in Laplace domain and then calculate it in the time domain by using the inverse Laplace transform techniques. Using this current component for the load, a KCL equation at the cell output node can be written, which is a function of the cell output and input voltages, the pre-characterized cell components, and the load electrical parameters. For simplicity, in the remainder of this section, we show the KCL equation for a simple capacitive load C_L (i.e., the current component for the load is simply $C_L\Delta V_o/\Delta t$.)

$$C_L\frac{\Delta V_o}{\Delta t} + C_o\frac{\Delta V_o}{\Delta t} + I(V_i,V_o) + C_M\frac{\Delta V_o}{\Delta t} - C_M\frac{\Delta V_i}{\Delta t} = 0 \qquad (4)$$

Equation (4) can be rewritten with respect to output voltage values, resulting in:

$$V_o(t_{k+1}) = V_o(t_k) + \frac{C_M\left(V_i(t_{k+1}) - V_i(t_k)\right) - I(V_i,V_o)\Delta t}{C_L + C_o + C_M} \qquad (5)$$

The accuracy of our current-based model in output voltage construction is presented in section 4. Next we will see how the high accuracy in output voltage waveform construction will be helpful in calculating the SC energy dissipation.

3.2 Short Circuit Current Waveform Calculation Using CSPC

The SC current of a logic cell is a non-linear function of the cell input and output voltage signals. Therefore, we pre-characterize the SC current of each cell with a two-D lookup table with the input voltage and output voltage values as the keys to the tables and the SC current as the table output. Having the input voltage, the output voltage waveform can be constructed by using our current-based model, which was described in section 3.1.

A SPICE-based pre-characterization process for SC current is performed. For each cell the current flow from V_{dd} to Gnd

terminals through the combination of pull-up and pull-down sections of the logic cell are evaluated while the input and output voltage values are set to a DC value ranging from 0 to V_{dd}. This pre-characterization is similar to the one explained in section 3.1 which was performed to measure $I_o(V_i,V_o)$. Figure 2 shows this process for a simple inverter logic cell. The zero voltage supplies, V_{M1} and V_{M2}, are added for the purpose of measuring the current flow through the pull-up and pull-down sections of the cell while V_{CH1} and V_{CH2} are added to provide input and output nodes with DC values. The SC current, $I_{sc}(V_i,V_o)$, is simply the minimum of the currents passing through V_{M1} and V_{M2}. A two-D lookup table is then created to store the $I_{sc}(V_i,V_o)$ values. Note that this table models the nonlinear behavior of the cell SC current with respect to the input and output voltage values. The current-based model is replacing the traditional look up table based models in STA tools. As a result characterization for generating the parameters for CSPC model is already being done. Complexity of this characterization step does not increase by adding the SC power calculation to the STA.[2]

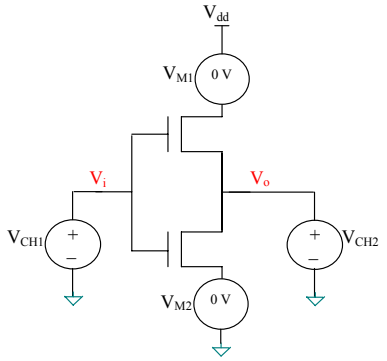


Figure 2. The SC current measurement during cell pre-characterization for our CSPC model.

4. EXPERIMENTAL RESULTS

To show the effectiveness of CSPC, the model was compared with Hspice simulations [18]. Waveforms with arbitrary shapes, ranging from simple saturated ramps to crosstalk-induced noisy ones with voltage fluctuations as high as 85% of V_{dd}, were applied to inputs of different logic cells. The set of experiments involved various logic cells, such as simple inverter and NAND gates, as well as complex cells such as AOI (And-Or-Invert) gates. Figure 3 shows comparison of CSPC results with Hspice for some examples of crosstalk-induced noisy waveforms given to a minimum sized inverter in our 130nm cell library with a V_{dd} of 1.2 volts. As seen, the output waveforms generated by CSPC closely match those generated by Hspice.

Figure 4 shows another comparison with Hspice for some examples of crosstalk-induced noisy waveforms given to a minimum sized inverter with a FO4 loading in our 130nm cell library. Figure 4(a) is for the case where only one aggressor is injecting the noise. The transition time at the input node of the aggressor and victim lines is set to 300ps. The input voltage, output voltage, and SC current waveforms obtained by CSPC as well as Hspice are depicted. It is seen that the CSPC-generated waveforms closely match the corresponding ones generated by Hspice. Figure 4(b) shows another example with the identical experimental setup, except for the number of aggressor lines which is two in this case. This figure shows that the accuracy of CSPC does not degrade no matter how distorted the input voltage waveform is. We note that the SC energy dissipation related to Figure 4(a) are 2.68pJ (2.78pJ) by Hspice (CSPC.) Results for the case of Figure 4(b) are 15.65fJ (15.74fJ). This constitutes more than 5X rise in SC energy dissipation when the number of aggressors is increased from one to two. This is because as the number of aggressor lines increases, the duration in which both NMOS and PMOS are operating increases; this in turn significantly raises the SC energy consumption level. Figure 4(c) illustrates the results for a minimum size FO4-loaded NAND3 for which a crosstalk noise is injected to one of the inputs through three aggressors, while the other two inputs assume a non-controlling, steady, high level logic value. The transition time at the input driver of the aggressor line as well as that of the NAND input victim line are set to 300ps. The SC energy dissipation for this case is 27.71fJ (28.01fJ) by Hspice (CSPC), meaning that the error of CSPC is less than 1.1% in this case.

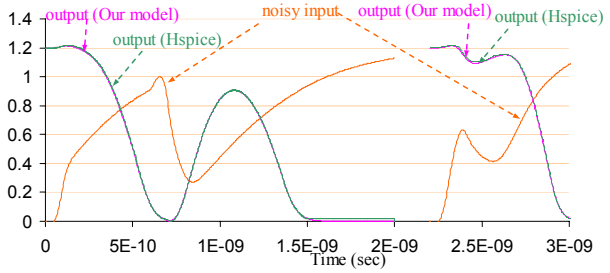


Figure 3. The actual waveforms and the ones computed by CSPC for some crosstalk-induced noisy waveforms.

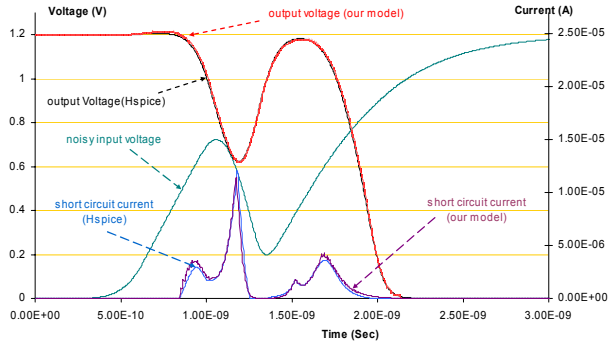
The switching energy consumption per signal transition for the inverter in the aforementioned experiments (Figure 4(a) and (b)) is measured as 8.89fJ. This shows an E_{sc}/E_{sw} ratio (i.e., SC to switching energy ratio per transition) of 30.1%, and 176.0% for the two cases of Figure 4(a) and Figure 4(b), respectively. These examples clearly demonstrate how severely the SC energy dissipation can be increased due to the noisy input signals even for a reasonable logic cell input transition time and output load.

To compare CSPC to conventional techniques, we implemented the technique by Dartu et al. in [11] in which an input signals are approximated by smooth saturated ramp waveforms in order to be compatible with the pre-characterized lookup tables. Figure 4(b) illustrates the SC waveform for one such ramp approximation. The corresponding SC energy dissipation is calculated as 7.1fJ, which is less than half of the actual SC energy dissipation by the noisy waveform (i.e., 45.9% error with respect to the Hspice report, 15.45fJ.) This underlines the fact that the shape of waveform should not be ignored during the SC power calculation.

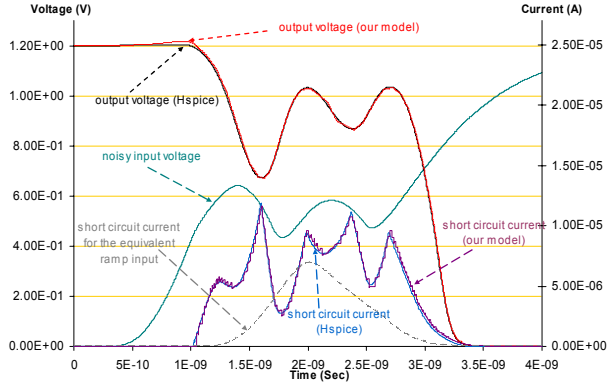
To investigate the accuracy of CSPC in dealing with a complex logic cells, an AOI22 (And-Or-Invert) with size 10*x* was studied, where *x* denotes the minimum size for an AOI22. The cell was FO4-loaded. One of the input nodes was subjected to crosstalk noise through a coupling capacitance of 80fF. The other inputs were set to their non-controlling values. We used the same characterization process as an inverter for complex gates. The corresponding aggressor and victim lines were driven by 10*x* inverters. The arrival time of the signal transition at the input of the victim line driver was set to 10ps while that of the aggressor

[2] For cells realizing more than one logic function (such as an AND cell, which is simply a NAND cell followed by an INV cell), the characterization process should be repeated for each logic function.

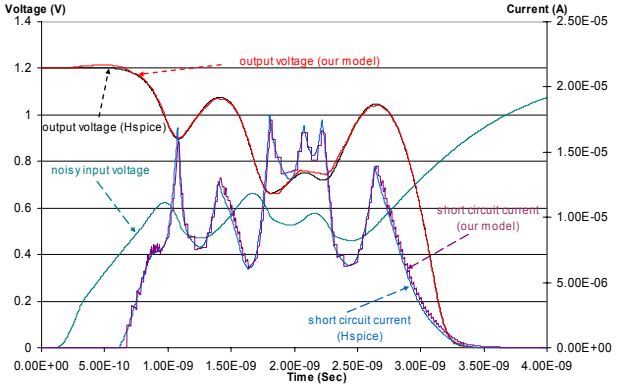
line driver (i.e., the noise injection time) was swept from 100ps to 250ps with a time step of 1ps. Figure 5 depicts the percentage error in SC energy dissipation calculation of the AOI22 compared with Hspice. The average (maximum) error of the SC energy calculation for the AOI22 cell is 1.16% (3.35%.) We repeated this experiment for different FO4-loaded logic cells with different sizes.



(a)



(b)



(c)

Figure 4. Comparison between CSPC vs. Hspice for minimum size inverter in (a) and (b) and minimum size NAND2 in (c), given single (a), double (b), triple aggressor (c) crosstalk-induced noisy waveforms.

An automated test was performed to validate CSPC against Hspice for different logic cell types using a similar experimental setup to that of the previous experiment on the AOI22. 150 noisy input waveforms were applied by sweeping the noise injection time for each logic cell. For each noisy input the transient analysis period and step size were set to 4ns and 3.3ps, respectively. Table 1 summarizes the average and maximum errors in the SC energy calculation of those logic cells. The runtime of CSPC is independent of the number of transistors in the logic cell. In contrast, the transistor count greatly affects the runtime of Hspice. For example, the Hspice simulation for XOR2 takes almost 3 times as long as that of the NAND2 whereas the runtime of CSPC is about the same for both cases.

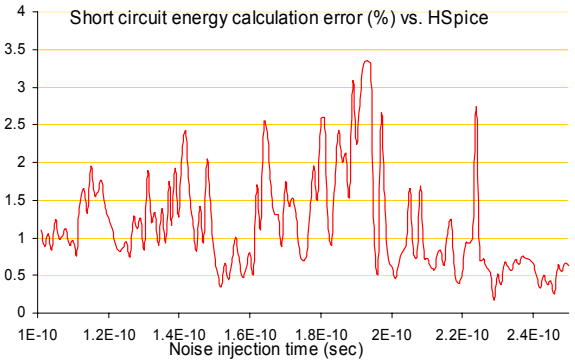


Figure 5. Absolute SC energy calculation error vs. Hspice for an AOI22 size 10x under noisy waveforms

Next we demonstrate the accuracy of CSPC for SC energy dissipation of glitches. Figure 6 shows a glitch induced by a coupling capacitance value of 50fF on the quiet victim, which happens to be the input node of a minimum-size inverter with a FO4 load. The output voltage waveforms constructed by CSPC as well as those computed by Hspice are also depicted. It is seen that the inverter output is not logically affected by the glitch, and therefore, the glitch will be typically ignored by the timing analysis or a validation tool. However, the corresponding SC energy dissipation is measured by Hspice to be 3.5fJ. This amount is in fact comparable with the SC dissipation measured for complete signal transitions at the input of the inverter, e.g., contrast this value to the energy dissipation for the case of Figure 4(a) reported by Hspice as 2.68fJ.

Table 1. Runtime and error comparison between CSPC and Hspice.

Logic Cell	Error (%)		Runtime		Runtime Speedup
	Avg.	Max	CSPC	Hspice	
INV 10x	1.11	2.13	82.8ms	244	2940
NAND2 10x	1.23	3.29	85.6ms	524	6120
XOR2 10x	1.41	3.52	94.4ms	1492s	15800
AOI22 10x	1.16	3.35	90.0ms	608s	6750

An AOI22 with a relative size of 10*x* was considered under a similar experimental setup as the one in Figure 5. However, this time the cell input under crosstalk attack was kept quiet. In addition, the arrival time of the aggressor line was set to a constant value, while its transition time was swept from 200ps to 400ps with a time step of 1ps. Figure 7 is the absolute error for the SC energy calculation of the corresponding 200 glitch cases.

CSPC was coded in C. All the experiments discussed in this section were performed on a Sun Fire V880 machine with the UltraSPARC III 750MHz processor running Sun Solaris operating system.

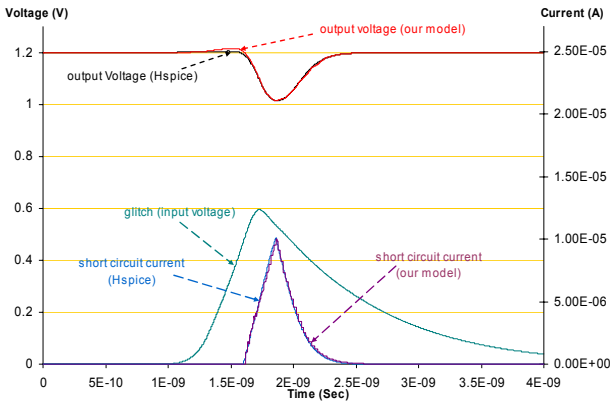


Figure 6. Hspice and CSPC waveforms for the example of a glitch.

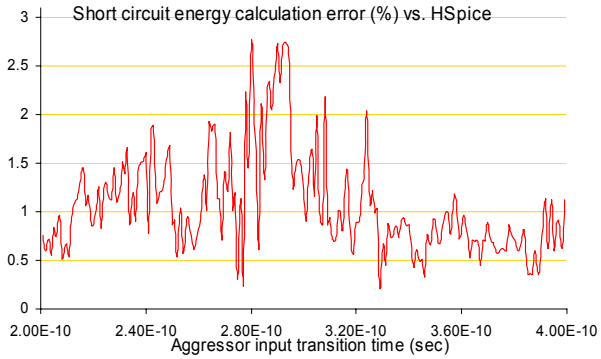


Figure 7. SC energy calculation errors of CSPC vs. Hspice for an AOI22 size 10x under glitches

5. CONCLUSION

An accurate technique to calculate the SC energy dissipation of logic cells was presented. The SC current was shown to be highly dependent on the input and output voltage values and hence the shape of the waveforms. This fact has been generally ignored by the conventional SC estimation techniques. To address this issue, we developed a novel current-based logic cell model that can accurately construct the output voltage waveform for a given input waveform of arbitrary shape subjected to noise. The input and output voltage waveforms are used to calculate the SC current and hence energy dissipation. A pre-characterization process is executed for each cell to model the electrical parameters such as the parasitic capacitances and nonlinear current sources. Our model is capable of considering the glitches in SC energy calculation. The Hpsice-based experimental results show the high accuracy of our technique. Extension of this work will consider the effect of process variations on SC power dissipation.

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