A Current-Feedback Instrumentation Amplifier With 5 μV Offset for Bidirectional High-Side Current-Sensing

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***Abstract*—This paper describes an instrumentation amplifier for bidirectional high-side current-sensing applications. It uses a multipath indirect current-feedback topology. To achieve low offset, the amplifier employs a combination of chopping and auto-zeroing in a low frequency path to cancel the offset of a wide-band amplifier in a high frequency path. With a 60 kHz chopper clock and a 30 kHz auto-zero clock, this offset-stabilization scheme results in an offset voltage of less than 5 μV, a CMRR of 143 dB and a common-mode input voltage range from 1.9 to 30 V. The input voltage-to-current (*V-I*) converters required by the current-feedback topology are implemented with composite transistors, whose transconductance is determined by laser-trimmed resistors. This results in a less than 0.1% gain inaccuracy. The instrumentation amplifier was realized in a 0.8 μm BiCMOS process with high voltage transistors, and has an effective chip area of 2.5 mm^2.**

***Index Terms*—Auto-zero, chopper, CMOS analog integrated circuits, current-sense, instrumentation amplifier.**

I. Introduction

In MANY sensor systems, there is a need to amplify weak differential signals that are often accompanied by strong common-mode (CM) signals. In the high-side current-sense application discussed in this paper, the voltage drop across a current-sensing resistor results in differential signals ranging from 10 μV to 100 mV with a CM voltage ranging from 1.9 to 30 V. Amplifying such weak signals requires an amplifier with an offset below 10 μV and a CMRR in excess of 130 dB, which is quite challenging.

There are three general approaches to implement instrumentation amplifiers that tackle the above-mentioned challenge. The first approach involves the use of operational amplifiers (opamps) with resistive feedback. The three-opamp instrumentation amplifier is probably the most well-known example of this approach [1]. In this topology, two opamps are used to implement a fully differential buffer, which is followed by a single opamp configured as a differential amplifier. The amplifier's CMRR is determined by resistor mismatch, and as a result cannot be very large. The second approach involves the use of switched capacitor techniques to overcome the CM voltage [2], [3]. However, not many monolithic processes have capacitors capable of handling 30 V CM voltages. The third approach involves the use of current-feedback instrumentation amplifiers, in which the use of isolation and balancing techniques has more potential to obtain a high CMRR [4]–[6]. In this paper, chopper offset-stabilization techniques used in opamps [11], [12] will be extended to current-feedback instrumentation amplifiers. Although this paper focuses on a high-side current-sense application, similar techniques can be used to design general-purpose instrumentation amplifiers with high CMRR and low offset.

In Section II, the current-sensing application will be described. In Section III, the concept of direct and indirect current-feedback instrumentation amplifiers will be discussed. In Section IV, the design of a current-feedback instrumentation amplifier will be discussed, with emphasis on the various dynamic offset compensation techniques used to achieve low offset. Section V describes the transistor-level design of the amplifier's input stages in more detail, since these stages determine the amplifier's gain accuracy. The measurement results are presented in Section VI.

II. Current-Sensing

Sensing supply currents is a fundamental requirement in many electronic systems, and the applicable techniques are as diverse as the applications themselves. Typical applications include: over-current protection, programmable current sources and current integration, or so-called Coulomb counting circuits used to monitor the charge level of a battery.

In battery supply-current sensing, the current is typically determined by measuring the small voltage drop across a current-sense resistor in series with the battery and the load as shown in Fig. 1. The sense-resistor can either be implemented between the negative power supply and the load, a technique called low-side current-sensing, or between the positive power supply and the load, called high-side current-sensing. A so-called current-sense amplifier is then used to amplify the small voltage drop across the sense resistor. In low-side current-sensing, the CM voltage is low and a regular instrumentation amplifier can be used to amplify the voltage across the sense resistor.

Both high-side and low-side current sensing are used in commercial applications. On the one hand, low-side current sensing has the disadvantage that the load is not directly connected to ground, which may be a problem in systems where the current through multiple loads must be sensed, or where, for practical or safety-related reasons, all such loads must be connected to a

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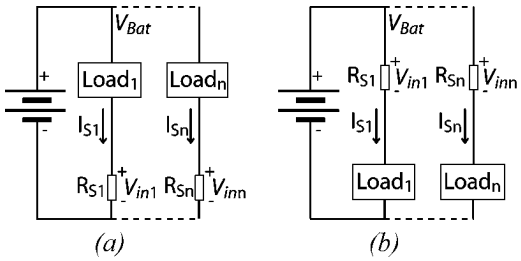

Fig. 1. Current-sensing principle: (a) low-side; (b) high-side.

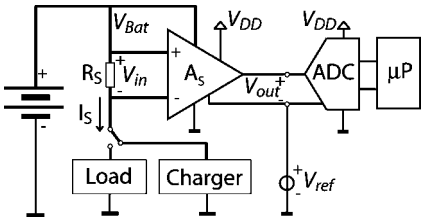

Fig. 2. Bidirectional high-side current-sense system.

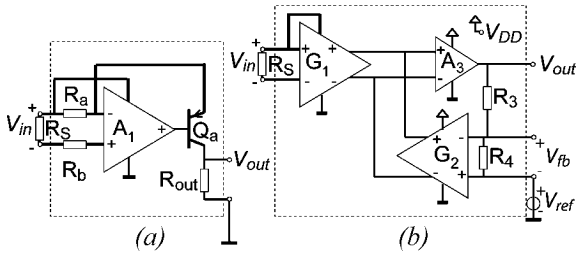

Fig. 3. A high-side current-sense amplifier based on (a) a current follower; (b) an indirect current-feedback instrumentation amplifier.

common ground. On the other hand, a high-side current-sense amplifier must be able to suppress a large input CM voltage, while also generating a ground-referred output voltage.

Focusing on the specific application of monitoring load currents in laptops, a few specifications can be derived. Nowadays, laptop battery voltages range up to 15 V and are expected to increase in the future. Considering that during charging a higher voltage is applied to the battery, it is reasonable to design for a 30 V maximum input CM voltage. Furthermore, the current through a laptop battery can range from a standby current of about 10 mA to peak currents of up to 10 A. To minimize the sense-resistor's value, and reduce its power dissipation, to preferably less than the power loss in the supply chain, two specifications for high-side current-sense amplifiers are critical: input offset voltage and CMRR. For instance, if a sense resistor of 1 mΩ [18] is used, the input voltage V_{in} can range from 10 μV to 10 mV. Therefore, the input offset should be less than 10 μV and the CMRR should be higher than 130 dB.

The circuit shown in Fig. 2 can be used to monitor the charge level of a battery. The current-sense amplifier A_S monitors the battery current via sense resistor R_s. The output voltage V_{out} is greater than V_{ref} for load currents, and less than V_{ref} for charging currents. The ADC digitizes the output of the current-sense amplifier A_S, and a microprocessor then integrates the result to determine the remaining charge in the battery. This application requires the current-sense amplifier to have a gain error of less than 0.5%.

Many topologies can be used for implementing a current-sense amplifier; amplifiers with resistive feedback, switched-capacitor amplifiers, current followers, or true instrumentation amplifiers. Examples of the last two are shown in Fig. 3. In Fig. 3(a), a current follower topology is shown [10]. Here, the opamp A_1 forces the sense voltage V_{in} over the input resistor R_a. The current through this resistor equals the output current. For a positive V_{in}, the gain of the current-sense amplifier can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{R_{out}}{R_a}. \tag{1}$$

This topology is unipolar, i.e., it only works for a positive V_{in}. Transistor Q_a separates the high input voltage from the low output voltage. The input CM voltage should always be higher than the output voltage, for proper biasing of transistor Q_a. To realize a low-offset current-sense amplifier, the opamp A_1 can be designed for low offset [10].

A current-sense topology based on a current-feedback instrumentation amplifier is shown in Fig. 3(b). This topology isolates the input and output CM voltages. This implies that the input CM voltage can be lower than the output CM voltage. The input transconductance G_1 amplifies the input voltage V_{in}, while a feedback transconductance G_2 amplifies the feedback-voltage V_{fb} across resistor divider R_3 and R_4. The difference in their output currents drives an opamp A_3. If this has sufficiently high gain, the output currents of G_1 and G_2 will effectively cancel each other. The opamp A_3 will then adjust the output voltage in such a way that

$$\frac{V_{out} - V_{ref}}{V_{in}} = \frac{R_3 + R_4}{R_4}\frac{G_1}{G_2}. \tag{2}$$

Unlike the current follower, the current-feedback topology can handle bidirectional currents. But its offset is the sum of the offsets of both G_1 and G_2.

III. Current-Feedback Instrumentation Amplifiers

A distinction can be made between direct current-feedback (DCF) and indirect current-feedback (ICF) instrumentation amplifiers [6]. In Fig. 4, both topologies are sketched. In both of them, transistors M_1, M_2 and resistor R_1 form a *V–I* converter with a transconductance of $1/R_1$. Another *V–I* converter consisting of M_3, M_4 and R_2, with a transconductance of $1/R_2$, provides feedback from the output.

The gain of both the instrumentation amplifier is then given by (2), where G_1 is the transconductor composed of M_1, M_2, and R_1, and G_2 is the transconductor composed of M_3, M_4, and R_2. In the DCF approach [Fig. 4(a)], transistors M_1 and M_2 are always biased at the same drain current I, while transistors M_3 and M_4 carry a signal dependent drain current. This difference in bias currents can be a source of nonlinearity. Furthermore, cascading the two *V–I* converters decreases the input CM voltage range. In the ICF approach [Fig. 4(b)], transistors M_1 and M_2 *and* transistors M_3 and M_4 carry a signal-dependent drain current, eliminating this source of nonlinearity, while

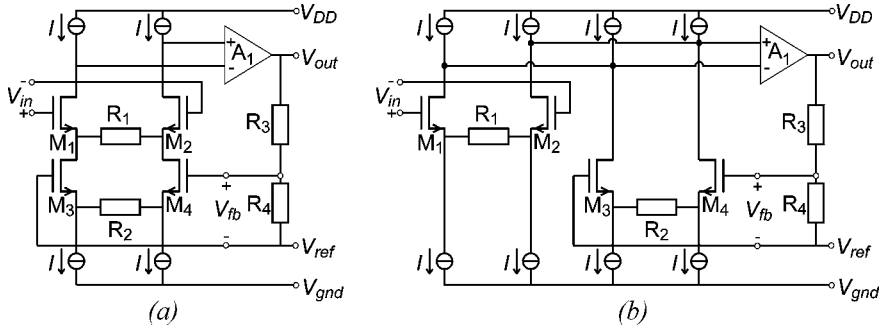

Fig. 4. (a) Direct current-feedback instrumentation amplifier. (b) Indirect current-feedback instrumentation amplifier.

the minimum supply voltage and input voltage range are also relaxed. In the ICF approach, the input common-mode voltage and reference common-mode voltage are independent of each other. This, however, comes at the price of an increased current dissipation. Therefore, the DCF approach is often used in biomedical low-power applications [7], [8]. This work focuses on gain accuracy and linearity, and therefore, the ICF approach is adopted.

The next part of this paper presents a low-offset indirect current-feedback instrumentation amplifier for high-side current-sensing applications. A combination of chopper and auto-zero offset stabilization techniques [11] is used to achieve an offset voltage of less than 5 μV over a CM input voltage range of 28 V, and a DC CMRR of more than 140 dB. The supply voltage V_{DD} can range from 2.8 to 5.5 V, while the input CM voltage V_{Bat} can independently range from 2 to 30 V. The use of separate supply voltages simplifies the task of interfacing the current-sense amplifier to other systems, e.g., an ADC. Furthermore, the amplifier's output can be referred to an external reference voltage V_{ref}, which can range from 0 to $V_{DD}-1.4$ V. Trimmed gain-setting resistors are used to achieve 0.1% gain accuracy with a fixed V_{ref}.

IV. System Topology

Because a normal chopper amplifier has a limited bandwidth, a multipath topology is used to implement this amplifier. A high frequency path determines the amplifier's gain bandwidth product, while a low frequency path determines the amplifier's DC and low-frequency characteristics such as offset and low frequency noise. Therefore, the low frequency path is designed for low offset. A simplified block diagram of the amplifier is shown in Fig. 5. The high frequency path consists of transconductor G_3 and feedback transconductor G_4. Their differential output current drives a two stage class AB operational amplifier implemented by stages G_2 and G_1. The low frequency path consists of a chopped input transconductor G_7 and a chopped feedback transconductor G_8, an integrator built around G_6, another transconductance G_5 and the two stage opamp (G_2 and G_1).

Choppers $\mathrm{CH}_{1,2,3}$ modulate the offset voltages of G_7 and G_8, so their offset is negligible. The difference between the output currents of G_7 and G_8 drives the integrator, which in turn drives a transconductance G_5. If the transconductances of G_7 and G_8 are equal, the integrator's output will converge to a voltage that ensures that V_{in} and V_{fb} are equal, i.e., the integrator loop compensates for the input offset of the high-frequency path. The integrator's output voltage drives transconductor G_5, which compensates the offset voltage of G_3 and G_4 by supplying a current

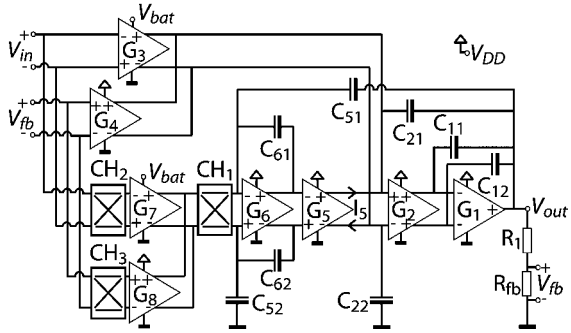

Fig. 5. Chopper offset stabilized indirect current-feedback instrumentation amplifier.

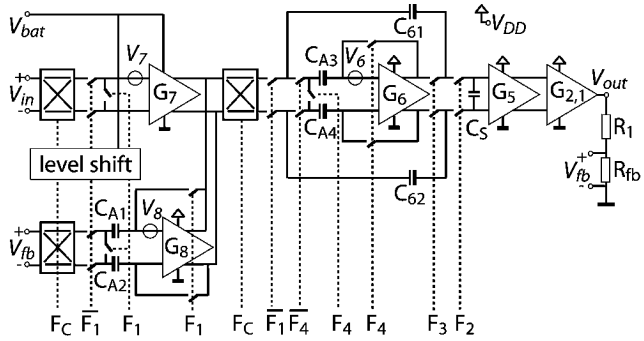

Fig. 6. Low-frequency path showing all chopping and auto-zero techniques used.

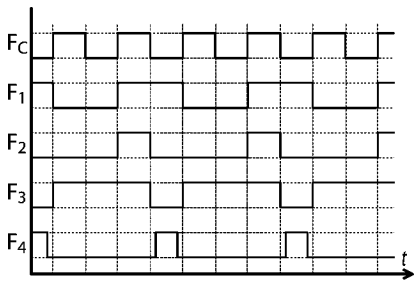

Fig. 7. Timing diagram.

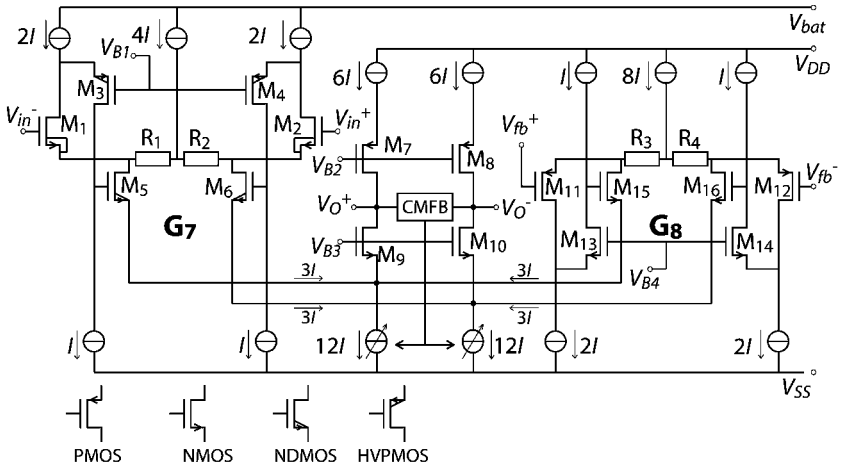

Fig. 8. Simplified schematics of the input stages.

I_5. In order to implement the high-side current sense amplifier, G_3 and G_7 are biased via the high-side CM input voltage V_{Bat}, while the other stages are biased via the supply voltage V_{DD}. This technique operates in the same way as chopper offset stabilization in an operational amplifier [11], [12].

Capacitors C_{11}, C_{12}, C_{21} and balancing capacitor C_{22} form a nested-Miller compensation network designed to obtain a GBW of 1 MHz with a load capacitance C_L of 100 pF. Capacitors C_{61} and C_{62} are used as integration capacitors. Capacitors C_{51} and balancing capacitor C_{52} are used to implement a multipath hybrid-nested-Miller frequency compensation scheme [14]–[16] with a smooth 20-dB/decade roll-off. Without capacitors C_{51} and C_{52} the amplifier would only be conditionally stable.

Input transconductors G_7 and G_8 determine the amplifier's low-frequency characteristics, such as its offset, $1/f$ noise, DC CMRR, and DC gain error. The offset and low-frequency noise is chopper modulated by chopper CH_1, while the input and feedback signals are chopper modulated and demodulated by choppers CH_2, CH_3, and CH_1, respectively. This results in a significant reduction of the offset and low-frequency noise introduced by G_7 and G_8. Transconductors G_3 and G_4 determine the amplifier's high frequency characteristics, such as its unity gain frequency. The output currents of G_7 and G_8 will cancel due to the feedback, and when $G_7 = G_8$ the DC gain will be

$$\frac{V_{out} - V_{ref}}{V_{in}} = \frac{R_1 + R_{fb}}{R_{fb}} \frac{G_7}{G_8} \approx \frac{R_1 + R_{fb}}{R_{fb}}. \tag{3}$$

The modulated offset voltage of G_7 and G_8 gives rise to ripple, which is filtered by the integrator. This results in a triangular ripple at the output of G_6, which in turn, gives rise to a triangular wave at the output of the whole amplifier. The input referred peak-to-peak voltage of this triangular wave is given by

$$V_{in-pp} = (V_7 + V_8) \frac{G_{7,8} G_5}{2 F_C C_6 G_{3,4}} \tag{4}$$

where V_7 and V_8 are the input referred offset voltages of G_7 and G_8, respectively, C_6 is the value of the integrating capacitors C_{61} and C_{62}, and F_C is the chopper frequency. In this design $G_{3,4} = G_{7,8} = 100\ \mu$A/V, $G_5 = 5\ \mu$A/V, $C_6 = 32$ pF, and $F_C = 60$ kHz, which together with a worst case offset $V_7 = V_8 = 10$ mV leads to a 26 mV input referred peak-to-peak triangular ripple voltage. To further reduce this ripple, a combination of auto-zeroing and chopping is used as shown in Fig. 6, where the implemented low frequency path is shown in more detail. Controlled by the clock F_1, the offsets of G_7 and G_8 are auto-zeroed by short-circuiting both their inputs, connecting G_8 in a unity-gain configuration and then storing the sum of their offset voltages on capacitors C_{A1} and C_{A2}. As stated earlier, G_7 and G_8 are chopped by clock F_C, which modulates both the residual offset of the auto-zero action and the undersampled noise associated with auto-zeroing away from DC. The timing diagram of

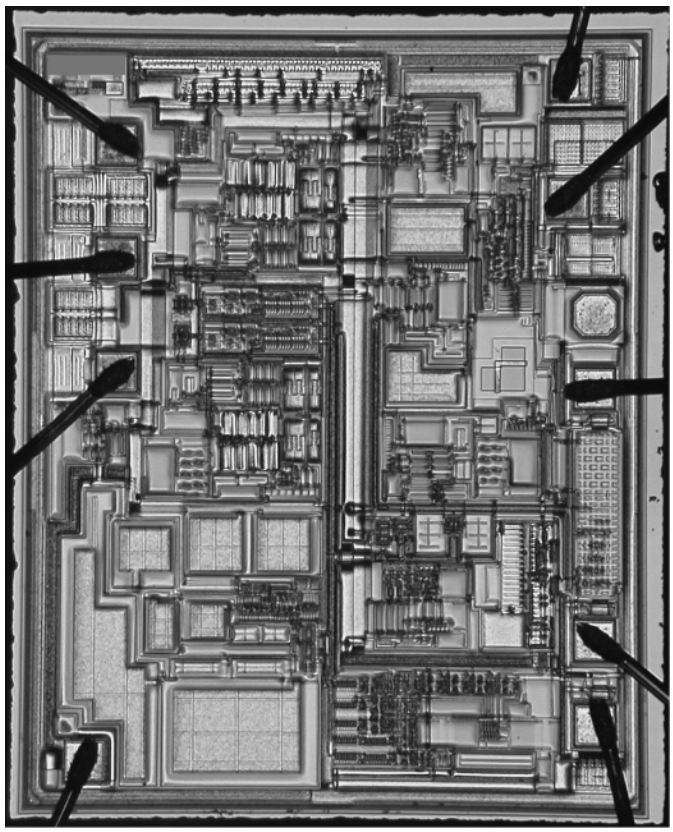

Fig. 9. Chip micrograph.

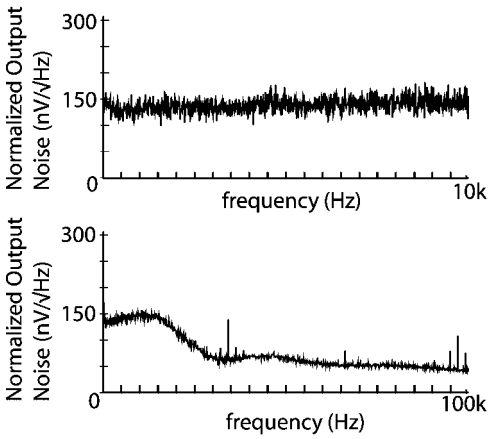

Fig. 10. Output noise spectra divided by the gain; $gain = 11$.

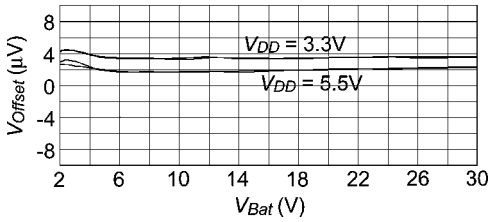

Fig. 11. Input referred offset voltage.

the system is shown in Fig. 7. All switches between V_{in} and G_7 are implemented with PMOS switches in a high-voltage epi-pocket. A level-shift circuit drives the high-side chopper switches. All other switches are implemented with NMOS transistors.

The combination of auto-zeroing, chopping and the use of a multipath topology is quite powerful. Auto-zeroing reduces the offset, which leads to a reduced ripple due to chopping. On the other hand, chopping modulates the folded noise associated with auto-zeroing to higher frequencies. At these frequencies the high frequency path dominates the noise characteristics. However, since the transconductances G_7 and G_8 only see the input and feedback voltages half of the time, the signal to noise ratio of the low frequency path is decreased by at least a factor $\sqrt{2}$.

The offset V_6 of the integrator together with the parasitic output capacitance $C_{par7,8}$ seen between the outputs of G_7 and G_8 and chopper CH_1 will also cause a residual equivalent input offset [11]. This is because the offset appears as a chopped voltage that charges and discharges the parasitic output capacitance of G_7 and G_8. The required current is provided by G_7 and G_8, which means that a voltage must be present at their inputs, and hence that there will be a residual offset at the input of the amplifier. The residual offset caused by this effect can be expressed as

$$V_{off,res} = \frac{4V_6F_CC_{par7,8}}{G_{7,8}}. \tag{5}$$

In this design, a 10 mV worst-case offset V_6 would lead to a 24 μV residual offset, when $C_{par7,8} = 1$ pF. To avoid this, the integrator is also auto-zeroed. During the auto-zeroing of G_7 and G_8, the integrator's output voltage is sampled on C_S by clock F_2. This sampling operation also reduces the triangular ripple caused by chopping. Next, the integrating capacitors C_{61} and C_{62} are disconnected from the output of G_6 by clock F_3, after which G_6 is configured in unity-gain and its offset V_6 stored on capacitors C_{A3} and C_{A4} by clock F_4. To avoid momentarily short-circuiting the integration capacitors, F_3 and F_4 are implemented as nonoverlapping clocks.

Referring to Fig. 5, the balancing capacitors C_{22} and C_{52} are actually needed to cancel zero's in the amplifier's open loop gain, which can be found around the bandwidth of the common-mode feedback control circuits. The resulting pole-zero doublets will not effect the settling of the amplifier, provided that the bandwidth of the common-mode control circuits is sufficient. The settling behavior of this amplifier is dominated by the combination of auto-zero and chopping offset stabilization of the low-frequency path. With a 20 mV input step and a gain of 100, the measured large signal 1% settling time is 160 μs.

V. Input Stages

To sense the positive rail, the high-side input stages G_3 and G_7 need to be designed with high-voltage capable NMOS input transistors. By contrast, the ground-sensing input stages G_4 and G_8 need to be designed with PMOS input transistors. Since these stages use different types of transistors and are operated at different CM voltages, their transconductances will be inherently mismatched. To solve this problem, composite transistors are used, whose transconductances are set by resistors [5], [17]. A simplified schematic of G_7 and G_8 is shown in Fig. 8.

The high-voltage input transconductors G_3 and G_7 are designed as follows. The input NMOS transistors M_1 and M_2 are always biased at the same drain current. They act as voltage followers with a constant gate-source voltage and force the differential input voltage across resistors R_1 and R_2. Although M_1 and M_2 operate at a high input CM voltage, to improve matching they have been implemented by low voltage transistors. In the high-side current-sense amplifier application the battery voltage V_{bat} is shorted to one of the inputs, therefore the drain-source voltage is limited by their gate-source voltage. Furthermore, using a twin-well process the backgate Pwell can be biased at a high voltage. The drains of M_1 and M_2 are connected to high-voltage PMOS folded-cascodes M_3 and M_4, that drive high-voltage NMOS transistors M_5 and M_6 functioning as inverting amplifiers and as current-followers.

The high gain of this local loop ensures that the transconductance of G_7 is accurately defined by the values of R_1 and R_2. With the biasing currents shown in Fig. 8, the amplifier's gain variation is less than 0.1% over the entire CM voltage range. The high-voltage devices M_3 to M_6 can handle CM voltages as high as 30 V, which is the limit imposed by the process used. With transistors M_1 to M_4 biased at a current $I = 2.5$ μA, the maximum input differential voltage range is $V_{dmax} = 6IR$, where $R = R_1 = R_2 = 10$ kΩ. In this design V_{dmax} corresponds to 150 mV. A similar topology is used for G_4 and G_8, using PMOS input transistors, NMOS cascodes and NMOS current followers. The resistors in G_7 and G_8 are laser-trimmed for an accurately defined transconductance.

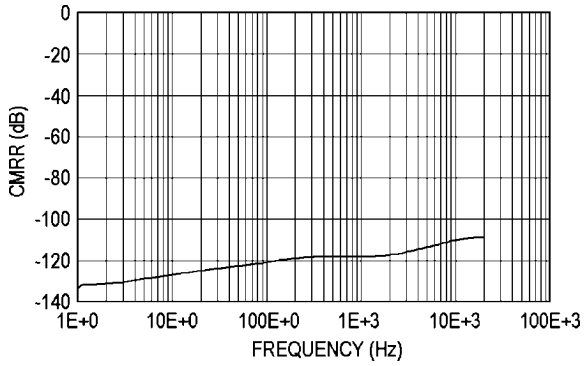

Fig. 12. CMRR as a function of frequency.

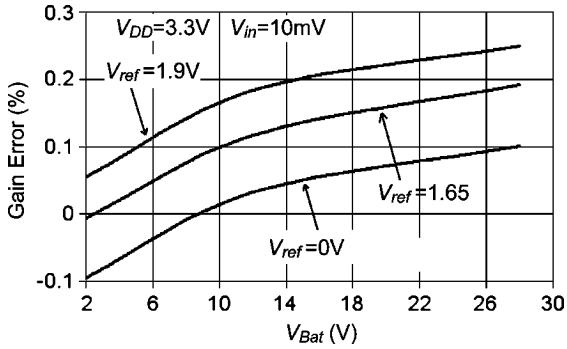

Fig. 13. Gain error.

The output currents of both the input stages are summed in a folded-cascode stage consisting of transistors M_7 to M_{10}. A common-mode feedback loop was also implemented to control the voltage at the output of the combined fully differential amplifier. The input stages G_7, G_8, G_3 and G_4 were each designed for a noise level of 50 nV/$\sqrt{}$Hz, and because the two input stages work in parallel, the their total noise is a factor $\sqrt{2}$ higher. The 50 nV/$\sqrt{}$Hz is considerably larger than the noise contribution of the degeneration resistors R_1 and R_2, which set a lower limit of 18 nV/$\sqrt{}$Hz. The current noise of all the current sources shown in Fig. 8 is the main source of this increased noise level.

VI. Measurement Results

The current-sense amplifier was fabricated in a 0.8 μm BICMOS process with high voltage transistors and laser-trimmed thin-film resistors. It has a die area of 2.5 mm^2. The chip micrograph is shown in Fig. 9. The output noise spectral density for a gain of 11 is shown in Fig. 10. At frequencies below 10 kHz, the input noise density is around 136 nV/$\sqrt{}$Hz. At frequencies above 15 kHz the noise level drops almost linearly towards 70 nV/$\sqrt{}$Hz, which is the noise level of the high frequency path. This means that the low frequency path has almost twice the noise level of the high frequency path. A factor $\sqrt{2}$ was expected due to the time-multiplexed operation of the low-frequency path, as it turns out, however, the low-frequency noise is 30% higher than expected. At frequencies between DC and 15 kHz, a slight increase in the noise level can be seen, which is due to the combination of auto-zeroing and chopping [11], [12], [14].

Measurements on 10 samples show that the amplifier's offset voltage is less than 5 μV. In Fig. 12, the offset performance of two samples is shown versus the input CM voltage V_{bat}. It can be seen that the offset stays within 2 μV over a 28 V change in V_{Bat}, which corresponds to a 143 dB DC CMRR. It can also be seen that the offset changes about 2 μV for a 2.2 V change in V_{DD}, which corresponds to a 121 dB DC PSRR. The CMRR as a function of frequency is shown in Fig. 12.

For a current-sense amplifier, offset is not the only important specification. The amplifier's gain accuracy should also be sufficiently high over the input CM range and reference CM range. Due to the finite gain of the input transistors used in G_7 and G_8, their gate-source voltage may change as the input CM voltage changes, causing gain errors. In Fig. 13 the gain error is shown as a function of the input CM voltage V_{Bat} at three reference voltages levels. It can be seen that this amplifier achieves 0.1% gain accuracy for a fixed V_{ref}, and 0.2% gain accuracy over the full V_{ref} range.

TABLE I
Comparison of Low-Offset Current-Sense Amplifiers

		LTC6102 [10]	This work
Year of release/publication		2007	2008
Offset		10µV	5µV
Bidirectional		No	Yes
Gain Accuracy		External resistor dependent	0.1%
I_{supply} shutdown		No	1µA
V_{DD}		V_{Bat}	2.8 to 5.5V
V_{Bat}		4 to 60V	1.9 to 30V
V_{out}		0 to 8V	0 to V_{DD}
I_{supply}	V_{Bat}	420µA	200µA
	V_{DD}	-	650µA

VII. Conclusion

An indirect current-feedback instrumentation amplifier for high-side current-sensing applications has been designed. Its supply voltage V_{DD} can range from 2.8 to 5.5 V, while its input CM voltage V_{Bat} can independently range from 2 to 30 V. The use of separate supply voltages simplifies the task of interfacing the current-sense amplifier to other systems, e.g., an ADC. Furthermore, the amplifier output voltage can be referred to an external reference voltage V_{ref}, which can range from 0 to $V_{DD}-1.4$ V. Chopping and auto-zeroing techniques have been used to achieve an offset voltage of less than 5 μV at room temperature over a CM input voltage range from 1.9 to 30 V, achieving a more than 143 dB DC CMRR. Furthermore, trimmed gain-setting resistors are used to achieve 0.1% gain accuracy for a fixed V_{ref}. In Table I, this work is compared to a commercially available precision current-sense amplifier [10]. Although both these amplifiers represent a new level of precision in current-sensing, the topology presented here has the natural bidirectional current-sensing capability of an instrumentation amplifier, and allows the use of independent CM input and output voltages.

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