

A Current-mode, 3V, 20MHz, 9-bit equivalent CMOS Sample-and-Hold Circuit

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Abstract— A new current-mode, low-power, low-voltage and high-speed CMOS sample-and-hold circuit has been designed and fabricated. A new current-mode differential switching scheme has been adopted to eliminate errors caused by feedthrough injection from the sample switches. The experimental result yields 9-bit resolution in 9mW power dissipation, in a 20MHz clock frequency from a 3V power supply.

I. INTRODUCTION

The pipeline architecture is commonly utilized in video-speed A/D converters. The use of current-mode and switched-current circuits has been studied to achieve low voltage and low power operation of the A/D converter. However, high speed operation using this approach has not been achieved [1]. We propose placing high-speed, high precision current-mode sample-and-hold circuit in front of the low resolution current-mode A/D converter to form a bit-block in a pipeline A/D converter. With this configuration, the operational frequency of a pipeline A/D converter becomes equal to the maximum operating frequency of each bit-block [2].

Aiming at the use as the front-end circuit for a bit-block in a pipeline A/D converter, we have designed and fabricated the CMOS current-mode sample-and-hold circuit. This paper describes the design and the evaluation result.

II. FEEDTHROUGH CANCELLATION

The basics of a current-mode sample-and-hold circuit are seen in Fig. 1. In order to cancel the feedthrough from the switch and obtain accurate output current equal to the input current, we developed a differential switching scheme. The circuit shown in Fig. 1 is composed of an I-V converter, two switches, and a differential amplifier. When input current I_{in} is applied to the diode connected transistor M5, a current change of $+I_{in}/2$ and $-I_{in}/2$ occurs in M5 and M7. This results in a small voltage change

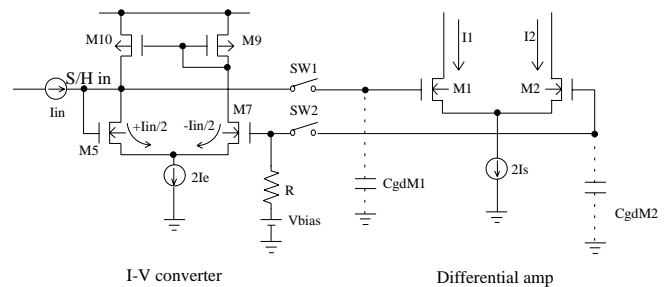


Fig.1. Differential sampling scheme

between the gates of M1 and M2 when switches SW1 and SW2 are both on. The differential amplifier amplifies this and produces output

currents I_1 and I_2 . Since transistors M5 and M7, and M1 and M2 simply form a current mirror in the differential configuration, I_{in} is accurately transferred to the output when the current difference of $I_1 - I_2$ is taken (provided that I_c is equal to I_s). The feedthrough from switches appears equally at the gate terminals of M1 and M2 when they become turned off. The feedthrough is suppressed by the common mode rejection characteristic of the differential amplifier. We can choose the DC bias point for the switches to be half of the VDD in this configuration, which reduces their on-resistance to as low as possible.

III. CIRCUIT DESIGN AND SIMULATION RESULT

The actual circuit implementation of the sample-and-hold circuit is shown in Fig. 2. A cascode connection of transistors is used throughout the circuit to increase the output impedance of the device. A 0.3pF of capacitor is connected to each gate of M1 and M2 to improve the linearity of the output waveform. The output circuit, which is composed of transistors M13 to M18, produces the current difference of M1 and M2, and outputs it in the current form.

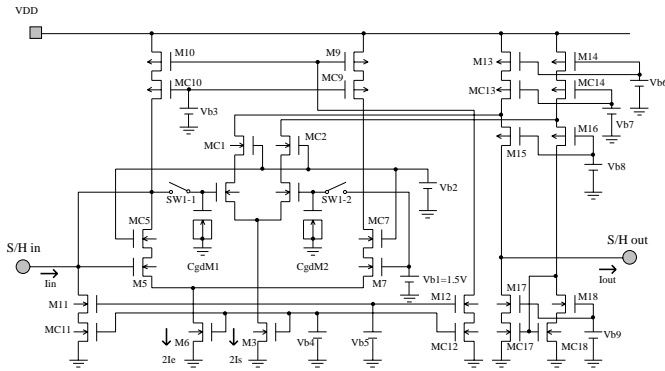


Fig.2. Designed sample-and-hold circuit

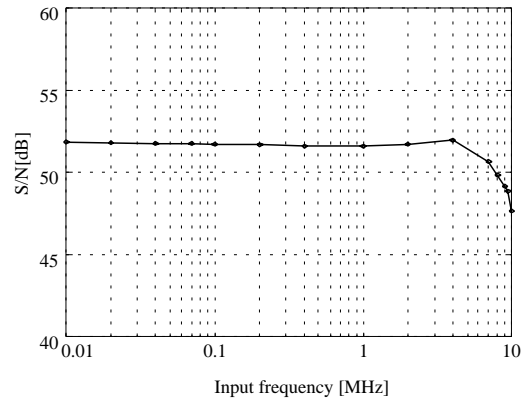


Fig.4. Input frequency v.s. S/N characteristic

The high-speed and high-performance capabilities of the designed sample-and-hold circuit were examined by a SPICE circuit simulation. The device parameters used were consistent with the MOS 0.6 μ m design rule. The threshold voltages (V_{th}) were 0.85V for NMOS and -0.85V for PMOS. Input signal frequency was 1MHz and input signal current was $\pm 20 \mu$ A. The supply voltage was 3V, and the clock frequency was 20MHz. The 0.01 % of the linearity has been observed. It clearly demonstrates that the realization of a current-mode sample-and-hold circuit for the intended purpose is possible.

IV. EXPERIMENTAL RESULT

The designed circuit was fabricated by using a 0.6 μ m CMOS process. Figure 3 shows the input and output waveforms. The output current is converted to the voltage using an external operational amplifier. The supply voltage is 3V, the input frequency is 2MHz in full-scale level and the clock frequency is 20MHz. Figure 4 shows the input frequency versus signal-to-noise (S/N) ratio characteristic, which is again observed with full-scale input, 3V supply and 20MHz clock. In all the case of the chip evaluation, however, the full-scale value of the input current is increased to $\pm 100 \mu$ A because the base-line noise level was more than we estimated. This problem should be further studied. The S/N ratio is 52dB relative to the full-scale in a 10MHz bandwidth for the input frequency range from DC to 5MHz. Even when the input frequency becomes 10MHz, 48dB of S/N is realized. The 9-bit A/D conversion system can be possibly constructed by using this sample-and-hold circuit. Figure 5 is the die photograph of the sample-and-hold chip. The size of the core circuit is $0.3 \times 0.5 \text{mm}^2$.

V. CONCLUSION

A current-mode CMOS sample-and-hold circuit has been designed, circuit simulated, fabricated, and its characteristics evaluated. A 3V, 20MHz with a 9-bit equiv-

alent S/N operation has been verified. The power dissipation for the core circuit in Fig. 2 was 3mW; that of total chip was 9mW. The S/N issue was left for further study. We conclude that this sample-and-hold circuit is applicable to a high precision MOS pipeline video-speed A/D converter.

REFERENCES

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- [2] Y. Sugimoto, S. Tokito, H. Kakitani and E. Seta, "A Current-Mode Bit-Block Circuit Applicable to Low-Voltage, Low-Power Pipeline Video-Speed A/D Converters" *IEICE Trans.Fundamentals*, Vol.E79-A, no.2, Feb. 1996.

photograph

Fig.3. Input and output waveforms (Upper:output,Lower:input)

photograph

Fig.5. Die photograph of the sample-and-hold IC