Research Article

A current mode instrumentation amplifier with high common-mode rejection ratio designed using a novel fully differential second-generation current conveyor

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Abstract
This study presents a high common-mode rejection ratio (CMRR), and high power-supply rejection ratio (PSRR) current-mode instrumentation amplifier (CMIA) to overcome the limitations of existing differential voltage second-generation current conveyors (DVCCII)-based CMIAs in achieving high CMRR. The design is based on a fully differential second-generation current conveyor block with a novel circuit design following by a current subtracting stage. The CMIA is designed and laid out in 130 nm CMOS technology operating under ± 1.2 V supply voltage in Cadence software. The post-layout simulation results show that the CMIA achieves low-frequency voltage and current CMRR- BW of 228.8 dB–10 kHz and 246 dB–10.6 kHz, respectively, with PSRR + /PSRR- of 108.2 dB/99.7 dB, power consumption of 507 µW, and a core area of 0.0015 mm^2. The unique quality of the circuit is that, it does not need well-matched active blocks, but inherently improves CMRR, bandwidth, and PSRR; hence it gains an excellent choice for integration.

Article highlights

- Highly accurate amplifier is designed to detect very weak signals of information (such as biomedical signals), and amplify them for further processing.
- This circuit has two different input terminals to accommodate both voltage and current signals.
- The final circuit is very small and consumes low power. Thus, it is a good choice for seamless integration to develop portable systems.

Keywords Current-Mode Instrumentation Amplifier (CMIA) · Fully Differential Second-Generation Current Conveyor (FDCCII) · High CMRR Amplifire · High PSRR Amplifire · Low Power-Low Voltage Amplifier · 130 nm CMOS technology

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1 Introduction

In the last decades, due to the increasing demand for portable and battery powered equipment and advances in technology downscaling trend, researchers and designers of analog processors have been encountered with some major challenges in the design of low-power low-voltage (LPLV) circuits and systems [1–3]. Current-mode (CM) signal processing was envisioned as a promising solution to design small and fast LPLV circuits and thus gained more popularity [3–7]. The major advantages of CM processors over the voltage-mode (VM) processors include wide dynamic range and bandwidth (BW), simple circuitry, high speed, low supply voltage and power consumption [4–6]. The incorporation of a high-CMRR instrumentation amplifier (IA) is crucial in many analog/mixed-mode systems such as data acquisition, biomedical circuits and control systems in order to suppress the unwanted common-mode signals along with the desired signals of information [1–5]. Several different voltage-mode instrumentation amplifiers (VMIA) have been reported so far, but they seriously suffer from gain-BW trade-off, and need for precisely matched resistors to achieve high CMRR [8–10]. As a result, the conventional VMIAs have been gradually replaced by current-mode instrumentation amplifiers (CMIA) [11–13].

The CMIA structures can be divided into two main configurations based on input signals as: the low input impedance CMIAs compatible with current input signals [14–16] and the high input impedance ones compatible with voltage input signals [8, 9]. The low input impedance CMIAs utilize the advantages of CM signal processing and have attracted great interests especially after the introduction of CM alternative of Wheatstone bridge (Azka cell) [17]. However, most of the reported CMIAs are of the high input impedance ones [8, 9] whose structures are classified into second-generation current conveyors (CCII)-based CMIAs [15, 19] and current sensing-based CMIAs [8, 20].

CCIIs are active blocks that have been used in designing different analog circuits and systems such as amplifiers [18–20], oscillators [21], analog switches [22, 23], and active filters [24, 25] to grant the benefits of CM circuit design. Although CMRR performance of CCII-based CMIAs is not limited by matching resistors to improve CMRR, they need well-matched active block pairs to achieve higher CMRR. For example, two topologies of CCII-based CMIAs by Wilson [15] and Kaulberg [26] which are suitable for floating loads and both floating and grounded loads, respectively, are reported. Based on experimental results in [15] and [26], CMRR performance of the CMIAs was controlled entirely by the quality and matching of CCII blocks; also, high differential gain and BW was achieved simultaneously while by varying the resistive load, CMRR was almost unchanged. To avoid this matching constraint, differential voltage second-generation current conveyors (DVCCII)-based CMIAs were introduced [10, 20]. Although DVCCII-based CMIAs contain only one active block, they are compatible with only voltage input signals. Among all of the reported CMIAs, those based on fully differential second-generation current conveyors (FDCCIIs) [13, 14] have been of great interest since they employ only one active block and thus no critical component matching conditions are required. Moreover, FDCCII-based CMIAs are compatible with differential input terminals that can be adapted to both voltage and current input signals and differential output terminals.

This paper proposes a FDCCII-based CMIA benefiting from the following features: a) the circuit is designed based on CM circuit techniques and benefits from all advantages of CM signal processing. b) The CMIA has been designed based on only one block of FDCCII with novel circuit design; thus, there is no need for well-matched active blocks to achieve high CMRR. c) Despite the conventional VMIA, in the designed CMIA for a good range of output resistive load there is almost no dependency between gain and BW meaning that the differential gain can increase while the BW remains unchanged. d) Also, the designed CMIA contains one low-impedance differential input in addition to another high-impedance one to process and amplify both current and voltage input signals, respectively. e) Finally, a current subtracting stage has been added to the main block to further improve CMRR and realize a high CMRR CMIA. The rest of the paper is organized as follows: in section II an overview of the FDCCII building blocks is provided. Transistor-level implementation of the CMIA and a detailed design description are presented in section III. Post-layout simulation results along with Process, Voltage, and Temperature (PVT) effect on the performance of the proposed FDCCII and the CMIA, implemented in TSMC 130-nm CMOS technology, are presented in section IV. Finally, section V concludes this work.

2 Fully differential second-generation current conveyors blocK

Functional block diagram with the directions of current and voltage along with the operational matrix of a typical FDCCII are shown in Fig. 1 and Eq. (1), respectively [5]. FDCCII is a current-mode active building block consists of two consecutively connected voltage and current buffers with six terminals, conventionally denoted as Y_+, Y_-, X_+, X_-, Z_+, and Z_-, as illustrated in Fig. 1. Ideally, there is a unity differential voltage gain across X and Y terminals ($V_{xd}/V_{yd}=1$) and a unity differential current gain between Z and X terminals ($I_{zd}/I_{xd}=1$). The ideal input impedance

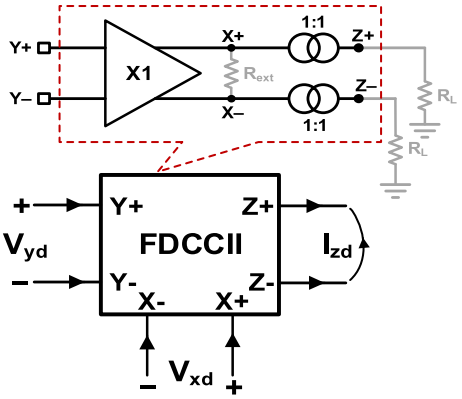


Fig. 1 Block diagram of a typical FDCCII.

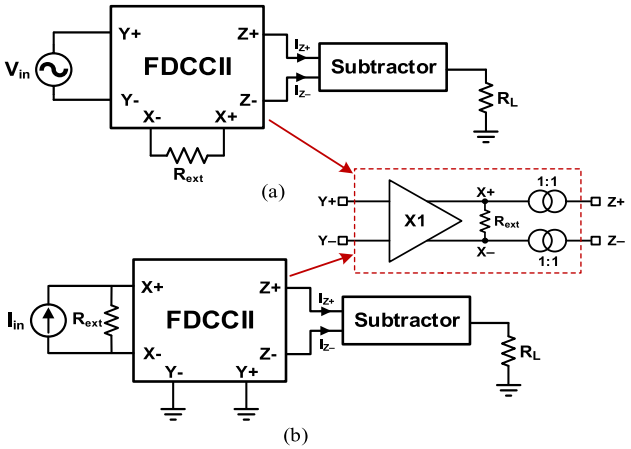


Fig. 2 CMIA configuration for **a** voltage input signals and **b** current input signals

at Y, input (output) impedance at X and output impedance at Z nodes are infinite, zero (infinite), and infinite, respectively. Practically, the non-ideal impedances at any abovementioned terminals, results in undesirable effects on the functionality of FDCCII.

The setup block diagrams of the implemented CMIA including the FDCCII followed by a current subtraction stage for voltage and current inputs are shown in Fig. 2a and b, respectively. The current subtracting circuit provides a single-ended topology enabling the CMIA to drive grounded loads.

$$\begin{bmatrix} I_{y+} \\ I_{y-} \\ V_{x+} \\ V_{x-} \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{y+} \\ V_{y-} \\ I_{x+} \\ I_{x-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

Also, the current subtractor cancels out the common-mode components of the output current signals at Z terminals resulting in a significant improvement in CMRR, which is a key characteristic of an IA.

The operation of the CMIA can be described based on the type of the input signal as follows. First, as it is shown in Fig. 2a, for voltage-input configuration, the unity gain voltage buffer between Y and X terminals transfers input voltage signals from Y to X [5] and assuming an ideal current conveyor, X_+ and X_- are receiving identical common mode signals. Thus, no common mode current signal is produced through the external resistor, R_{ext}. As a result, no common-mode current signal conveys from X to Z terminals through the current buffer, and hence no common-mode current passes through the resistive load (R_L). However, in real case, the existence of the common-mode signals cannot be ignored.

In case of current-input configuration, the current signal is applied to the low-impedance differential input terminal of X (Fig. 2b) and Y terminals are grounded. The common-mode components of the current signal are conveyed from X to Z through the unity-gain current buffer. Assuming a perfectly matched current mirrors in the current subtractor, any potentially common-mode current components can be removed at the final output using the current subtractor leading to higher voltage and current CMRR.

3 Current-mode instrumentation amplifier circuit

The design is mainly focusing on improving CMRR, targeting high-performance CMIA. The CMOS realization of the designed CMIA is shown in Fig. 3 consisting of the FDCCII and the current subtracting stage. Like most of the FDCCIIs [14, 27], the voltage tracking performance depends on the matching tolerances between output currents of two transconductors (M_1–M_8). Transistors M_1–M_2 and M_3–M_4 are the differential pairs of the input transconductor stages that share active loads of M_{25}–M_{26}. The differential pairs must be tightly matched to achieve a unity differential voltage gain from Y to X terminals. Using translinear loops in X terminals (including M_{T1}–M_{T8}), the internal impedances of X nodes get reduced resulting in very low impedance input terminals with higher absorption of current signal. A common-mode feed forward (CMFF) approach has been employed using M_5-M_8 to decrease common-mode voltage/current signals at nodes B, C, X_+, and X_-. In common mode condition, any common mode signals at Y (X) input terminals generate current signals in M_2 and M_3 (M_1 and M_4) and the same current signals will be generated in M_6 and M_7 (M_5 and M_8). Then, M_{23}-M_{26} generate the same

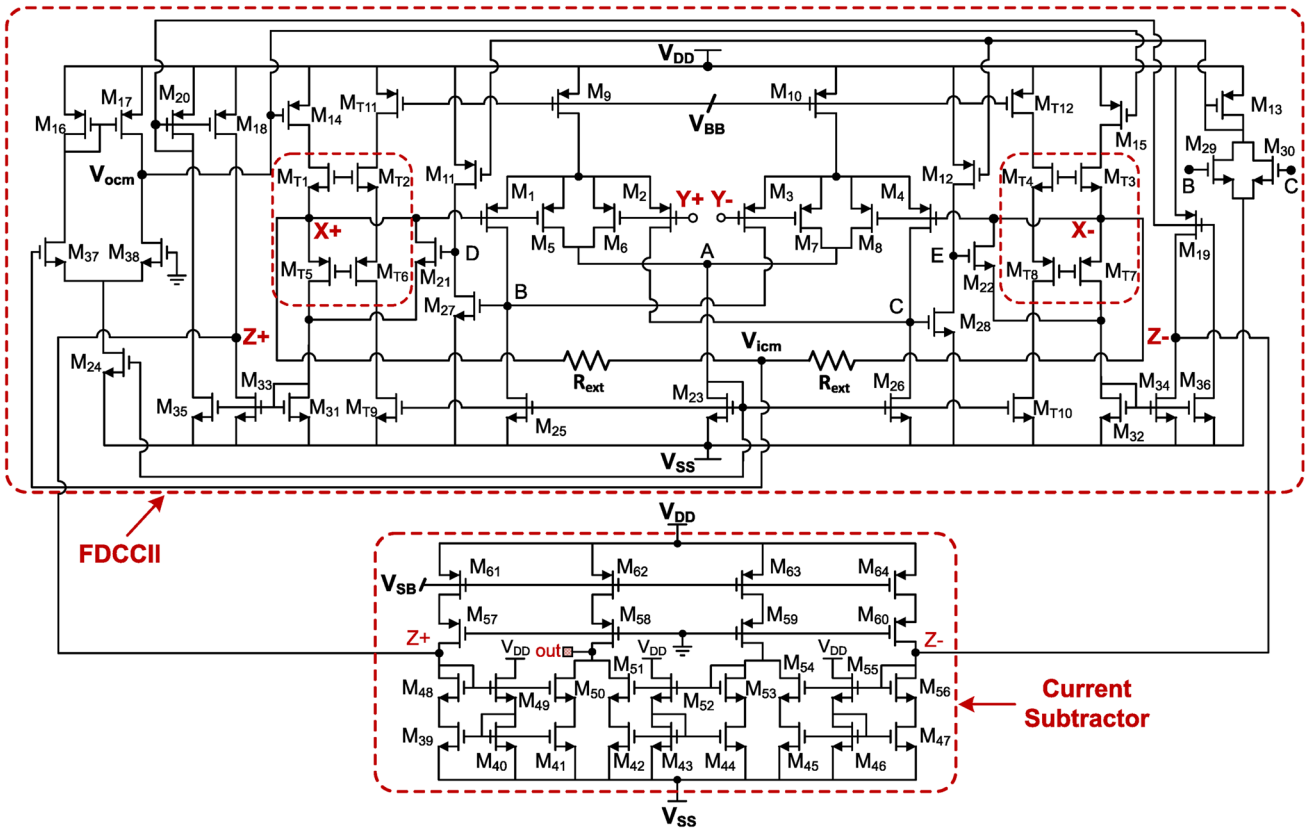


Fig. 3 Schematic of the designed CMIA

current signals with negative sign (as M_{23}–M_{26} are NMOS devices) and add them to B and C. Thus, at node B and C the effect of common mode current signals is removed following by the cancellation of the effect of common mode signals at X nodes. The CMFF technique makes voltage/current signals at B (C) and X_+ (X_-) to remain unchanged in the presence of common mode signals resulting in CMRR improvement.

To avoid amplification of common-mode voltage signals at M_{11} and M_{12} drains (D and E), another CMFF circuit was employed using current mirrors M_{11}-M_{13} and the pair of M_{29}- M_{30}. Any common mode signals at B and C generate common mode current signals in M_{27} and M_{28}. Then, M_{29}–M_{30} apply the same current signals (as the current signals in M_{27} and M_{28}) with negative sign to current mirror M_{11}–M_{13} and node D and E. Thus, the common-mode current signals of D and E nodes are cancelled following by the cancellation of common mode signals at X nodes and further improvement of CMRR. M_{31}-M_{34} are current buffer stages between X and Z terminals that should be matched to achieve a unity differential current gain. At Z terminals, the simple current mirror M_{18}–M_{20} along with transistors M_{35}–M_{36}, act as a CMFF technique. These transistors remove common-mode currents passing through Z terminals by adding the same current signals with negative sign to Z terminals resulting in current and voltage CMRR improvement.

The bias voltage of the current and voltage buffers is provided by V_{ocm}. This voltage is generated by the CMFB (Common Mode Feed Back) block consisting of the current mirror M_{16}-M_{17} and differential pair M_{37}–M_{38}. The function of the CMFB block is to set the common-mode voltages of X nodes to zero using negative feedback approach. By considering the internal mismatches in the FDCCII, the presence of common mode signals at Y terminals results in nonidentical common mode signals at X_+ and X_-. As a result, a common mode current signals flows through the external resistances R_{ext} due to the difference between X_+ and X_- potentials. This current signal changes the common-mode voltage of node V_{icm}. (M_{37} gate) This voltage variation, stimulates differential pair M_{37}–M_{38} to change M_{38} drain voltage (V_{ocm}) using M_{16} and M_{17}. Variation in

V_{ocm} changes common-mode currents passing through M_{14}–M_{15} using a negative feedback connection that finally prevents the common-mode currents to pass through M_{T1}–M_{T2}. As a result, the common mode signals at X_+ and X_- are removed.

The current subtracting stage consists of three improved Wilson current mirrors (M_{39}-M_{56}) with cascade active loads (M_{57}–M_{64}) [27] as it is shown in Fig. 3. The first current mirror (M_{39}-M_{41}, M_{48}–M_{50}) sends I_{z+} to the final output (node *out* in Fig. 3). The second and the third current mirrors (M_{42}- M_{44}, M_{51}- M_{53}, and M_{45}-M_{47}, M_{54}-M_{56}) convey $-I_{z-}$ to the output.

$$I_{z+,diff} \cong -I_{z-,diff}, I_{z+,com} \cong I_{z-,com} \begin{Bmatrix} I_{out,com} = I_{z+,com} - I_{z-,com} \cong 0 \\ I_{out,diff} = I_{z+,diff} - I_{z-,diff} \cong 2I_{z+,diff} \end{Bmatrix} \tag{2}$$

In common mode condition, $I_{z+,com} \cong I_{z-,com}$ and in differential mode condition $I_{z+,diff} \cong -I_{z-,diff}$. At the output node, $I_{out} = I_{z+} - I_{z-}$ flows through the resistive load connected to the output (R_L). This means (as expressed in Eq. 2), ideally the common-mode current signals of Z_+ and Z_- are removed at the output current flow through R_L, while the differential ones are doubled. This results in the improvement of differential gain and reduction in common mode gain which can be translated into a significant improvement in CMRR. In the following sections, the performance of the CMIA with and without current subtracting stage is studied in detail to investigate the effect of adding the current subtracting stage on the performance of the CMIA.

The voltage and current CMRRs are obtained using Eq. (3) and Eq. (4) where $\varepsilon_{1(2)}$ and $\varepsilon'_{1(2)}$ are the current tracking errors of the current subtracting stage for differential and common-mode signals, respectively and β_i for i = 1–9 are defined gains and errors (the detailed derivation is described in the Appendix). Also, the internal resistance of X terminals can be expressed using Eq. (5).

$$CMRR_V \cong \frac{\beta_7\left(CMRR_{V_{XY}} \times \left(\beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right) - \beta_4\right)(R_{ext} + r_x) + \beta_3\beta_4\alpha_2)}{\beta_3(\beta_8 - \beta_9)(R_{ext} + r_x)} \times \frac{1 + \varepsilon_{1(2)}}{1 + \varepsilon'_{1(2)}} \tag{3}$$

$$CMRR_I = \frac{\left(\beta_7\left(\left(CMRR_{V_{XY}} \times \beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right) - \beta_4\right)(R_{ext} + r_x) + \beta_3\beta_4\alpha_2\right)}{\left(CMRR_{V_{XY}} \times \beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right) \times \beta_3(\beta_8 - \beta_9) \times (R_{ext} + r_x)} \times \frac{\left(\beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right) \times (1 + \varepsilon_{1(2)})}{1 + \varepsilon'_{1(2)}} \tag{4}$$

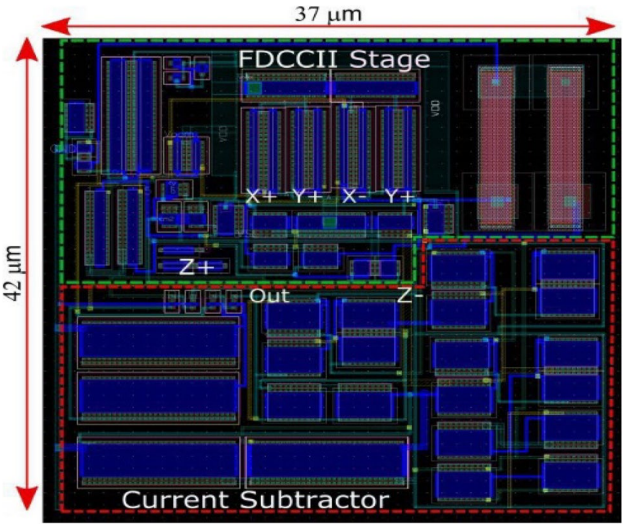


Fig. 4 The CMIA layout

$$r_{x+(-)} = \frac{1}{g_{mMT1(3)+}g_{mMT5(7)}} \tag{5}$$

4 Post-layout simulation results and discussion

The proposed circuit is designed and laid out in TSMC 130 nm single-poly, eight-metal CMOS process and its performance is evaluated using CADENCE software tool after parasitic (RC) extraction. Figure. 4 shows the CMIA layout which occupies an active area of only 37×42 µm^2. The transistor dimensions used in this design are listed in Table 1. In this simulation, the following parameters are set: $R_{ext} = 450$ Ω, $R_L = 1$ kΩ, the bias voltage applied to the gates of M_9, M_{10}, MT_{11}, and M_{T12} (V_{BB}) is 0.6 V, and the bias voltage of the current subtracting stage (V_{SB}) is 0.5 V, such that each transistor of the input differential pairs (M_1–M_8) have a current bias of approximately 4.2 µA.

4.1 Core fully differential second-generation current conveyors characterization

In this section, the performance of the stand-alone FDCCII is evaluated to ensure that the performance of the main building block is sufficient to support the CMIA operation. The post-layout and Monte Carlo (MC) simulation results on the most important design metrics of the FDCCII block including common mode and

Table 1 Transistor Sizes

Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)	Transistor	W/L (μm/μm)
M_1–M_8	6.4/0.5	M_{21}–M_{22}	6.1/0.6	M_{39}–M_{56}	3.6/2
M_9–M_{10}	5.4/1	M_{23}, M_{25}–M_{28}	2.3/1	M_{57}, M_{60}, M_{61}, M_{64}	0.4/0.2
M_{11}–M_{13}	1/0.8	M_{24}	4.6/1	M_{58}, M_{59}, M_{62}, M_{63}	10.4/2.6
M_{14}–M_{15}	2.4/0.5	M_{29}–M_{30}	1.2/1	M_{T1}–M_{T4}	1/0.5
M_{16}–M_{17}	9/1	M_{31}–M_{34}	0.4/1.6	M_{T5}–M_{T8}	2/0.6
M_{18}–M_{19}	0.4/0.5	M_{35}–M_{36}	0.2/2	M_{T9}–M_{T10}	1/0.4
M_{20}	0.4/0.6	M_{37}–M_{38}	0.9/0.6	M_{T11}–M_{T12}	4/0.8

Table 2 FDCCII characteristics

Parameter	Post-layout	MC Results		
		μ*	σ**	σ/μ
Vx_{diff}/Vy_{diff}	0.991003	0.978478	0.032712	3.34%
Vx_{com}/Vy_{com}	0.004420	0.004630	0.000628	13.56%
Iz_{+diff}/Ix_{diff}	0.975997	0.963255	0.034687	3.60%
Iz_{-diff}/Ix_{diff}	0.975810	0.963314	0.034577	3.59%
Iz_{+com} / Ix_{com}	4.075×10^{-6}	4.3182×10^{-6}	0.5066×10^{-6}	11.73%
X impedance (R_x) [Ω]	16.1	16.90	1.32	7.8%
Z impedance (R_z) [kΩ]	687.6	682.8	86.76	12.70%
3 dB B.W of Vx_{diff}/Vy_{diff} [MHz]	49.27	–		
3 dB B.W of Iz_{+com}/Ix_{+com} [MHz]	1.68	–		
3 dB B.W of Iz_{+diff}/Ix_{+diff} [MHz]	45.36	––		
Power consumption [μW]	446.2	–		

*μ = Mean value, **σ = Standard deviation

differential mode voltage and current gains between X and Y as well as Z and X, respectively, the BW of the differential gains, the internal impedance in X and Z terminals, and power consumption for 1000 iterations are given in Table 2. For differential signals, the FDCCII achieves an input voltage tracking error of ~ 0.009 from Y terminal to X terminal ($1-\frac{V_{xd}}{V_{yd}}$). In addition, the output differential current tracking error from X to $Z_{+(-)}$ terminal ($1-\frac{I_{z+(-)}}{I_{xd}}$) is approximately 0.024. The FDCCII also has a low impedance of 16.1 Ω at current input terminal of X_+ (X_-) and a high output impedance of ~ 687 kΩ at terminal Z_+ (Z_-). The frequency response of X terminal internal resistance, R_x, is shown in Fig. 5 which shows a low-frequency value of 16.1 Ω with a 3-dB BW of 2.53 MHz. MC simulation results demonstrate that the common-mode voltage and current gains are more susceptible to the device mismatches than the differential ones.

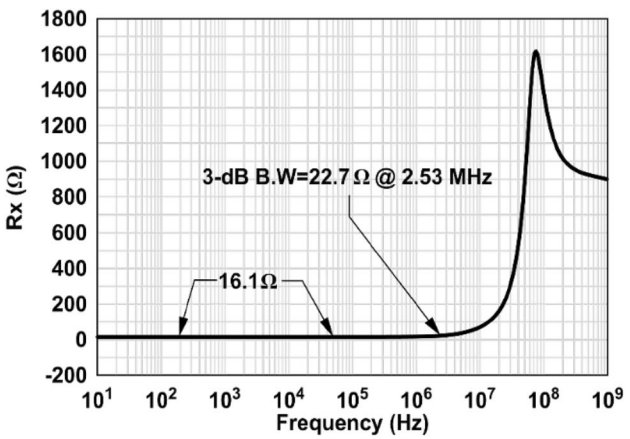


Fig. 5 X-terminals intrinsic resistance

4.2 Current-mode instrumentation amplifier characterization

The frequency responses of voltage and current CMRRs of the CMIA consisting of the FDCCII followed by the current subtracting stage are shown in Fig. 6. The designed CMIA achieves a high voltage CMRR of 228.8 dB with 3-dB BW of 10.0 kHz and a high current CMRR of 246 dB with 3-dB BW of 10.6 kHz at a supply voltage of ± 1.2 V. Figure 7a shows voltage and current CMRR magnitude at DC over different R_{ext}. An average voltage and current

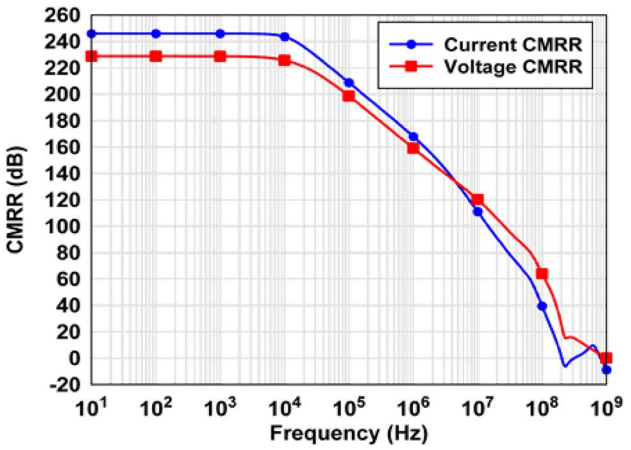


Fig. 6 Voltage and current CMRR when VDD = ±1.2 V, R_L=1kΩ, and R_{ext} = 450 Ω for the proposed CMIA

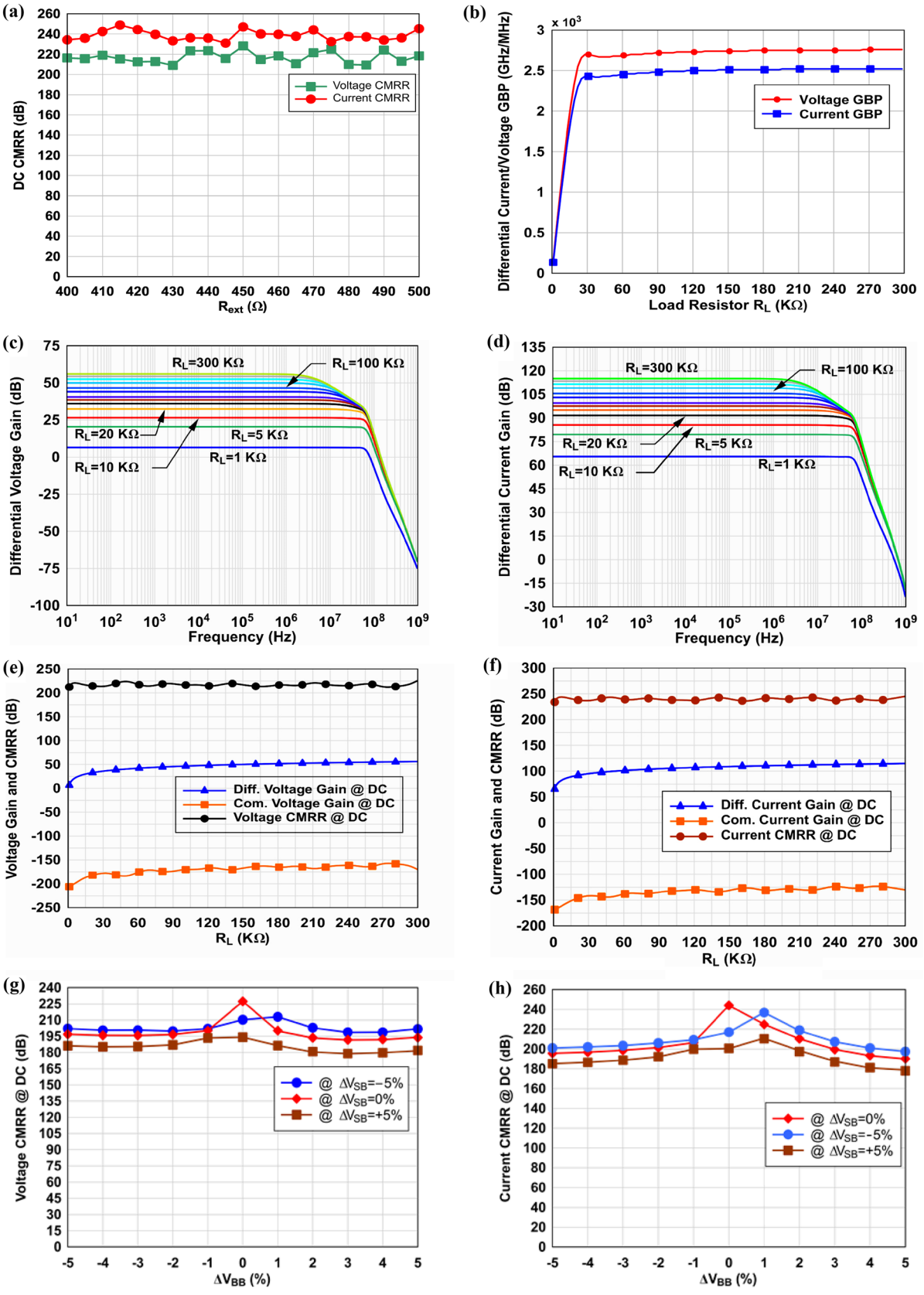
CMRR magnitude of ~220 and ~240 dB are obtained, respectively, when R_{ext} varies from 400 Ω to 500 Ω. Differential voltage and current gain-bandwidth products (GBPs) with different resistive loads (R_L) changing from 1 kΩ to 300 kΩ are shown in Fig. 7b. Also, Fig. 7c and d shows the differential voltage gain and current gain of the CMIA over different R_L. From Fig. 7b, it is obvious that for 1 kΩ ≤ R_L < 32 kΩ, both voltage and current GBPs were linearly increasing with the output load, indicating that the differential voltage/current gain increases with an increase in R_L, while the BW remains almost constant as shown in Fig. 7c and d. In this range of R_L, the trade-off between gain and BW that inherently exists in voltage-mode circuits is almost negligible. For R_L ≥ 32 kΩ, the compromise between gain and BW develops, leading to a decrease in GBPs rate. For R_L ≥ 100 kΩ, the CMIA behaves similar to a voltage mode circuit as the GBPs remain almost constant with increase in R_L suggesting that the magnitude of the differential gains is inversely proportional to the BW. The magnitude of differential gain, common mode gain, and CMRR at DC frequency over different R_L for the CMIA with voltage and current input signals, are shown in Fig. 7e and f, respectively. Based on the figures, it is obvious that by increasing the R_L, the differential gain magnitude increased, but increasing R_L resulted in the decrease of common mode gain magnitude; as a result, the CMRR for both voltage and current signals remained almost constant over different R_L. Figure 7g and h shows the voltage and current CMRR magnitude at DC over different V_{BB}, changing from $0.95 \times V_{BB}$ ($\Delta V_{BB} = -5\%$) to $1.05 \times V_{BB}$ ($\Delta V_{BB} = +5\%$) while ΔV_{SB} is 0%, + 5%, or − 5%, respectively. Based on Fig. 7g and h, the voltage and current CMRR magnitudes are > 180 dB while bias voltages are changing by ± 5% and this magnitude of CMRRs are close to Monte Carlo results shown in Fig. 8. Also, the current CMRR magnitude is more sensitive to variations in the bias voltages when compared to that of voltage CMRR.

The impact of local process variations on voltage and current CMRRs of the CMIA and their BWs is investigated using Monte Carlo (MC) analysis with 1000 runs. The obtained results are shown in Fig. 8 indicating that both the current and voltage CMRRs have almost equal mean values of ~ 185 dB with ~ 11.3 kHz of 3 dB-BWs. The positive and negative PSSR curves ($PSRR_+$ and $PSRR\_$) are depicted in Fig. 9. The $PSRR_+$ and PSRR − are 108.2 dB and 99.7 dB at DC frequencies, respectively. Figure 10 illustrates the input referred noise of the CMIA from 10 to 100 kHz. The rms value of the input referred noise is 3.61 µV, integrated from 10 to 1 kHz. The simulation results also indicate that the output offset of the CMIA is 1.67 µV. Table 3 summarizes the performance of the CMIA and compares it with the single FDCCII block. In the case where the current subtractor is detached from the FDCCII outputs, and two load resistors of 1 kΩ are connected to Z_+ and $Z\_$, while other circuit parameters and simulation conditions remain unchanged. The results verify the effectiveness of incorporation of the current subtracting stage in the CMIA as it enhances current and voltage CMRRs by 131 and 110 dB, respectively, while increasing power consumption by only 12%.

4.3 Process, voltage, and temperature variations' influence

In this section the robustness of the proposed CMIA against process, voltage, and temperature (PVT) variations is investigated in details. The simulated differential voltage gain from X to Y and differential current gain from Z to X for the FDCCII block in different process corners including Typical-Typical (TT), Slow-Slow (SS), Fast-Slow (FS), Slow-Fast (SF), and Fast–Fast (FF) are shown in Fig. 11a and b, respectively. In Fig. 11a and b, the worst corners of FS and FF shows a maximum of ~ 10 and ~ 5% variation in differential voltage and current gains, respectively, when compared to TT condition. In addition to the FDCCII, the aforementioned five process corners for the simulated voltage and current CMRRs of the CMIA are shown in Fig. 11c and d, respectively. For the CMIA, the average low-frequency voltage/current CMRR over different process corners is 204.1 dB/200.2 dB while a maximum variation of 16.5%/32.9%, with respect to the TT corner, is observed at FF/FF corner. Moreover, 3 dB-BW for the voltage/current CMRR remains above 7.94 kHz/7.82 kHz in the worst corner (SS/FS).

The performance summary of the CMIA over temperature range of − 25 °C to 75 °C at ± 1.2 V supply voltage is shown in Table 4. A minimum CMRR of ~ 170 dB is achieved


(a)
DC CMRR (dB)
Rext (Ω)
Voltage CMRR
Current CMRR
(b)
x 10^3
Differential Current/Voltage GBP (GHz/MHz)
Load Resistor RL (KΩ)
Voltage GBP
Current GBP
(c)
Differential Voltage Gain (dB)
Frequency (Hz)
RL=300 KΩ
RL=100 KΩ
RL=20 KΩ
RL=5 KΩ
RL=10 KΩ
RL=1 KΩ
(d)
Differential Current Gain (dB)
Frequency (Hz)
RL=300 KΩ
RL=100 KΩ
RL=20 KΩ
RL=5 KΩ
RL=10 KΩ
RL=1 KΩ
(e)
Voltage Gain and CMRR (dB)
RL (KΩ)
Diff. Voltage Gain @ DC
Com. Voltage Gain @ DC
Voltage CMRR @ DC
(f)
Current Gain and CMRR (dB)
RL (KΩ)
Diff. Current Gain @ DC
Com. Current Gain @ DC
Current CMRR @ DC
(g)
Voltage CMRR @ DC (dB)
ΔVBB (%)
@ ΔVSB=−5%
@ ΔVSB=0%
@ ΔVSB=+5%
(h)
Current CMRR @ DC (dB)
ΔVBB (%)
@ ΔVSB=0%
@ ΔVSB=−5%
@ ΔVSB=+5%

◂**Fig. 7** **a** Voltage and current CMRR magnitude at DC over different Rext varying from 400 to 500 Ω. **b** Voltage and current GBP **c** differential voltage gain, and **d** differential current gain for different R_L from 1 kΩ to 300 kΩ. **e** and **f** the magnitude at DC frequency of differential, common mode and CMRR over different R_L for the CMIA with voltage and current input signals, respectively. **g** Voltage and **h** current CMRR magnitude at DC over different V_{BB} and V_{SB}. Note: in **b**–**h** R_{ext} is 450 Ω

for both current and voltage signals at − 25 °C which is quite comparable to that of the recently reported CMIA designs [14, 19, 27]. Despite the CMRR magnitude, the voltage/current CMRR 3 dB-BW is less vulnerable to the temperature changes as it remains above 10 kHz/9.5 kHz over the entire temperature range.

In addition to ± 1.2 V supply voltage, the CMIA is characterized for lower supply voltages of ± 1.0 V, ± 0.8 V, and

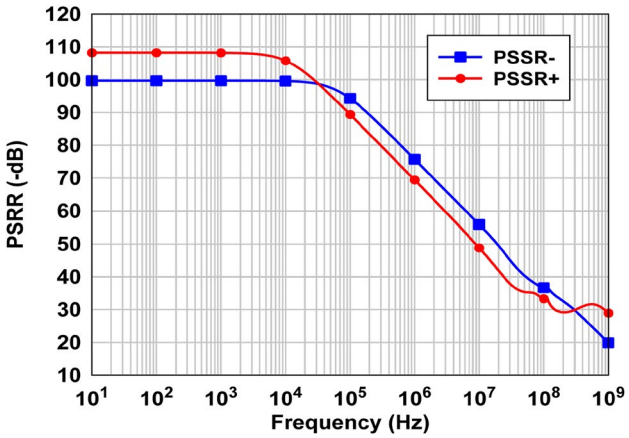


Fig. 9 Simulated $PSRR_+$ and $PSRR_-$ of the CMIA

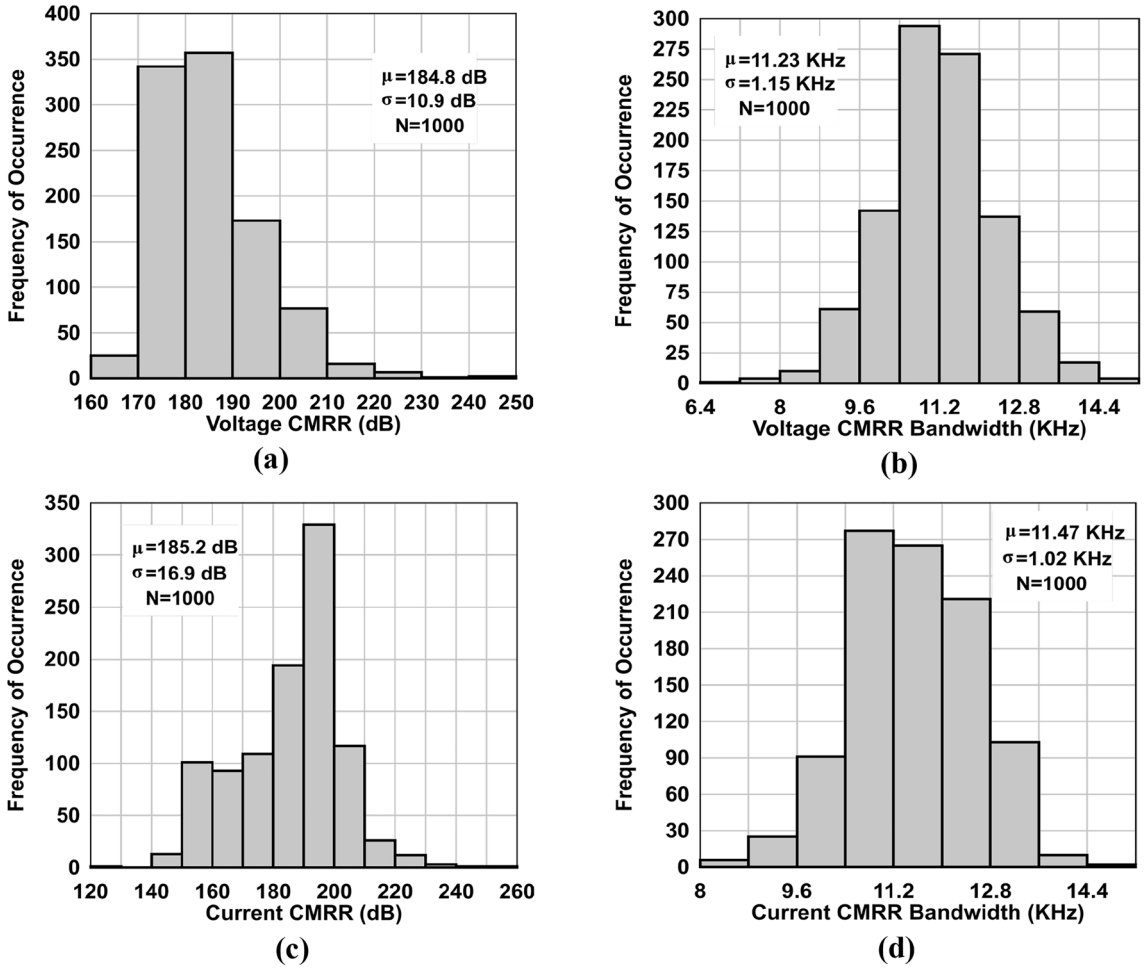


Fig. 8 Monte Carlo results for **a** voltage CMRR, **b** voltage CMRR 3dB-Band Width; **c** current CMRR and **d** current CMRR 3dB-Band Width for the proposed CMIA

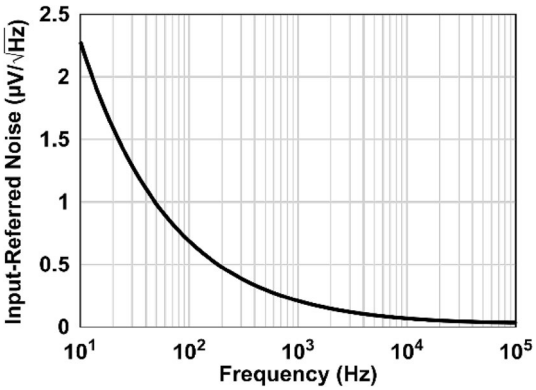


Fig. 10 Simulated input-referred noise of the CMIA

even ± 0.6 V at room temperature as it is shown in Table 4. The CMIA exhibits nearly similar CMRRs' performances with ± 1 V and ± 0.8 V while the CMRRs' BWs are approximately scaled down with the voltage supply. Also, it shows 15.2%/17.8% and 13.1%/23.3% voltage/current CMRR reduction when voltage supply is reduced from ± 1.2 V to ± 1 V and ± 0.8 V, respectively. While a voltage/current CMRR of 185.6 dB/191.9 dB is obtained from ± 0.6 V supply voltage (which corresponds to only 18.8%/21.9% reduction in voltage/current CMRR compared to ± 1.2 V nominal supply voltage at room temperature), the power consumption significantly decreases from 507.2 to 72.8 μW which can be translated into ~ 86% reduction, as it is shown in Table 4.

Table 5 summarizes the CMIA performance and compares it to previously published designs. The novel CMIA exhibits superior performance in terms of CMRR for both voltage and current inputs without the need for accurately matched components. To make a fair comparison, a figure of merit (FoM) is defined in Eq. 6.

$$FoM = \max\left(\frac{CMRR_V \times BW_{\mathrm{CMRR}_V}}{P}, \frac{CMRR_I \times BW_{\mathrm{CMRR}_I}}{P}\right) \quad (6)$$

In Eq. 6, $CMRR_V$ and $CMRR_I$ are low-frequency voltage and current CMRRs, respectively, BW_{CMRR_V} and BW_{CMRR_I} are their corresponding 3-dB BWs (in kHz), and P is the power consumption (in μW). The FoM reflects the ability of a CMIA to reject the frequency components of common-mode signals at a given power consumption. To provide a fair comparison, same voltage/current CMRR and BW are assumed in FoM calculations when either of the data was not reported.

5 Conclusion

In this paper, a novel high CMRR CMIA in 130-nm CMOS technology is proposed. The CMIA includes an FDCCII to accurately convey the differential signals which is followed by a current subtracting stage to remove the common-mode components from the output current. The employed CMFB and CMFF techniques along with an accurate common-mode current subtraction stage

Table 3 CMIA characteristics with and without current subtractor

Parameter	CMIA without Current Subtractor (FDCCII with resistive loads at Z_+ and Z_-)				CMIA (FDCII followed by Current Subtractor and resistive load at node '*out*')			
	Post-layout	MC Results			Post-layout	MC Results		
		μ*	σ**	σ/μ		μ*	σ**	σ/μ
Voltage CMRR [dB]	118.8	106.51	12.73	11.9%	228.8	184.8	10.9	5.9%
Current CMRR [dB]	114.7	106.88	18.47	17.28%	245.9	185.2	16.9	9.12%
Voltage CMRR 3 dB- BW [KHz]	4580	4780	314	6.56%	10.0	11.23	1.15	10.02%
Current CMRR 3 dB-BW [KHz]	1770	1882	218	11.58%	10.6	11.47	1.02	9.08%
Differential Voltage Gain 3 dB- BW [MHz]	89.31	84.35	6.75	8.0%	69.6	65.3	6.21	9.5%
Differential Current Gain 3 dB- BW [MHz]	84.23	81.76	5.91	7.22%	70.4	67.4	5.46	8.1%
PSRR + / PSRR- [dB]	50.6/69.5	–			108.2/99.7	–		
Power [μW]	446.2	–			507.2	–		

* μ = Mean value, ** σ = Standard deviation

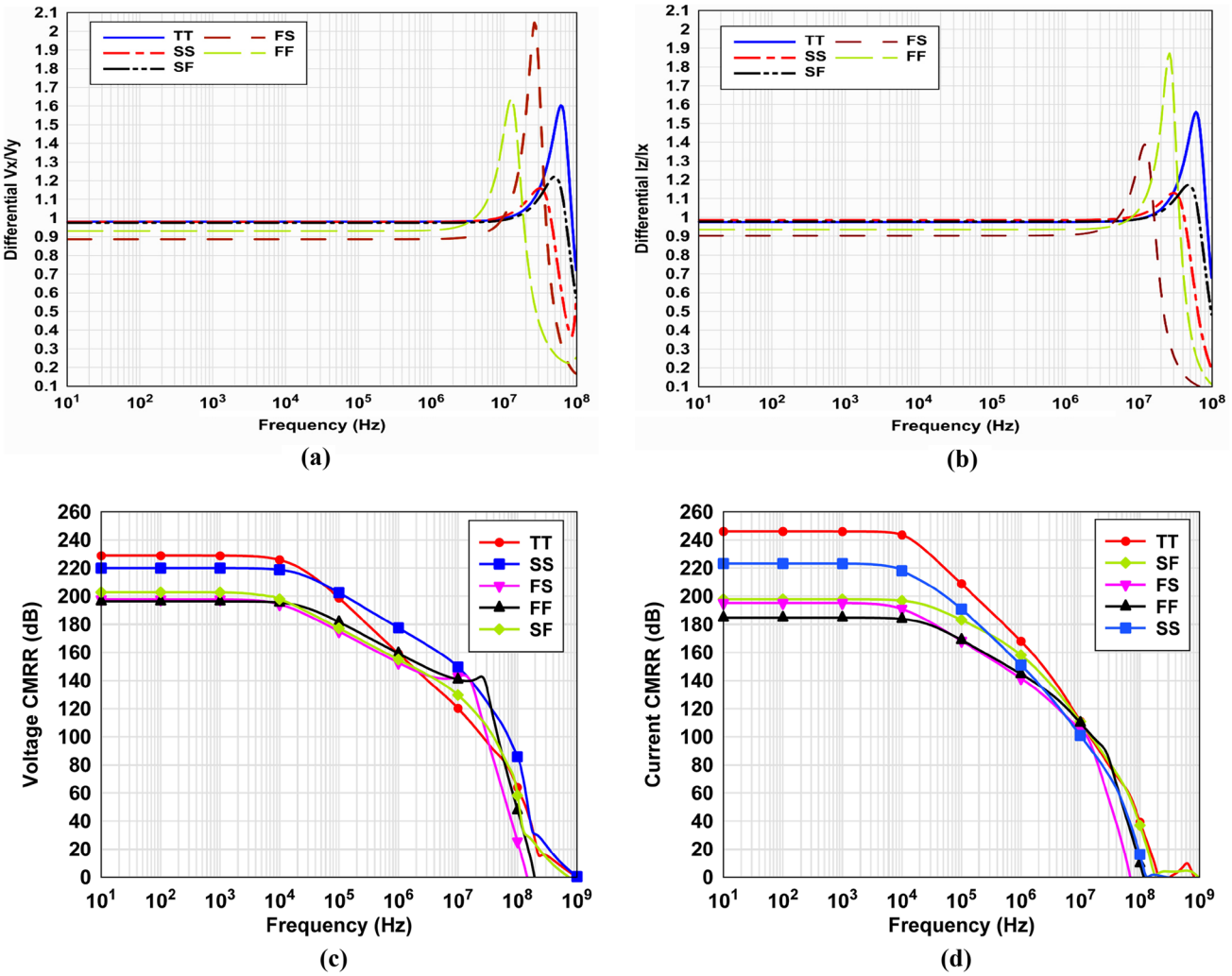


Fig. 11 Corner analyses for **a** differential voltage gain from X to Y and **b** differential current gain from Z to X of the FDCCII block. Corner analyses for **c** Voltage CMRR, and **d** current CMRR of the proposed CMIA

Table 4 CMIA performance over temperature and different supply voltages

Temperature [°C]	− 25	0	27				50	75
Supply Voltage [V]	± 1.2	± 1.2	± 1.2	± 1*	± 0.8**	± 0.6†	± 1.2	± 1.2
Voltage CMRR [dB]	170.6	179.3	228.7	193.8	198.6	185.6	185.10	181.37
Voltage CMRR BW [KHz]	10.21	10.52	10.02	8.79	9.12	11.1	15.80	20.92
Current CMRR [dB]	170.0	188.6	245.9	202.9	188.5	191.9	192.5	186.1
Current CMRR BW [KHz]	9.55	11.32	10.63	8.98	7.62	8.78	15.81	20.03
Power [µW]	–		507.2	454.8	213.9	72.8	–	

*V_{SB} = 0.4 V, V_{BB} = 0.4 V; **V_{SB} = 0.3 V, V_{BB} = 0.25 V; †V_{SB} = 0.15 V, V_{BB} = 0.15 V

Table 5 A comparison table summarizing the performance metrics of this work with others

Parameter	This Work				[19] (2017)	[13] (2011)	[28] (2022)	[29] (2019)	[30] (2019)	[31] (2021)
Signal Type	Voltage		Current		Voltage	Current	Voltage	Voltage	Voltage	Voltage
CMOS Technology [nm]	130				130	180	180	180	180	180
Supply Voltage [V]	±1.2	±0.6	±1.2	±0.6	0.4	±0.8	1.8	±0.9	1.8	±1.2
CMRR @ DC [dB]	228.8	197.3	246	159.6	64.7	91	135	147.68	127	~110
CMRR 3 dB BW [kHz]	10.0	11.1	10.6	8.78	100	1.15	<5	~20	13.78	N.A
Diff. Gain 3 dB BW [MHz]	69.6	37.3	70.4	38.7	<381	10.18	N.A	0.777	1	N.A
Power [μW]	507	72.8	507	72.8	14	219	N.A (1.89 μA)	38.88	9	N.A (2.3 μA)
Input Referred Noise [μV_{rms}]	3.61 (10–1000 Hz)				1.1 (0.07–150 Hz)	N.A	3.14 (0.5–5 kHz)	N.A	N.A	3.2 (0.5–400 Hz)
Area [mm^2]	0.00155				0.021	N.A	0.227	N.A	N.A	1.57
FoM/FoM*	1				0.29×10^{-6}	0.45×10^{-8}	1.02×10^{-5}	2.28×10^{-3}	6.31×10^{-4}	0.11×10^{-5}

This work when VDD is ± 1.2 V (FoM = 41.7 × 109)

allows the CMIA to achieve a high CMRR for both types of input signals. Post-layout simulation results have demonstrated the robustness of the CMIA against PVT variations. The CMIA's ability to efficiently operate with 50% of its nominal supply voltage as well as the small silicon area, and low power dissipation makes it suitable for battery-powered and portable health monitoring systems. Future research focuses on realizing the circuit using the same technology and demonstrate its high CMRR performance and feasibility for fabricating standalone health monitoring devices such as highly sensitive portable stethoscopes for measuring electroencephalography (EEG) signals.

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Data availability The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of interest The authors have no relevant financial or non-financial interests to disclose.

Ethical approval This article does not contain any studies with human participants or animals performed by any of the authors.

Appendix

This section describes the governing equations of the proposed FDCCII. In the following calculations, R_{ext} has not been considered.

Voltage gain between X and Y

If differential input voltage of $V_{Y_{diff}} = V_{Y_+} - V_{Y_-}$ ($V_{Y+} = -V_{Y-} = \frac{V_{Ydiff}}{2}$) is applied to Y-terminals, Eq. (7) to Eq. (8) could be concluded. The drain currents of M_1 (M_2) and M_5 (M_6) can be written as Eq. (7), where V_{sM1} and V_{sM5} are the source voltages of M_1 and M_5.

$$i_{ac1(2)} = g_{m1(2)}\left(V_{X(Y)+} - V_{sM1}\right),\ i_{ac5(6)} = g_{m5(6)}\left(V_{Y(X)-} - V_{sM5}\right) \tag{7}$$

Applying KCL at the source of M_1, we arrive at:

$$\begin{aligned}\frac{-V_{sM1(5)}}{r_{o9(10)}} &= \left(\left(g_{m1(6)} + g_{m3(8)}\right) \times \left(V_{X+(-)} - V_{sM1(5)}\right)\right) \\ &+\left(\left(g_{m2(5)} + g_{m4(7)}\right) \times \left(V_{Y-(+)} - V_{sM1(5)}\right)\right) \\ V_{sM1(5)} &= \frac{-\left(\left(g_{m1(6)} + g_{m3(8)}\right) \times V_{X+(-)} + \left(g_{m2(5)} + g_{m4(7)}\right) \times V_{Y-(+)}\right)}{\frac{1}{r_{o9(10)}} + \left(g_{m1(6)} + g_{m3(8)}\right) + \left(g_{m2(5)} + g_{m4(7)}\right)}\end{aligned} \tag{8}$$

using (7) and (8), small signal voltage and internal resistance at node B(C) can be written as Eq. (9) and (10):

$$\begin{aligned} V_{B(C)} &= \left(i_{ac1(2)} + i_{ac5(6)}\right) R_{outB(C)} \\ &= R_{outB(C)}\left(V_{x+(-)}A_{1(2)} - V_{x-(+)}A_{3(4)} \right. \\ &\quad \left. + V_{y-(+)}A_{5(6)} - V_{y+(-)}A_{7(8)}\right) \end{aligned} \tag{9}$$

$$R_{outB(C)} = r_{o25(26)} // r_{o9(10)} g_{m1(6)} r_{o1(6)} // r_{o10(9)} g_{m5(2)} r_{o5(2)} \cong r_{o25(26)} \tag{10}$$

where A_is can be derived based on Eq. (1) and (2) as follow:

$$\begin{aligned} A_{1(2)} &= g_{m1(6)} - g_{m1(6)} r_{o9(10)} \frac{g_{m1(6)} + g_{m3(8)}}{-1 + r_{o9(10)}\left(g_{m1(6)} + g_{m2(5)} + g_{m3(8)} + g_{m4(7)}\right)} \\ A_{3(4)} &= g_{m5(2)} r_{o10(9)} \frac{g_{m6(1)} + g_{m8(3)}}{-1 + r_{o10(9)}\left(g_{m5(2)} + g_{m6(1)} + g_{m7(4)} + g_{m8(3)}\right)} \\ A_{5(6)} &= g_{m5(2)} - g_{m5(2)} r_{o10(9)} \frac{g_{m5(2)} + g_{m7(4)}}{-1 + r_{o10(9)}\left(g_{m5(2)} + g_{m6(1)} + g_{m7(4)} + g_{m8(3)}\right)} \\ A_{7(8)} &= g_{m1(6)} r_{o9(10)} \frac{g_{m2(5)} + g_{m4(7)}}{-1 + r_{o9(10)}\left(g_{m1(6)} + g_{m2(5)} + g_{m3(8)} + g_{m4(7)}\right)} \end{aligned} \tag{11}$$

When differential voltage signal is applied to the input nodes (Y_+, Y_-), as $V_{gs1} = V_{gs3}, V_{gs2} = V_{gs4}, V_{gs5} = V_{gs7}, V_{gs6} = V_{gs8}$ and M_1-M_8 have the same bias current, we can assume that $g_{m1} = g_{m3}, g_{m2} = g_{m4}, g_{m5} = g_{m7}, g_{m6} = g_{m8}$. In addition, in the denominator of Eq. (11) $r_{o9(10)}\left(g_{m1(6)} + g_{m2(5)} + g_{m3(8)} + g_{m4(7)}\right) \gg -1$. As a result, A_1-A_8 can be expressed as Eq. (12) and $V_{B(C)}$ can be simplified to Eq. (13). On the other hand, when a common-mode voltage is applied to the input nodes (terminals Y) since the bias currents of M1–M8 are not equal anymore, A_1-A_8 are defined as previously shown in Eq. (11).

$$\begin{aligned} A_1 = A_4 = A_6 = A_7 &= \frac{g_{m1} \times g_{m2}}{g_{m1} + g_{m2}}, \\ A_2 = A_3 = A_5 = A_8 &= \frac{g_{m5} \times g_{m6}}{g_{m5} + g_{m6}} \end{aligned} \tag{12}$$

$$V_{B(C)} = R_{outB(C)} \frac{g_{m1(5)} \times g_{m2(6)}}{g_{m1(5)} + g_{m2(6)}} \left(\left(V_{x+(-)} - V_{x-(+)}\right) - \left(V_{y+(-)} - V_{y-(+)}\right)\right) \tag{13}$$

The drain voltage and internal resistance of M_{11}(M_{12}) are shown in Eq. (14) and (15), respectively. Using Eq. (14) and KCL at X_+ (X_-), voltage at X_+ (X_-) node is as Eq. (16).

$$V_{d,M11(12)} = -i_{ac27(28)} R_{outdM11(12)} = -g_{m27(28)} . R_{outd,M11(12)} . V_{B(C)} \tag{14}$$

$$R_{outdM11(12)} = r_{o27(28)} // r_{o11(12)} \tag{15}$$

$$V_{x+(-)} = V_{dM11(12)} \frac{g_{m21(22)} r_{o14(15)}}{\left(g_{m21(22)} r_{o14(15)} + g_{m31(32)} + r_{o14(15)} + 1\right)} \tag{16}$$

Based on Eq. (1) to (10), voltage at terminal X is simplified as follow:

$$V_{x+(-)} = A_{9(10)} A_{1(2)} \left(\left(V_{x+(-)} - V_{x-(+)}\right) - \left(V_{y+(-)} - V_{y-(+)}\right)\right) \tag{17}$$

where,

$$\begin{aligned} A_{9(10)} &= -g_{m27(28)} . \left(r_{o27(28)} // r_{o11(12)}\right) \\ &\quad \times \frac{g_{m21(22)} r_{o14(15)} \times r_{o25(26)}}{\left(g_{m21(22)} r_{o14(15)} + g_{m31(32)} + r_{o14(15)} + 1\right)} \end{aligned}$$

For differential-mode voltage signals ($V_{Y+} = -V_{Y-} = \frac{V_{Ydiff}}{2}$), based on Eq. (18), we get:

$$V_{x+} - V_{x-} = V_{xdiff} = V_{Ydiff}\left(\beta_4 - \frac{\beta_2 \beta_3}{2\beta_1}\right) \tag{18}$$

As a result, the differential gain between X and Y is as follow in Eq. (19).

$$Av_{XYdiff} = \frac{V_{Xdiff}}{V_{Ydiff}} = \beta_4 - \frac{\beta_2 \beta_3}{2\beta_1} \tag{19}$$

Where,

$$\begin{aligned} \beta_1 &= 1 - A_1 A_9 - A_2 A_{10} \cong -\left(A_1 A_9 + A_2 A_{10}\right) \\ &= -\frac{+A_{10}\left(g_{m5} g_{m6}\left(g_{m1} + g_{m2}\right)\right)}{\left(g_{m1} + g_{m2}\right) \times \left(g_{m5} + g_{m6}\right)} \end{aligned}$$

$$\beta_4 = \frac{A_1 + A_2}{2A_2} = \frac{g_{m1} g_{m2}\left(g_{m5} + g_{m6}\right) + g_{m5} g_{m6}\left(g_{m1} + g_{m2}\right)}{2\left(g_{m5} g_{m6}\left(g_{m1} + g_{m2}\right)\right)}$$

On the other hand, According to Eq. (18) , for common-mode voltage signals ($V_{Y+} = V_{Y-} = V_{Ycom}$) we have:

$$V_{x+} = V_{x-} = V_{xcom} = V_{Ycom} \times \left(\beta_6 - \frac{\beta_5 \beta_7}{\beta_1}\right) \tag{20}$$

and therefore, the common-mode gain between X and Y can be derived as follows:

$$Av_{XYcom} = \frac{V_{Xcom}}{V_{Ycom}} = \beta_6 - \frac{\beta_5 \beta_7}{\beta_1} \tag{21}$$

where,

$$\beta_5 = A_3 A_9\left(A_6 - A_8\right) + \left(A_5 - A_7\right)\left(1 - A_2 A_{10}\right)$$

$$\beta_6 = \frac{A_5 - A_7}{A_3 A_9}$$

$$\beta_7 = \frac{A_3 A_9 - A_1 A_9 + 1}{A_3 A_9} \cong \frac{A_3 - A_1}{A_3}$$

Current Gain between X and Z terminals

The internal resistance of X nodes can be derived as:

$$r_{x+(-)} \cong \frac{1}{g_{m\mathrm{MT1(3)}+}g_{m\mathrm{MT5(7)}}} \tag{22}$$

For current input signals, the output current signal at Z terminals are as follow:

$$\begin{aligned} i_{Z+(-)} &= \alpha_{1(2)} i_{X+(-)} \rightarrow i_{Z+(-)} = \frac{V_{Z+(-)}}{R_L} \\ &= \alpha_{1(2)} \frac{V_{X+(-)}}{R_{ext}//r_{x+}} \rightarrow \frac{V_{Z+(-)}}{V_{X+(-)}} = \frac{\alpha_{1(2)} R_L}{R_{ext}//r_{x+}} \end{aligned} \tag{23}$$

Where,

$$\alpha_{1(2)} = \frac{i_{M31(32)}}{i_{M33(34)}} = \frac{\left(V_{gs31(32)} - V_{Th31(32)}\right)}{\left(V_{gs31(32)} - V_{Th33(34)}\right)} \times \frac{1 + \lambda \frac{V_{X+(-)}}{g_{m21(22)} r_{o21(22)}}}{1 + \lambda V_{Z+(-)}}$$

For differential mode current signals, ignoring the channel-length modulation effect (λ), the current gain between Z and X terminals can be expressed as follow:

$$\begin{aligned} i_{Zdiff} &= i_{Z+} - i_{Z-} = V_{X+}\left(\frac{\alpha_1}{R_{ext}//r_{x+}}\right) - V_{X-}\left(\frac{\alpha_2}{R_{ext}//r_{x-}}\right) \\ &= V_{X+} \times \beta_7 + \frac{\beta_4 \alpha_2}{R_{ext}//r_{x-}} V_{ydiff} \end{aligned} \tag{24}$$

According to Eq. (18) and (19), we have:

$$V_{X+} = \frac{V_{xdiff} - \beta_4}{\beta_3},\ V_{ydiff} = \frac{V_{xdiff}}{Av_{XYdiff}} \tag{25}$$

Assuming that $r_{x+} = r_{x-} = r_x$ and, as a result $V_{xdiff} = r_x i_{xdiff}$, and using Eq. 24)ifferential current Z terminal can be calculated by Eq. (26) as follow.

$$i_{Zdiff} = i_{Xdiff}\left(r_x\left(\beta_7 \frac{Av_{XYdiff} - \beta_4}{\beta_3 Av_{XYdiff}} + \frac{\beta_4 \alpha_2}{Av_{XYdiff}(r_x)}\right)\right) \tag{26}$$

Therefore, the differential current gain between X and Z nodes can now be expressed as given in Eq. (27).

$$Ai_{ZXdiff} = \frac{i_{Zdiff}}{i_{Xdiff}} = r_x\left(\beta_7 \frac{Av_{XYdiff} - \beta_4}{\beta_3 Av_{XYdiff}} + \frac{\beta_4 \alpha_2}{Av_{XYdiff}(R_{ext} + r_x)}\right) \tag{27}$$

Where,

$$\beta_7 = \frac{\alpha_1}{R_{ext}//r_{x+}} + \frac{\alpha_2(1 - A_1 A_9)}{A_3 A_9 (R_{ext}//r_{x-})}$$

Moreover, the differential voltage gain between Y and Z nodes can be calculated by Eq. (28) as follows:

$$Av_{ZYdiff} = \frac{V_{zdiff}}{V_{Ydiff}} = \frac{i_{Zdiff} R_L}{\left(\frac{r_x i_{Xdiff}}{Av_{XYdiff}}\right)} = \frac{R_L}{r_x} \times Av_{XYdiff} \times Ai_{ZXdiff} \tag{28}$$

For common-mode current signals ($V_{Y+} = V_{Y-} = V_{Ycom}$), the common-mode current signal at Z terminals are given by Eq. (29).

$$i_{Zcom} = V_{X+com}\left(\frac{\alpha_1}{2R_{ext}//r_{x+}}\right) - V_{X-com}\left(\frac{\alpha_2}{2R_{ext}//r_{x-}}\right) \tag{29}$$

Assuming $r_{x+} = r_{x-} = r_x, r_x \ll 2R_{ext}$ and as $V_{xcom} = r_x i_{xcom}$, then froEq. (11a), we obtain:

$$\left(\beta_8 - \beta_9\right), V_{Ycom} = \left(\beta_8 - \beta_9\right)\frac{r_x i_{xcom}}{Av_{XYcom}} \tag{30}$$

As a result, the common-mode current and voltage gains between X and Z nodes can be derived as given in Eq. (31) and Eq. (32), respectively.

$$Ai_{ZXcom} = \frac{i_{Zcom}}{i_{Xcom}} = \frac{\left(\beta_8 - \beta_9\right) r_x}{Av_{XYcom}} \tag{31}$$

$$i_{Zcom} = \frac{V_{Zcom}}{R_L} = \left(\beta_9\right) V_{Ycom} \rightarrow Av_{ZYcom} = \frac{V_{Zcom}}{V_{Ycom}} = R_L\left(\beta_8 - \beta_9\right) \tag{32}$$

Where,

$$\beta_8 = \frac{\alpha_1}{2R_{ext}//r_{x+}} \times \left(\frac{(A_6 - A_8)A_3 A_9 A_{10} - \left(A_9 A_5 - A_9 A_7\right)\left(1 - A_2 A_{10}\right)}{A_3 A_9 - \left(1 - A_2 A_{10}\right)\left(1 - A_1 A_9\right)}\right)$$

$$\beta_9 = \frac{\left(A_9 A_5 - A_9 A_7\right) A_4 A_{10} - \left(A_6 A_{10} - A_8 A_{10}\right)\left(1 - A_1 A_9\right)}{A_4 A_{10}\left(A_3 A_9 - \left(1 - A_2 A_{10}\right)\left(1 - A_1 A_9\right)\right)}$$

Voltage and CurrenCMRR

By combining Eq. (19) and (21), voltage CMRR between X and Y terminals is obtained as given in Eq. (27), (30)

$$CMRR_{V_{XY}} = \frac{Av_{XYdiff}}{Av_{XYcom}} = \frac{\beta_4 - \frac{\beta_2 \beta_3}{2\beta_1}}{\beta_6 - \frac{\beta_5 \beta_7}{\beta_1}} \tag{33}$$

Using (28) and (31), voltage CMRR between terminals Z and Y can be expressed by Eq. (34) as follows.

$$CMRR_{V_{ZY}} = \frac{Av_{ZYdiff}}{Av_{ZYcom}} = \frac{\beta_7\left(CMRR_{V_{XY}} \times \left(\beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right) - \beta_4\right)(R_{ext} + r_x) + \beta_3\beta_4\alpha_2)}{\beta_3(\beta_8 - \beta_9)(R_{ext} + r_x)} \quad (34)$$

Finally using Eq. (27) and (31), current CMRR between Z and X terminals can be simplified to Eq. (35).

$$CMRR_{I_{ZX}} = \frac{Ai_{ZXdiff}}{Ai_{ZXcom}} = \frac{\left(\beta_7\left(\left(CMRR_{V_{XY}} \times \beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right) - \beta_4\right)(R_{ext} + r_x) + \beta_3\beta_4\alpha_2\right) \times \left(\beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right)}{\left(CMRR_{V_{XY}} \times \beta_6 - \frac{\beta_5\beta_7}{\beta_1}\right) \times \beta_3(\beta_8 - \beta_9) \times (R_{ext} + r_x)} \quad (35)$$

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