A Current Source Model for CMOS Logic Cells Considering Multiple Input Switching and Stack Effect

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Abstract

This paper presents a current source model (CSM) of a CMOS logic cell, which captures simultaneous switching of multiple inputs while accounting for the effect of internal node voltages of the logic cell. Characterization procedures for various components of the proposed CSM are described and application of the model to output waveform computation is discussed. Experimental results to assess the accuracy and efficiency of the proposed multiple input switching CSM in the context of noise and timing analyses in VLSI circuits are reported.

1. Introduction

The down scaling of layout geometries to 65nm and below has resulted in a significant increase in the packing density and the operational frequency of VLSI circuits. An unfortunate side effect of this technology advancement has been the aggravation of noise effects, such as the capacitive crosstalk noise. The conventional static timing analysis (STA) techniques model signal transitions as saturated ramps with known arrival and transition times and propagate these timing parameters from the circuit primary inputs to the primary outputs. However the different waveforms with identical arrival time and slew (transition) time applied to the input of a logic cell or an interconnect line can result in very different propagation delays through the component depending on the exact form of the applied signal waveform [1]. Therefore the shape of the voltage waveforms should be considered in order to ensure accurate timing and noise analysis results in sub-90nm CMOS designs.

In the ASIC design flow, combinational and sequential logic cells are pre-characterized for the input-to-output propagation delay and output slew as a function of the input slew and effective output capacitance (C_{eff}). This characterization is based on an implicit assumption about the saturated ramp form of the voltage waveforms that drive the inputs of a logic cell or are produced at its output. We shall refer to this modeling technique as the voltage-based method throughout this paper. Voltage-based approach is inherently incompatible with the arbitrary shapes of voltage waveforms, and thus, falls short when dealing with noisy inputs such as crosstalk-induced noisy waveforms. A current source (CS) model is load independent and can handle any electrical waveform at internal signal lines of the circuit; therefore, it overcomes the above-mentioned shortcomings of the voltage-based models.

The authors of [2] were among the first to present a real CS model (CSM) of a CMOS logic cell (called Blade) in which a pre-characterized current source is utilized to capture the non-linear behavior of the cell with respect to the input and output voltage values. Keller et al. [3] presented a CSM for the purpose of crosstalk noise analysis. Similar to Blade, a pre-characterized current source is used. The parasitic components, namely the Miller and the output capacitances are assumed to be constant regardless of the input and output voltage values. In practice, these capacitive effects can vary by orders of magnitude depending on cell input and output voltage values. In [4] this weakness is resolved by introducing a nonlinear output capacitance model. The authors of [5] used nonlinear input, output, and Miller capacitors along with an output current source, all of which are functions of the input and output voltages.

Errors as high as 100% may be produced in gate delay and output slew estimates during timing analysis if the multiple input switching (MIS) effect is not modeled. If inputs of a logic cell such as a NAND2 gate arrive simultaneously, then the cell delay is significantly different from the case where one of the inputs has been stable at a non-controlling value for a while before the other input arrives. Most STA tools utilize the single input switching (SIS) cell delay/slew models even if the timing windows for the input signal anticipate a MIS event. This can result in a significant under-estimation of cell delay/slew and makes the delay analysis optimistic [6]. In [7] the authors present an extension to CSM to

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handle the MIS case. In their model, each input and output pin of the cell is modeled with a voltage-dependent current source and a nonlinear capacitor. Each circuit element is made dependent on all the input voltage values and the output voltage. However the effect of the internal node voltages is completely ignored (see below). This simple model can result in 20% or higher delay estimation error in some cases. Therefore in this paper we present a complete CSM model which is not only capable of handling simultaneous input switching but also accurately captures the effect of internal node voltages.

The remainder of this paper is organized as follows. In Section 2 we provide the background and motivation for the problem. Section 3 presents our MCSM (Multiple Input Switching Current Source Modeling). While Section 4 is dedicated to simulation results, Section 5 concludes the paper.

2. Background and Motivation

2.1 Single Input Switching CSM

We first review a CS model for single input switching (SIS) of combinational logic cells similar to the one in [5]. This will give us to a better appreciation of the model for multiple inputs switching, which will be presented in the next section.

Various CSMs for SIS are essentially similar in the sense that they all model the output current of the logic cell with a voltage-dependent current source. A DC analysis step is performed to pre-characterize this current source as a function of the input and output voltages of the cell. The difference between the existing SIS CSMs is mainly on how they capture the model capacitances.

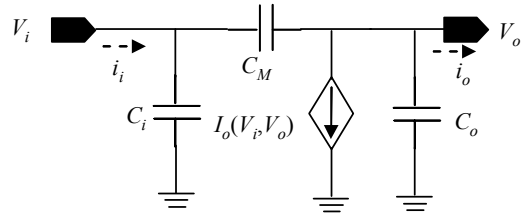

Fig. 1. A SIS CSM for combinational logic cell

The CS model for a SIS combinational logic cell, depicted in Fig 1., comprises of three nonlinear capacitances, namely, input and output parasitic capacitances, C_i and C_o, to capture the capacitive loading at input and output nodes of the cell and a Miller capacitance, C_M, to capture the capacitive coupling effect between the input and output nodes. The model also includes a nonlinear current source, I_o, at the output. Each component is a function of the input and output voltage values. The current source is characterized with DC analysis on the output, while the output and Miller capacitances are characterized by using transient analysis on the input and output.

2.2 Multiple Input Switching and Stack Effect

It is demonstrated that a CS model which considers only the input and output nodes is not able to characterize a multiple input switching logic cell accurately.

For the sake of presentation and without loss of generality, in the remainder of this section, we limit the discussion to a NOR2 gate whose transistor level diagram is shown in Fig. 2. The key concepts and analyses for other types of logic cells with two or more inputs are similar.

In a NOR2 gate, when the inputs are set to '00' and the output node becomes '1', not only the load capacitance C_L will be charged to V_{dd}, but also the capacitance of the internal node N, i.e., C_N, will be fully charged from its initial voltage V_N to V_{dd}. Clearly, a higher initial value of V_N necessitates less output current to charge up this internal node, and therefore, the transition of the output to '1' becomes faster. The exact value of V_N depends on the previous state of the inputs (we ignore the effect of leakage currents here).

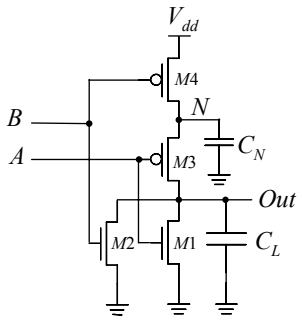

Fig. 2. Transistor level diagram of a NOR2 gate.

Consider two different "input history" cases. In the first case, the inputs of the NOR change from '10' (A='1', B='0') to '11' and then to '00'. In this case, in input state '10', node N is connected to the supply voltage, and therefore, its voltage is V_{dd} ; when input B changes to '1', node N floats and some current is injected into it through the gate-drain capacitance of M4 and thus, the voltage of N increases by ΔV_1. Therefore, right before the '00' transition at the inputs, the voltage of N is $V_{dd}+\Delta V_1$. In the second case, the inputs of the NOR2 gate start from '01', change to'11' and finally settle at '00'. In input state '01', the voltage of N is (body-affected) $|V_{t,p}|$. When input A changes to '1', again node N floats and some charge is injected into it through the Miller capacitance of M3 which causes the voltage of N to rise to $|V_{t,p}|+\Delta V_2$. Fig. 3 presents the SPICE waveforms for the voltage of the internal node under these two scenarios, which confirms our analysis.

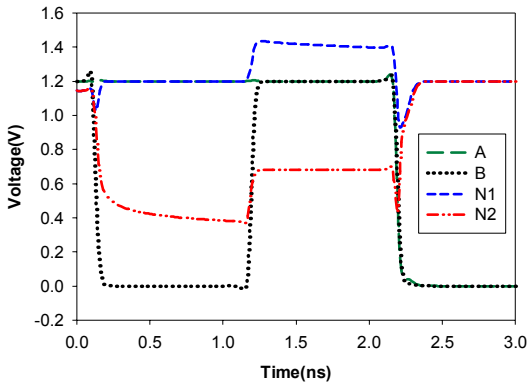

Fig. 3. Voltage waveforms of the internal node of NOR2 gate for two different input patterns.

From the above discussion, one expects that the 50% propagation delay of the '11' to '00' input transition to be less in the first case (which results in the output waveform denoted by Out1) compared to the second case (i.e., whose output waveform is denoted by Out2). SPICE results reported in Fig. 4 confirm this expectation. The delay difference between the two cases for the same input-transition pattern (i.e., from '11' to '00') is reported in Fig. 5 under different output loads. From this figure one can see there is a significant difference between these two cases. We call the aforementioned effect the internal node voltage, the stack effect, or the history effect. MIS CSMs that ignore the internal node effect produce inaccurate timing, especially for lightly loaded logic cells.

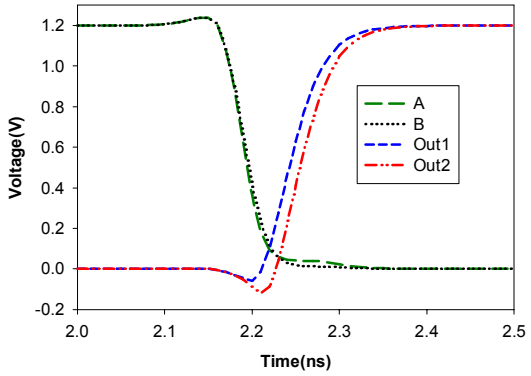

Fig. 4. Output voltage waveforms of NOR2 gate for the '11' to '00' input transition under two different input histories.

3. Multiple Input Switching CSM

This section explains components of the CS model of a combinational logic cell when multiple inputs are switching simultaneously. For the sake of simplicity, we consider that no more than two inputs are switching at the same time. More precisely, even when the logic cell has more than two inputs, we model the cell based on a maximum of two varying inputs (all other inputs are set

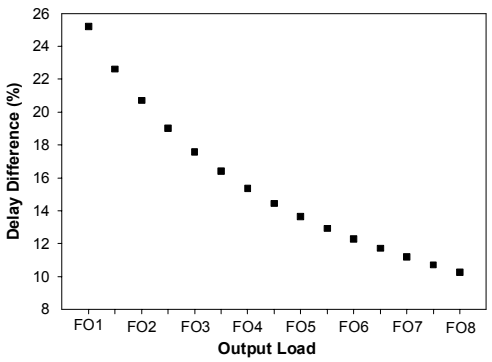

Fig. 5. Difference between the low-to-high propagation delays for the '11' to '00' input transitions under two different initial voltages for the internal node of NOR2 gate.

to their non-controlling values). This is a modeling decision that restricts a timing analysis tool, and can adversely affect accuracy of the delay estimates, but is important for managing the model complexity.

3.1 Baseline Model Neglecting the Internal Node Voltages

A simple CS model which extends the model of [5] to handle the MIS case is depicted in Fig. 6(b). Notice that unlike [7], the baseline MIS CS model accounts for the Miller capacitances, which are quite important especially when the input slew rate is high.

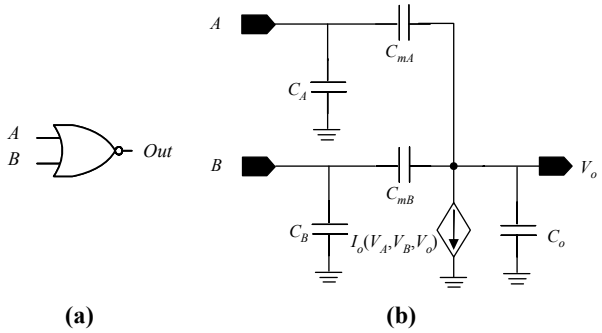

Fig. 6. A simple MIS CSM for NOR2 gate which does not capture the internal node effect.

The major shortcoming of this baseline model is the absence of an initial voltage value and stored charge on internal node capacitances (e.g., node *N* in the transistor-level schematics of the NOR2 gate in Fig. 2).

3.2 Complete Model Considering the Internal Node Voltages

In the following subsections we describe how to model the initial internal node voltages and consider their effect on the output voltage calculation.

The modeling of the internal node is based on the following observation. The voltage value at node *Out* in Fig. 7(a) is a function of the voltage value at node *N*.

Moreover, $V(N)$ itself is dependent on voltage values of nodes A, B, and Out as well as the circuit parameters.

Node N is considered as both an input and an output. To calculate $V(N)$, we model the circuit at node N by a voltage dependent current source and a voltage dependent capacitance, cf. Fig. 7(b). For simplicity we do not model the Miller effect between node N and other nodes. From our simulation results, this simplification does not introduce much error.

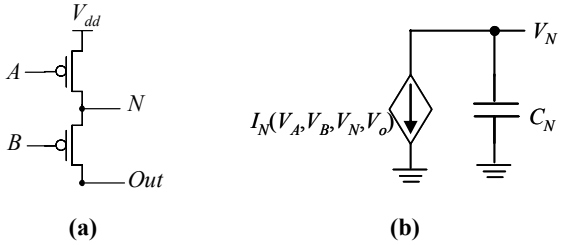

Fig. 7. Modeling the internal node of a NOR2 gate.

3.3 MCSM: Characterization

This subsection explains how to characterize dependent current sources and various capacitances of the proposed MIS CSM.

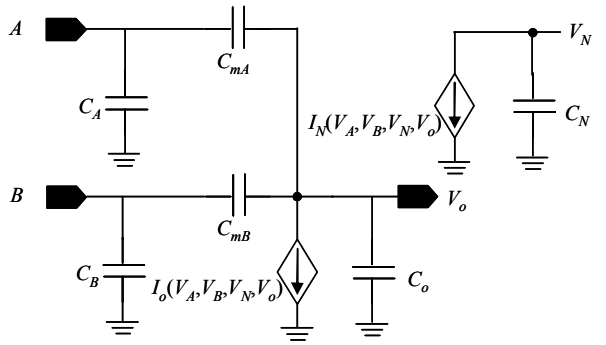

Fig. 8. Complete MIS CSM of a NOR2 gate.

As shown in Fig. 7, the proposed MCSM model consists of six nonlinear capacitive components, namely, input and output parasitic capacitances to model the parasitic loading at input and output nodes of the logic cell, Miller capacitances to model the capacitive coupling between the input nodes and the output node, and the internal node capacitance. The model also has two nonlinear current sources, one at the output node and one at the internal node. Each of these components is a function of the voltage values at the input, output and internal nodes. As a result, the cell model is represented by the following two KCL equations, which essentially account for the currents at the output pin and at the internal node of the cell during the switching.

$$i_o + I_o(\mathbf{V}) + \{C_o(\mathbf{V}) + C_{mA}(\mathbf{V}) + C_{mB}(\mathbf{V})\}\frac{\partial V_o}{\partial t} - C_{mA}(\mathbf{V})\frac{\partial V_A}{\partial t} - C_{mB}(\mathbf{V})\frac{\partial V_B}{\partial t} = 0 \quad (1)$$

$$I_N(\mathbf{V}) + C_N(\mathbf{V})\frac{\partial V_N}{\partial t} = 0 \quad (2)$$

In the above equations, $\mathbf{V} = (V_A, V_B, V_N, V_o)$ represents a four-dimensional vector of node voltages. The Miller capacitances C_{mA}, C_{mB}, the output capacitance C_o, and the internal node capacitance C_N values are characterized through a series of SPICE-based transient simulations, in which saturated ramp input and output voltages are applied to input and/or output and internal nodes while the output current is monitored. Four-dimensional lookup tables are used to store C_{mA}, C_{mB}, C_o and C_N values because these capacitances vary as a function of the input and output voltages of the model which in turn change with time during input/output transitions. During the characterization step, different slopes for the ramp input waveforms are used and the capacitance values are calculated for each input slope, and finally, an average value for the parasitic capacitances is stored. Based on our experiments, changing the slope of the ramp voltage waveform in the characterization step has a very small effect on the pre-characterized capacitance values.

The values of current sources I_o and I_N, in response to DC voltage levels on the inputs, output, and internal node are also determined for each logic cell. These voltage sources are swept from $-\Delta v$ to $V_{dd}+\Delta v$ where Δv is a safety margin for the cases where the voltage reaches a value above (below) V_{dd} (zero). The current at output and internal node are measured in SPICE and I_o and I_N current sources are characterized for different $\mathbf{V} = (V_A, V_B, V_N, V_o)$ values. As a result, to model the nonlinear behavior of a logic cell with respect to the input, output, internal node voltage values, a 4-D lookup table is created to store the values of $I_o(\mathbf{V})$ and $I_N(\mathbf{V})$.

Precise estimation of the output load is critical for accurate output voltage calculation of a cell. The output node of a cell is usually connected to several fan-out cells directly or indirectly through an interconnect line. The input parasitic capacitances of fan-out cells should be thus considered as part of the load when calculating the output voltage of the driver cell. The following equation is used to characterize the parasitic capacitance seen at input A of a cell.

$$i_A = \{C_A(\mathbf{V}) + C_{mA}(\mathbf{V})\}\frac{\partial V_A}{\partial t} - C_{mA}(\mathbf{V})\frac{\partial V_o}{\partial t} \quad (3)$$

A similar formula can be used for node B.

A SPICE-based transient analysis is used to determine C_A and C_B. In this analysis, a saturated ramp is applied to the one input while the output node is connected to a DC

voltage source, and the input current, is measured. Although the input parasitic capacitances, C_A and C_B, are in fact functions of the input and output voltage values, in practice, an input-voltage-dependent C_A and C_B, are all that can be efficiently utilized. This is because when calculating the output voltage waveform of a logic cell, the output voltage values of its fanout cells are unknown, and therefore, calculation of C_A and C_B values of the fanout cells cannot make use of any information about the output voltage levels of these fan-out cells. That is why we say that making C_A and C_B dependent on V_o is not useful in practice.

3.4 MCSM: Utilization

The logic cell characterization steps of the model are load-independent, because the model components are characterized as a function of the input, output and internal node voltage values rather than the input slew and output effective capacitance. Therefore the output voltage waveform can be constructed for a given input voltage waveform in the presence of an arbitrary load. Note that the current drawn by the load can always be written as a function of the output voltage of the logic cell and the load components. Using this current component for the load, a KCL equation at the cell output node can be written, which is a function of the cell output and input voltages, the pre-characterized cell components, and the load electrical parameters. For simplicity, in the remainder of this section, we show the KCL equation for a simple capacitive load C_L (i.e., the current component for the load is simply $C_L \partial V_o/\partial t$). The KCL at the output node can be written with respect to output voltage values, resulting in:

$$V_o(t_{k+1}) = V_o(t_k) + \frac{C_{mA}\times(V_A(t_{k+1}) - V_A(t_k)) + C_{mB}\times(V_B(t_{k+1}) - V_B(t_k)) - I_o(\vec{V})\Delta t}{C_L + C_O + C_{mA} + C_{mB}} \quad (4)$$

The internal node voltage value V_N is calculated as follows:

$$V_N(t_{k+1}) = V_N(t_k) - \frac{I_N(\mathbf{V})\Delta t}{C_N} \quad (5)$$

The internal node effect is smaller when the fanout load is significantly larger than the diffusion capacitances of the driver cell. This is due to the fact that whether or not some additional output current is needed to charge the internal capacitances becomes less significant when the output current is large.

The complete MCSM can be used selectively for different logic cells based on the output load. Using this selective modeling, one can use the simple MCSM of Fig. 6(b) for the logic cells that drive a relatively large load. Otherwise, the complete MCSM of Fig. 7 should be used.

4. Simulation Results

To study the accuracy of the proposed model, we performed extensive simulations and compared our MCSM with HSPICE [8]. A 130nm cell library with the supply voltage of 1.2V has been used in these simulations. The set of experiments involved common logic cells, i.e., inverter, NAND and NOR cells.

In the first experiment, we compared the efficiency of MCSM in modeling the delay of a NOR2 gate for the fast and slow transitions described in Section 2.2. The result of this simulation is shown in Fig. 9. From this figure one can see that MCSM captures the effect of internal node and accurately models the delay. The maximum error of MCSM for these two cases is 4%, while using a MIS CSM which neglects the internal node voltages (as described in Section 3.1) results in 22% error.

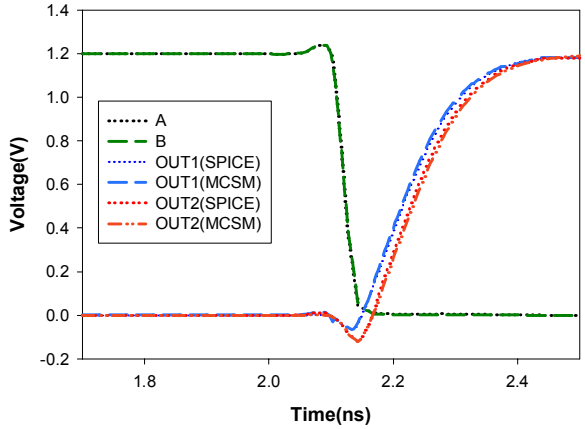

Fig. 9. MCSM waveforms compared to HSPICE simulations for fast and slow cases.

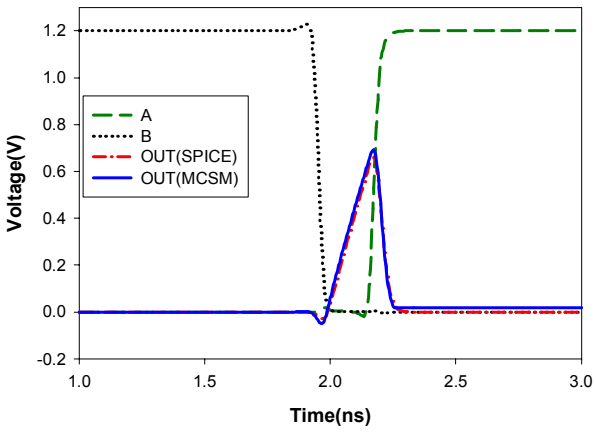

Fig. 10. Using MCSM to accurately model glitches.

Fig. 10 compares the results of HSPICE and the proposed model when a glitch occurs at output of a NOR2 cell. As shown in the figure, the MCSM completely models the logic cell and the generated

waveforms by MCSM for output nodes follow the HSPICE waveforms closely.

Fig. 11 compares the results of HSPICE and MCSM for MIS on a NOR2 gate. The output voltage waveform predicted by SIS CSM presented in [5] is also shown for comparison. From this figure one can see that MCSM accurately models the output voltage waveform, while using a SIS CSM results in significant error.

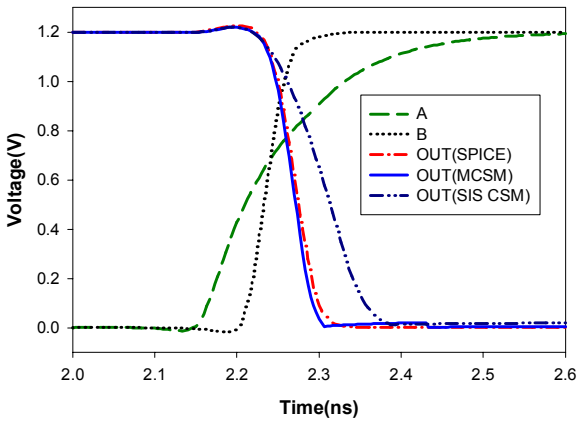

Fig. 11. MCSM waveform compared to HSPICE simulations and SIS CSM presented in [5].

The shape of the waveform greatly impacts the accuracy of timing analysis; therefore, delay and output slew metrics may not be sufficient to construct shape of the waveform. Our model is able to compute close-to-SPICE output waveforms in terms of their actual shape. We use the Root Mean Squared Error (RMSE) as a metric to compare waveform similarities. RMSE is defined as:

$$RMSE = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(V_{SPICE}(t_k) - V_{MSCSM}(t_k)\right)^2} \qquad (6)$$

where V_{SPICE} and V_{MCSM} are the voltage values of the output of the logic cell at a given time. For each experiment, k=1 represents t_1 which is the time at which the noisy input starts to change whereas k=N represents t_N when output node reach their stable final values (either high or low). We finally normalize *RMSE* to V_{dd} to take out the effect of V_{dd} scaling. To generate different noisy waveforms for this experiment, the noise injection time is swept for a time period 1ns with a step size of 10ps. Input line *A* of the NOR2 gate is coupled to an aggressor line through a 50fF coupling capacitance. Both the victim and aggressor lines are driven by minimum sized inverters. The NOR2 gate under consideration has a FO2 load. The arrival time of the signal transition at the input of the victim line driver is set to 2.2ns while that of the aggressor driver (i.e., the noise injection time) is swept from 2ns to 3ns with a time step of 10ps. Fig. 12 shows the 50% delay error when output waveforms are compared for the MCSM and SPICE for the period of noise injection. The average RMSE is 1.4% of V_{dd}, which confirms that our voltage waveform closely matches that produced by SPICE.

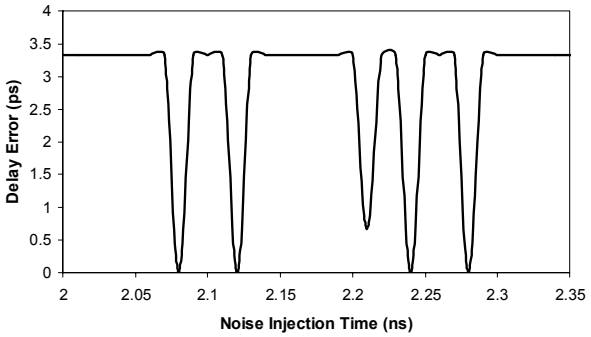

Fig. 12. Delay error vs. noise injection time.

5. Conclusion

In this paper we presented an accurate current source model (CSM) for multiple switching CMOS logic cells which effectively captures the internal node voltage effect. This model, which is called MCSM, is especially useful for delay and noise analysis of lightly loaded cells. We showed because of neglecting the effect of internal node voltages, previous multiple input switching current source models (MIS CSM) may result in significant error in delay calculation, especially for lightly loaded cells. We showed that the accuracy of our proposed technique is comparable with HSPICE. More precisely, it has been demonstrated that the maximum delay error of our model, which captures the internal node voltage effect, is 4% while that of a CSM without this capability is about 22%.

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