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A DC to 3-Phase Series-Resonant Converter with Low Harmonic Distortion

H. HUISMAN AND S. W. H. DE HAAN

Abstract—A type of dc to 3-phase series-resonant converter (s.r.-converter) for potentially submegawatt industrial applications is presented. The converter provides variable-frequency sine-wave currents, with low harmonic distortion at the output terminals, and with the frequency ranging from -200 through dc to +200 Hz. The converter can transfer power in both forward and reverse power-flow directions to almost any type of load circuit. The methods of control are formulated such that they can be implemented easily with high-speed logical circuits. Test results for a 1-kW demonstration converter are supplied.

I. INTRODUCTION

DURING the last decade the interest in electrical wind-energy conversion has increased significantly. This attention concerns both the generation of autonomous multiphase ac grids, as well as the delivery of power to existing utility grids. To carry out the electrical conversion process, one often uses a cycloconverter or a cascaded ac-dc and dc-ac converter. The dc to 3-phase converter presented in this paper is considered as an intermediate step in the development of a novel type of 3-phase-to 3-phase cycloconverter. Apart from wind-energy conversion this converter can be applied to other areas of technology including power generation and variable frequency-machine driving.

Fundamentals of dc to 3-phase ac power conversion have been known for many decades. Because of the simplicity of control and the clarity of insight into the method of operation, some of these systems, such as the load-commutated bridge inverter, the square-wave inverter, and the high-frequency pulsewidth-modulated inverter, are well developed [1] and widely spread. The advantages of these systems are, however, countered by one or more of the following disadvantages:

- 1) the stress on electronic switches is high due to forced commutation techniques,
- 2) heavy and costly filters are required to remove the low-frequency harmonic content of the electrical waveforms, and
- 3) the power factor is poor and cannot be controlled freely. The s.r. dc to 3-phase ac converter presented, which is based on a concept presented by Schwarz [2], does not possess these disadvantages. Moreover, the system has the common features of series-resonant converters (s.r.-converters) such as, 1) the system is inherently short-circuit proof, 2) the size of the system is small due to the high internal frequency, and 3) the system is capable of controlling and turning off power by a frac-

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The authors are with the Delft University of Technology, Mekelweg 4, 2624, CD Delft, The Netherlands.

tion of a millisecond. The technology of the single-quadrant

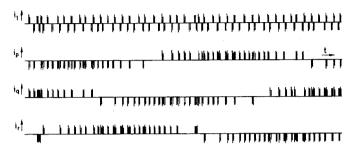


Fig. 1. Example of the distribution of the current pulses in the resonant current i_l over the line currents i_p , i_q , and i_r .

dc-dc s.r.-converter has been well established by now and many authors have discussed the subject [3]-[6].

Since the beginning of the eighties attempts have been made to break through to the development of ac and multiphase s.r.-converters. Some successful experiments of ac-dc s.r.-converters were reported by Schwarz [7], [8]. Recently, a single-phase dc-ac converter has been presented [9]. The 3ϕ -dc (3-phase to dc) s.r.-converters described up to now [7], [8] do, however, extract currents from the power grid which are similar to the currents which are extracted by a 3-phase diode rectifier. These square-wave-like currents cause harmonics in the supply lines, while the power factor is theoretically limited to 0.955 [8].

From a fundamental point of view, the s.r.-converter is capable of dealing with multiphase ac power in a more sophisticated way [2]. A s.r.-converter can be considered as a network which generates an array of current pulses at a high frequency (5-50 kHz). By properly distributing the pulses from this highfrequency carrier over the 3 lines of the grid, it is possible to generate current waveforms, which do contain one single frequency in the low-frequency range (<3 kHz). The principle of the process is illustrated in Fig. 1, where resonant current pulses are represented by impulses. Fig. 1 is obtained from a simulation program, which operates similarly to the one described in [10]. The high-frequency content of the output current is removed by a relatively small filter, with the result being a low-frequency phase current with low harmonic distortion. The pulse distribution process can be applied both to 3ϕ -dc converters as well as to dc- 3ϕ converters.

In this paper a dc- 3ϕ converter is described which is based on the above principle. The converter is capable of generating a 3-phase output waveform with frequencies ranging from ca +200 via 0 to -200 Hz (phase reversal). Moreover, the converter can be connected to leading as well as lagging loads ($+180^{\circ}$ to -180°), both linear and nonlinear, in both the forward and

reverse power-flow directions. The critical points that can be identified in the system design of the dc-3 ϕ converter are: 1) the pulse-distribution algorithm (line selection), 2) the algorithm for the selection of particular switches in the selected lines (switch selection, and 3) the method of control to guarantee thyristor turnoff and continued oscillation (V_c -control). The method of control is in accordance with a control mode, which is described in a companion paper [11]. The theory is verified on a small-scale (1 kW) demonstration converter.

II. PROPERTIES OF THE GENERALIZED DC-DC S.R.-CONVERTER

The operation modes of the $dc-3\phi$ s.r.-converter is based on the principles of the dc-dc s.r.-converter, which is treated in literature [3]-[6], [11], [12]. To enable greater insight, some properties of the dc-dc s.r.-converter will be reconsidered in a nonorthodox manner. Fig. 2 shows the basic, generalized dc-dc s.r.-converter. The input switch matrix consisting of switches Q_A and Q_B connects the resonant circuit to $+E_s$ or $-E_s$, where E_s is the dc source voltage. The output matrix consisting of switches Q_C and Q_D connects the resonant circuit to $+V_o$ or $-V_o$. By appropriate control of the switch matrices a bipolar voltage, compounded of square waves, is generated across the resonant circuit, thus inducing a resonant current of the well-known shape (Fig. 3(a)). In this paper the resonant current is considered as a series of current pulses. The time of initiation of the Kth current pulse is denoted by β_k , where β is the normalized time defined by $\beta = t/\sqrt{L_1 C_1}$.

The current gap which is not present in most dc-dc converters is a prerequisite in ac-converters for the purpose of commutation and control [11]. Depending on the application, the switches are implemented as single diodes or as combinations of diodes and/or controllable switches such as thyristors and MOSFET's. In multiphase converters all symbolical switches should be implemented as thyristors. Although the multiphase converter does not contain diodes, we will stick to the term "diode current" for each first current segment following a current zero crossing; the second current segment will be designated as "thyristor current". The Kth event between the time β_k and β_{k+1} will also be referred to as the Kth converter cycle.

It is well known that a number of switching modes can be distinguished for the generalized s.r. dc-dc converter [4], [11]. It will be shown that all switching modes have the following properties in common:

- 1) the diode current is (at least) opposed by the highest terminal voltage (this follows from the commutation condition),
- the thyristor current at the high-voltage side extracts power from that source (this follows from the power balance), and
- 3) both diode and thyristor currents on the low-voltage side transfer power in the desired direction.

Conversely, one may state that if the above rules are obeyed, one can transfer power in any desired direction in any combination of input and output voltages.

The statements are based on the following considerations.

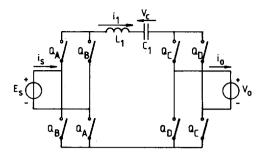


Fig. 2. Basic schematic and the definition of the voltages and currents in a generalized s.r. dc-dc converter.

Suppose that in the symbolic converter from Fig. 2, the source voltage E_s and the output voltage V_o are both allowed to be positive or negative. In either an input or an output line the current will be prescribed by some reference. The desired power direction is defined by the sign of this reference current and the sign of the actual voltage at the associated port. As stated before, a resonant current phase consists of a diode current and a thyristor current. Q_D and Q_T are defined as the charge transferred by the diode and the thyristor current, respectively. Both Q_D and Q_T are defined such that they are always positive. The input and output matrices facilitate Q_D and Q_T being routed in any desirable direction on input and output terminals.

If one bears in mind that the energy transferred by a current in a certain interval is equal to the product of voltage and transferred charge, it follows from considering the energy balance applied to the input and output port of the converter (Fig. 2)

$$E_s(Q_D S_{11} + Q_T S_{12}) = V_o(Q_D S_{21} + Q_T S_{22}). \tag{1}$$

Here S_{11} to S_{22} indicate in which direction the charge flows on input and output, so S_{ij} is either +1 or -1. Note that (1) is valid under nonsteady-state conditions, provided that $v_{cp}(k) = v_{cp}(k+1)$ and that both E_s and V_o are constant during the cycle considered.

From (1) it follows that

$$-\frac{Q_D}{Q_T} = \frac{S_{12}E_s - S_{22}V_o}{S_{11}E_s - S_{21}V_o}$$
 (2)

Because both Q_D and Q_T are positive, the sign of the left-hand term is negative. To satisfy (2), the coefficients S_{i1} and S_{i2} of the highest voltage, either E_s or V_o , should be opposite in sign. On the low-voltage side both S_{ii} and S_{i2} are unconstrained, so that they are chosen such that the power is transferred in the desired direction. For a proper commutation from the diode to the thyristor current the diode current is required to be opposed by the highest voltage. By way of example Fig. 3(b) shows the resulting current waveforms of i_s and i_o , if $E_s > 0$, $V_o > 0$, $|E_s| < |V_o|$ and $i_{oref} < 0$.

The elaboration of the switch selection mechanism in the $dc-3\phi$ converter presented is primarily based on the previous discussion. The basic diagram of the power network of the converter is depicted in Fig. 4. The switches symbolize appropriate electronic switches such as antiparallel thyristors.

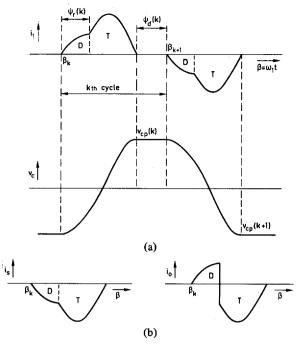


Fig. 3. (a) Resonant current waveform for converters with a current gap. (b) Example of source and load currents in a converter when $E_s > 0$, $V_o > 0$, $|E_s| < |V_o|$ and $i_{oref} < 0$.

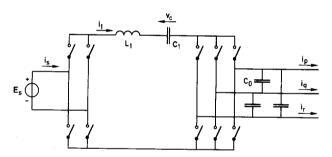


Fig. 4. Basic schematic of the power network of a dc-3 ϕ s.r.-converter.

In essence, the multiphase-converter operation is based on a selection mechanism which, for any converter cycle, selects two out of three output lines to carry currents. The particular implementation of this line-selection mechanism will be discussed later. For our present considerations it is important to note that once one of the three output lines has been excluded from current flow, during this particular converter cycle, the converter can be treated as a generalized dc-dc converter.

A. Basic Requirements

Prior to describing the control and selection mechanisms, we formulate requirements which the ac-converter has to meet. The converter should be able to inject currents in any arbitrary active or passive output circuit. These currents will often be sinusoidal of shape. The size and shape of the voltages at the output terminals depend on the character of the load and the shape of the injected currents. The amplitudes of the output voltages are allowed to be greater as well as smaller than the source voltage. For that reason the converter should be able to transfer power to a lower as well as to a higher terminal voltage. Moreover, because the load may require reactive

power, the instantaneous power should be allowed to flow in both directions. The output capacitors of the converter are sufficiently large to justify the assumption that the output voltage is constant during a converter cycle, although the output voltage is essentially a low frequency ac-voltage. One should bear in mind that the output capacitors are intended to remove the high-frequency content (order 10 kHz) from the output waveform.

Concluding, it is evident that during each converter cycle the multiphase converter should be able to operate as a generalized dc-dc converter.

B. The Principal Functions and Block Diagram

To operate as a dc-dc converter during a converter cycle, it is necessary to select for each converter cycle two lines on the ac side. Two out of M lines have to be selected for an M-phase converter. This line-selection process and the associated pulse-distribution process is controlled by the actual measured output currents $i_m(m=p,q,r)$ and by the references for the output current i_{mref} . The selection circuit, which is of the integral-pulse-controller type [11], [13], [14] is symbolically indicated in the lower left of the block diagram in Fig. 5. The line-selection block also generates a signal p whenever a current pulse should be initiated to bring one of the output waveforms in accordance with the reference.

After two grid lines have been selected, it is the known by measurements, to which actual input and output voltage the dc-converter will be connected. The appropriate information is passed via a multiplexer to the switch-selection logic. The switch-selection logic, in the middle of Fig. 5, determines from the signs of the passed signal and from the state of the converter (diode cycle, thyristor cycle, or gap) which switches have to be closed during the following converter subcycle. Four out of 20 switches have to be selected. This information is passed to the latched thyristor pulse generators whenever a p-signal is issued during a current gap or when a cs (change state) signal is issued by the so-called V_c -peak predictor.

Essentially, the p-signal initiates the turnover from the current gap to the diode current, while the cs-signal initiates the turnover from the diode current to the thyristor current.

The v_{cp} -predictor generates a cs-signal whenever this circuit predicts that the resonant capacitor voltage will be at a specified reference level at the end of the converter cycle.

C. Switch-Mode Selection

Once a pair of terminals has been selected, an appropriate and unique set of switches can be designated.

Explicitly, the switch-selection process for the diode and the thyristor cycle, respectively, will be explained with reference to Fig. 2.

1) Diode Cycle: Based on the sign of the capacitor voltage v_c at time β_k , it is known in which direction the resonant current will flow during the following converter cycle. As stated before, the diode current should at least be opposed by the highest terminal voltage $(E_s \text{ or } V_o)$. So, if one measures E_s , V_o , and v_c , one can straightforwardly designate two switches on the "high-voltage side" which have to be closed. On the low-voltage side, the direction of the current is such that the

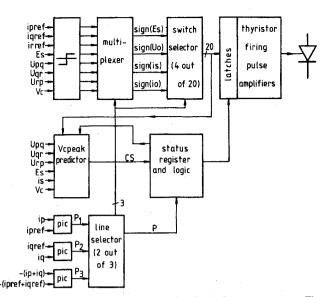


Fig. 5. Block diagram of the controller for the dc-3 ϕ s.r.-converter. The PIC and the V_{cp} -predictor do process analog signals. All other circuits process booleans.

desired power transfer direction, defined by $I_{oref} \cdot U_o$, is satisfied.

So, if $|V_o| < |E_s|$ then sign $(i_o) = \text{sign } (i_{oref})$ and sign $(i_s) = -\text{sign } (E_s)$ (3)

and if

$$|V_o| > |E_s|$$

 $|V_{\alpha}| > |E_{\alpha}|$

then sign $(i_o) = \text{sign}(V_o)$

and sign
$$(i_s) = \frac{\operatorname{sign}(i_{oref}V_o)}{\operatorname{sign}(E_s)}$$
 (4)

If the directions of i_s and i_o are known, and if the direction of i_1 is known, a unique set of four appropriate thyristors can be designated. Note that sign (i_1) in the Kth cycle follows from sign $(v_c(\beta_k))$.

2) Thyristor Cycle: The current direction on the low-voltage side occurs during the thyristor cycle such that the desired power-transfer direction is satisfied. On the high-voltage side the direction of the thyristor current is opposite to that of the diode current on that side.

So, if
$$|V_o| < |E_s|$$
 then sign $(i_o) = \text{sign } (i_{oref})$ and sign $(i_s) = \text{sign } (E_s)$ (5) and, if

then sign
$$(i_o) = -\text{sign}(V_o)$$

and sign
$$(i_s) = \frac{\text{sign } (i_{oref} V_o)}{\text{sign } (E_s)}$$
 (6)

If the signs of E_s , V_o , I_{oref} , and v_c are determined, the appropriate switches can be designated easily from (3) to (6).

D. Line Selection

In the following section it is assumed that a s.r.-converter should feed an M-phase network with ac power. For the purpose of driving machinery, it is suitable if the converter behaves like a multiphase current source, although for multiphase power generation a voltage-source character is more appropriate. The line-selection mechanism will be explained with respect to a current-source character. The multiphase converter should be controlled such that the current i_m in line m ($m = 1, 2, \dots, M$) is a replica of a reference current i_{mref} ($m = 1, \dots, M$). The reference current in lines $1, \dots, M - 1$ can be chosen freely; the reference current in line M follows from

$$\sum_{m=1}^{M} i_{m,ref} = 0. (7)$$

The current waveform synthesis is based on the concept of pulse-integral control [11], [12]. In a dc-dc converter the resonant current i_1 is measured, subsequently rectified and compared to a reference $i_{\rm ref}$. The error signal $(|i_1|-i_{\rm ref})$ is fed to an integrator. Whenever the integrator output e_c exceeds some threshold e_T , the power switches are actuated, thus generating another current pulse. When two successive threshold crossings are denoted by t_a and t_b , the following holds:

$$\int_{t_a}^{t_b} (i_o - i_{ref}) dt = 0.$$
 (8)

For dc and single-phase converters, t_a and t_b coincide with the beginning of two successive converter cycles.

For normal unipolar dc-dc s.r.-converters the implementation of the pulse-integral controller (PIC) for the output current i_o is relatively simple because $i_o = |i_1|$. In multiphase converters only two lines are served during a converter cycle. For that reason (8) is implemented such that the interval (t_a, t_b) effectively spans several cycles. This implies that during each cycle a limited error occurs for each line. Moreover, the implementation should be modified such that the PIC can handle both positive and negative values of i_1 and i_{ref} . Fig. 6(a) gives the implementation of one of the M-1 PIC's and Fig. 6(b) shows the associated waveforms. Whenever the integrator output e_c gets into one of the arced areas, a pulse-request signal P_m is generated.

The gap between the comparator levels is intended to prevent the immediate generation of a pulse request whenever the reference signal changes polarity. If $\Delta=0$, this undesirable side effect will occur. For optimal functioning the gap should

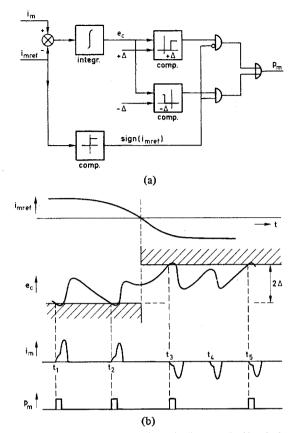


Fig. 6. Bipolar PIC for line m. (a) Schematic diagram. (b) Signals that may occur at the time that the reference signal i_{mref} is reversing polarity. Note that at time t_4 a pulse request that is issued by another line is served.

be slightly larger than the integrator swing during a current pulse, although this is not critical. Note that signal P only indicates that line m requests a current pulse. It does not indicate in which direction the current pulse should flow into the line.

All lines are equipped with individual PIC's and the pulse-request signals are logically OR'ed. When a pulse request is issued, the next converter cycle will be generated. The line that issues the request will take part in the oscillation and the current will flow in that line in the direction of the associated reference. Next a second line that will take part in the oscillation should be selected. Only those lines whose sign of the reference current is opposite the reference sign of the line that issues the pulse request are considered. If more than one line satisfies this requirement, a line is selected whose integrator output is closest to the associated threshold level. Note that the line selection process described above is based for a great part on two-state logic, which can be implemented easily with digital electronics.

After two lines on the ac side have been selected, the converter can further be considered as a generalized dc-dc converter. For this specific dc-dc converter, the voltage between the selected line will be designated as output voltage V_o , while the output current in the line that issued the pulse request will be denoted by i_o .

The further selection of switches is carried out as described in the preceding section.

During the servicing of a pulse-request, i.e., the generation

of a current pulse, the pulse-request signal will inherently be cleared due to the integrator action.

E. V_c -Control

One of the most critical points in multiphase converters is the choice of the firing-angle control module. This control module should be chosen such that thyristor turn-off conditions and uninterrupted converter operation are guaranteed.

In a companion paper [11], a control module has been presented which guarantees continuous oscillation, in particular under dynamic conditions and at abrupt changing source and load voltages as occurring in multiphase converters. This control module maintains the capacitor peak voltage at a predescribed level V_{cpref} , which should be at least twice the highest terminal voltage.

During the diode interval following β_k , the circuit continuously generates a real-time prediction of $v_{cp}(k)$ according to the following formula [11]:

$$v_{cp}(k) = U_1 - U_2 + \{(U_1 - U_2 - v_c(\beta))^2 + (Z_1 i_1)^2\}^{1/2}$$
(9)

where U_1 and U_2 correspond to either $+E_s$ or $-E_s$ and $+V_o$ or $-V_o$, depending on the current flow direction through the source and load in the interval considered. At a time β , the prediction would be valid if the circuit were to turn over from the diode to the thyristor cycle at that time. So whenever the predicted value crosses the reference value V_{cpref} , the turnover is actually initiated. The beginning of a converter cycle at time β_k is initiated by the logically OR'ed pulse request signals.

As discussed in [11], the control module provides a method of independent control of the average current and capacitor peak voltage. Note that the time between the termination of a thyristor cycle and the initiation of the next diode cycle should be larger than the thyristor turnoff time t_q . Protection circuitry is provided to delay the initiation of a diode cycle if a pulse-request signal is issued before the associated thyristors have turned off.

Because the charge which is transferred by the resonant circuit in a converter cycle is limited to $2 v_{cp}/C_1$, this does in fact signify that the converter inherently has a current limiting character.

III. VERIFICATION

The proposed algorithms and the associated electronics were tested on a 1-kW demonstration converter which had the following specifications (refer to Fig. 4):

source voltage	E_{s}	= 120 V dc
maximum inverter frequency	f_1	= 10 kHz
peak capacitor voltage	V_{cp}	= 350 V
maximum allowable output voltage	V_{oma}	x = 170 V
resonant capacitor	C_1	$= 1.11 \ \mu F$
resonant inductor	L_1	$= 146 \mu H$
input filter capacitor	C_s	$= 50 \mu\text{F}$
output filter capacitors	C_o	$= 50 \mu\text{F}$
power at full load	P_o	= 1 kW

The electronic switches are implemented with 10 pairs of antiparallel thyristors of the type SKT16F08DS.

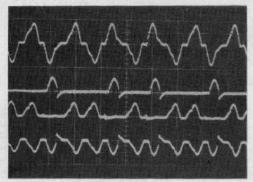


Fig. 7. Pulse-distribution process at a low output frequency. Upper trace: resonant current ca, 40 A/div. Lower traces: unfiltered line currents, 50 A/div, 100 μs/div.

The converter was primarily intended to demonstrate the most important features of the dc-3 ϕ s.r.-converter such as harmonic distortion, power factor regulation and load independence. Optimizing the performance with respect to efficiency and size was not a goal, although a maximum efficiency of 85 percent was established. The relatively high losses are due to the low source voltage in combination with the oversized power network.

Fig. 7 shows the resonant current and the unfiltered output currents at a relatively low line frequency. Note the difference in shape of the current pulse in the lines p and q, which is due to the fact that $V_{pr} < E_s$ while $V_{qr} > E_s$.

Fig. 8 gives an impression of the pulse-distribution mechanism. Simultaneously, it is shown that the capacitor peak voltage is maintained within 10 percent at a constant level.

The filtered and unfiltered currents in line p are shown in Fig. 9. The frequency of the reference current is approximately 60 Hz. From the frequency spectrum of Fig. 10(a) it can be concluded that the harmonic distortion of the filtered line current is extremely low. The 3rd, 5th, and 7th harmonics are at least 40 dB below the 100-Hz fundamental component. For comparative purposes, the harmonics of a line-commutated converter are indicated in the same graph. The difference is self-explanatory.

As stated in relation to (7), two reference currents can be chosen independently. For the purpose of examining the cross distortion between lines, a frequency spectrum (Fig. 10(b)) was recorded for a condition in which line p generated a 100-Hz sinoid, and line q a 130-Hz sinoidal current. The cross distortion is approximately -25 dB. Note that the 3rd, 5th, and 7th harmonics have disappeared from the graph. The "grass" at -60 dB between the harmonics is due to the more or less stochastic character of the unfiltered line current, which is rooted in the fact that the inverter cycle is not synchronized with the ac-cycle. From the last graph it may be concluded that the converter presented can be considered as a multiphase current amplifier. Any arbitrary current i_{ref} can be reproduced in the output line.

To investigate the ability of the converter to feed currents in nonlinear and active loads, two test circuits were set up. In the first circuit the converter was connected to an asynchronous machine. The converter was able to accelerate and decelerate the machine in both rotation directions. When the axis of the machine was connected to a mechanical drive, it was possible

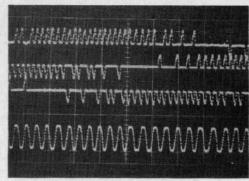


Fig. 8. Sinusoidal (200 Hz) modulated output currents. Upper traces: unfiltered line currents 50 A/div. Lower trace: resonant capacitor voltage ca, 700 V/div.

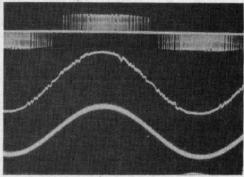


Fig. 9 Sinusoidal (60 Hz) modulated currents in line p. Upper trace: unfiltered current in line p, 50 A/div. Middle trace: filtered current in line p, 10 A/div. Lower trace: reference for line p, 2 ms/div.

to use the machine as a generator, thus transferring power to the dc "source" E_s . The reactive power for the machine was in both cases supplied by the converter.

In the second-setup the converter was connected via a transformer to the 3-phase utility grid. In order to test the ability of the converter to supply current independent of the actual output voltage, a 33 1/3-Hz 3ϕ reference was phase locked to the 50 Hz grid, forcing the converter to supply a 33 1/3-Hz current. The filtered output currents, shown in Fig. 11, arise from a superposition of the 33 1/3-Hz converter current and a 50-Hz current, which is caused by the connection of the converter filter capacitors to the grid.

IV. CONCLUSIONS

A dc- 3ϕ s.r.-converter is presented which has a combination of favorable properties compared to other types of multiphase converters.

These properties include:

low size and weight of the converter;

low harmonic distortion of the generated currents;

ability to generate low-frequency ac currents (up to several

hundreds of Hz) of any arbitrary shape;

ability to feed currents to almost any type of load including existing utility grids, machinery and passive loads;

potential ability to process hundreds of kW of power with an efficiency of more than 90 percent;

high speed of reaction;

inherently short-circuit proof; and

both forward and reverse power flows.

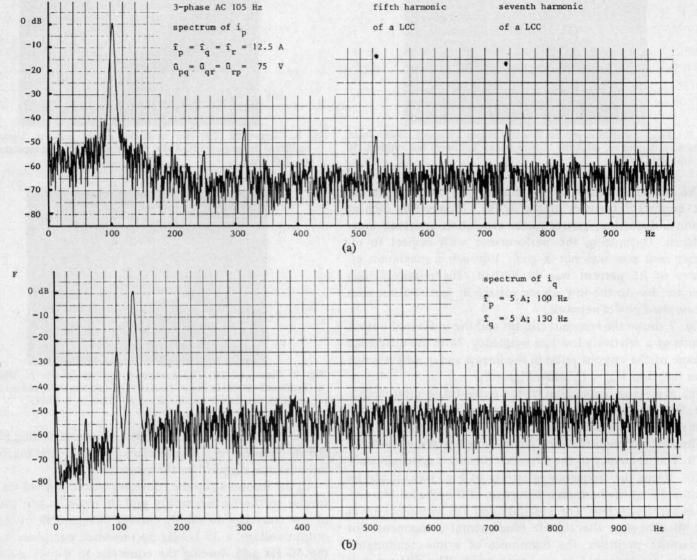


Fig. 10 Frequency spectra of the line currents. (a) Spectrum of i_p ; the reference for line p is a 100-Hz sinoid. (b) Spectrum of i_p ; the references for the lines p and q are 100- and 130-Hz sinoids, respectively.

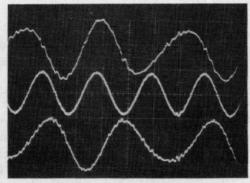


Fig. 11 Filtered load currents in lines p and q when the converter is connected to a 50-Hz 3-phase grid and while the current reference is set to 33 1/3 Hz. Upper trace: i_p , 10 A/div. Middle trace: V_{pq} , 100 V/div. Lower trace: i_q , 10 A/div; 10 ms/div.

The properties of the converter are rooted in combining a well-known s.r. power network topology with a novel method of preserving the energy content of the converter (v_{cp} -control), and of distributing current pulses over the output lines.

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