[7] C. S. G. Conroy, W. A. Lane, and M. A. Moran, "Statistical design techniques for D/A converters," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1118–1128, Aug. 1989.
[8] J. Bastos, M. Steyaert, and W. Sansen, "A high yield 12-bit 250-MS/s CMOS D/A converter," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 1996, pp. 431–434.
[9] C.-H. Lin and K. Bult, "A 10-b, 500-Msample/s CMOS DAC in 0.6 mm," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1948–1958, Dec. 1998.
[10] Y. Cong and R. L. Geiger, "Switching-sequence optimization for gradient error-compensation in thermometer-decoded DAC array," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 585–595, July 2000.
[11] M. Borremans, A. Van der Bosch, M. Steyaert, and W. Sansen, "A low power, 10-bit CMOS D/A converter for high speed applications," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2001, pp. 157–160.
[12] *High-Speed Design Techniques*, Analog Devices Inc., Norwood, MA, 1996.

A DDS-Based PLL for 2.4-GHz Frequency Synthesis

A. Bonfanti, F. Amorosa, C. Samori, and A. L. Lacaita

***Abstract*—In this transactions brief, we present a direct digital synthesizer (DDS)-based phase-locked loop (PLL), for frequency synthesis at 2.4 GHz with 80-MHz tuning range. The DDS signal is mixed with the voltage-control oscillatior output in the PLL feedback path. This solution helps in avoiding some of the typical tradeoffs in PLL. In particular, it is possible to achieve a very high-frequency resolution together with fast settling and spectral purity. These characteristics are often incompatible both in integer and fractional dividers PLL. A prototype was fabricated on PCBs and tested. The settling time is about 3 μs for 0.1 ppm (240 Hz) accuracy. Worst-case spurs are –53 dBc at 8-MHz offset from the carrier. The integrated phase noise in the band 1 kHz –1 MHz is 0.9° rms. This architecture is also suitable for direct frequency modulation, without necessitating any calibration system.**

***Index Terms*—Direct digital synthesizer (DDS), frequency synthesis, phase-locked loop (PLL), phase noise, wireless communication.**

I. Introduction

A phase-locked loop (PLL) adopted as a frequency synthesizer in wireless communication systems has to match tight conflicting requirements. Frequency tuning range of several tens of megahertz has to be covered and adjusted within frequency steps of some hundreds of hertz or less. Spurs must be carefully minimized, calling for narrow-loop bandwidth, but on the other side, settling time in channel switching has to be short, in some cases less than 1 ms. These specifications cannot be usually fulfilled by using a PLL with an integer-*N* divider. A PLL for the synthesis in gigahertz range, with a frequency accuracy of 1 kHz, should have $f_{\rm REF} = 1$kHz, a loop bandwidth narrower than 100 Hz and an enormous division factor which would impair the inband phase noise performance [1]–[3]. A fractional-*N* divider PLL partially solves these problems. However, it introduces fractional spurs and a tradeoff still exists between frequency resolution and agile frequency switching. With $f_{\rm OUT}$ in the gigahertz range, a very good frequency resolution 1 Hz has been demonstrated but with a loop bandwidth less than 100 kHz [4]. In this transactions brief, we describe a 2.4-GHz PLL which is free from above mentioned tradeoffs. Our architecture is similar to an offset PLL [5]–[7], but it uses a direct digital synthesizer (DDS) to generate the offset frequency. We also show that this architecture allows for a large PLL bandwidth. That characteristic, together with the use of the DDS, makes this synthesizer potentially suitable for direct frequency modulation, without requiring any preemphasis and digital calibration loop that are instead necessary in fractional-*N* PLL [8]. We focused on the following requirements: the output frequency must span the 80-MHz band around 2.4 GHz with a 1-kHz resolution, the settling time for a 0.1 ppm accuracy has to be less than 10 μs, the integrated phase noise in the band 1 kHz -1 MHz less than 1° rms, and the spurs below -50 dBc at few megahertz from the carrier. The system has been implemented with commercially available components on three PCBs. Measurements demonstrate good performance in terms of noise, spurs, accuracy, and fast channel switching.

Manuscript received October 1, 2002; revised March 26, 2003. This work was supported in part by the Italian Ministry of Research (MIUR) in the Frame of PRIN 2003 Project. This paper was recommended by Associate Editor K. Yang.

A. Bonfanti, C. Samori, and A. L. Lacaita are with the Department of Electronics and Information Technologies, Politecnico di Milano, Milano, 20133 Italy (e-mail: bonfanti@elet.polimi.it).

F. Amorosa was with the Department of Electronics and Information Technologies, Politecnico di Milano, Milano, 20133 Italy. She is now with Accent, Milano, 20137 Italy.

Digital Object Identifier 10.1109/TCSII.2003.820250

II. DDS–PLL Architecture

Fig. 1(a) shows the simplest form of a DDS. The clock drives a phase accumulator, whose output sweeps a PROM, providing a digital sine wave at its output, afterward converted into an analog signal by the DAC. The frequency is varied via a tuning word, by setting the number of points to skip in building the phase ramp. Today, commercially available DDS can not be driven with a frequency higher than 300 MHz, therefore, the highest output frequency is 75 MHz, assuming at least four samples per period. The minimum frequency step depends on the length of the tuning word. The DDS employed in this project is tunable with a 48 b word, equivalent to a minimum frequency step of about 1 μHz. Its output spectrum is characterized by the presence of many spurious signals. Fig. 1(b) shows the output of our DDS when 26 MHz are synthesized using a 280-MHz clock. It is easy to recognize the two replicas, at $f_{\rm CLOCK} \pm 26$ MHz, attenuated with a *sinc* shape, due to the sampled-and-held nature of the output signal. Their location is well known, and they can be easily filtered. The noise floor is instead due to the quantization noise of the D/A, [1], in our case 12 b. Given its high-frequency resolution, the DDS appears also interesting in wireless applications, the only shortcoming being the low-output frequency. A straightforward solution is to use the DDS as a reference for a *N*-integer PLL with *N* fixed. The channel selection is performed by the DDS itself, which can change its frequency by a very fine step. Unfortunately, as seen in Fig. 1(b), the DDS is far from being an ideal source, its noise floor and spurs are transferred to the output amplified by N^2 in power. Usually, this number is still high, impairing the use of this scheme in the RF field.

To overcome this limit, the system in Fig. 2(a) does not use the DDS as a reference. After the D/A conversion, the DDS output is instead mixed to the VCO output. The image rejection mixer (IRM) removes the high side mixing product. When the PLL is locked, the relationship between the signals in Fig. 2(a) is

$$f_{\rm OUT} = N \cdot M \cdot f_{\rm REF} + M \cdot f_{\rm DDS}. \quad (1)$$

In this scheme, the channel selection term $M \cdot f_{\rm DDS}$ is independent of $f_{\rm REF}$. In this way, $f_{\rm REF}$ can be high, allowing a large PLL bandwidth and fast frequency switching. The division factor $N \cdot M$ is consequently reduced, lowering the amplification of the PFD and divider phase noise. The $f_{\rm OUT}$ resolution depends only on the DDS being $\Delta f_{\rm OUT} = M \cdot \Delta f_{\rm DDS}$.

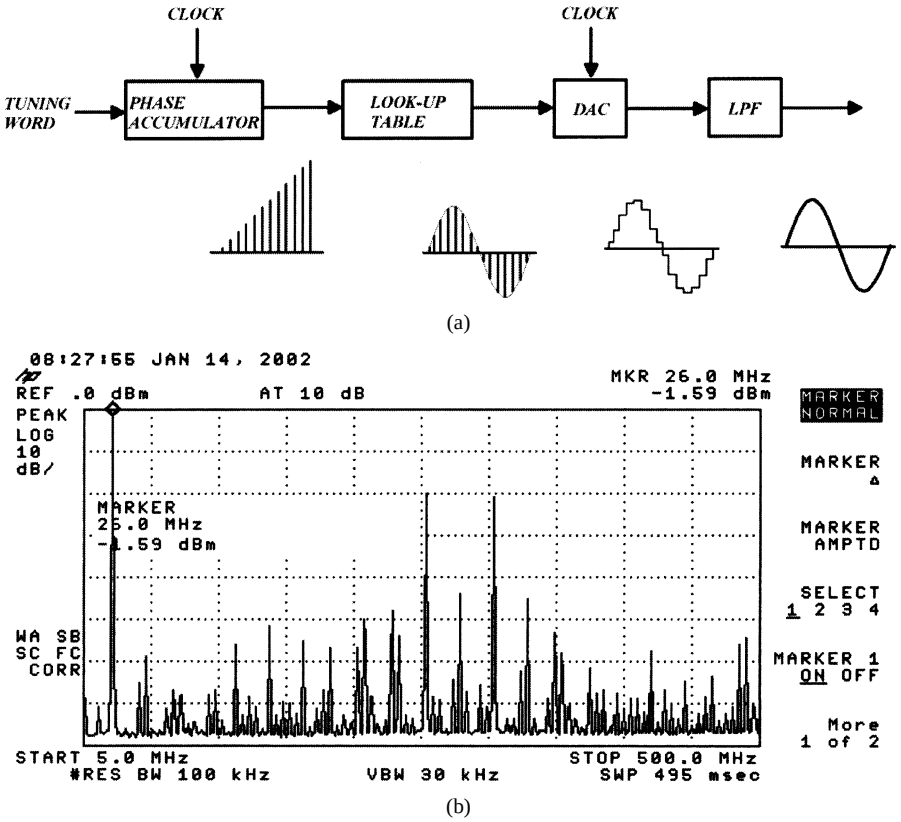

Fig. 1. (a) Building blocks of a DDS and (b) measured output spectrum.

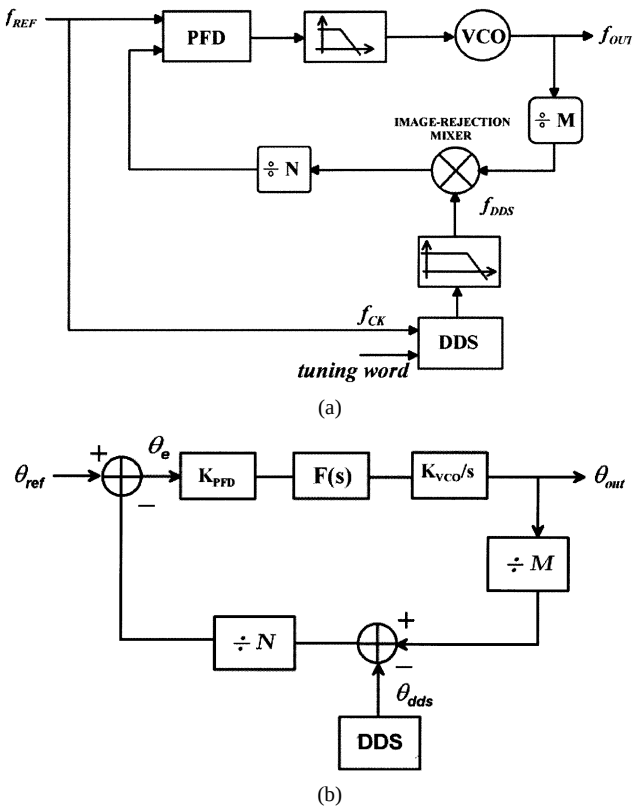

Fig. 2. (a) DDS-based PLL and (b) its linear model.

This synthesizer structure is similar to an offset PLL [5]–[7] where a low-frequency PLL takes the place of the DDS. With respect to these solutions our system has a much finer frequency resolution, and features the possibility to digitally modulate the output frequency. Note that this capability is achieved together with a large bandwidth, that makes the system also suitable for direct generation of frequency modulation schemes, as FSK, GFSK, etc. The direct frequency modulation has been already demonstrated in [8], by modulating the fractional division factor in a PLL. However, as explained in [4], the PLL band has to be very narrow to achieve the desired frequency accuracy. That, in turn, entails a preemphasis of digital data, and the use of a complex calibration loop for the PLL parameters, to match the preemphasized signal band.

To simplify the practical implementation, in our prototype a single 70 MHz signal was used both as input reference and as DDS clock. The clock is multiplied by four inside the DDS and the highest DDS frequency results 70 MHz. The DDS output is fed to an external low-pass passive filter, featuring a flat band up to 80 MHz, and an attenuation larger than 40 dB from 150 MHz. The filter removes the spurs lying at $f_{\mathrm{CLOCK}} \pm f_{\mathrm{DDS}}$, shown in Fig. 1(b).

Since the DDS cannot cover the target 80-MHz range, the divider-by-M (prescaler) was inserted to reduce the DDS frequency range to 80/M MHz. The prescaler, however, amplifies by M^2 the DDS noise and spurs, therefore, the factor M has to be kept as low as possible. We adopted $M = 2$. The DDS is correspondingly tuned between 8 and 48 MHz, with a minimum step, Δf_{DDS}, of 500 Hz. A finer step can be easily achieved with our DDS, but it would be beyond the resolution of the test setup. The second divider has $N = 16$, therefore, f_{OUT} varies between 2256 and 2336 MHz with 1 kHz steps, see (1). The VCO covers the range 2.2 –2.6 GHz with an average gain $K_{\mathrm{VCO}} \cong 160$ MHz/V. The PFD has a gain $K_{\mathrm{PFD}} \cong 1.8/2\pi$ V/rad. Its output is a current signal that is then fed to the external *RC* low-pass filter. The pole of the filter was set at 2 MHz ($\mathrm{R} = 390\ \Omega$, $\mathrm{C} = 200$ pF).

The dynamics of the PLL can be studied using the well-known linear model [2], [3]. In Fig. 2(b), the variables are the signal phases, θ_{REF}

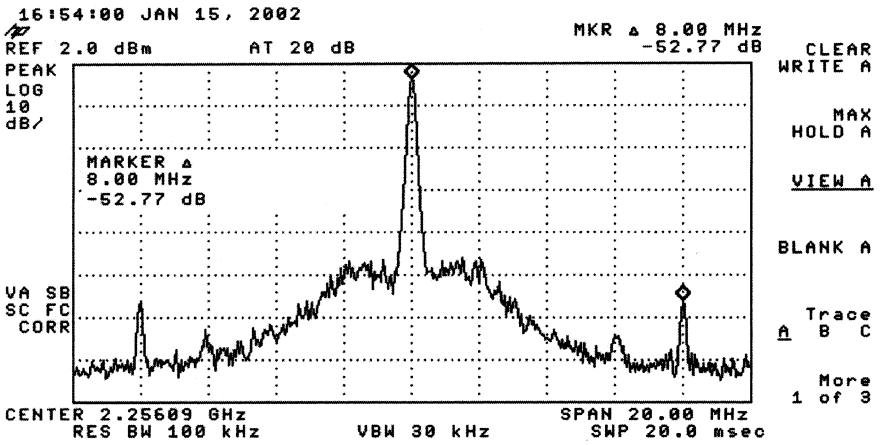

Fig. 3. Measured output spectrum, for a frequency span $= 20$ MHz.

and $\theta_{\rm OUT}$, and the VCO acts as an ideal integrator. With respect to the usual framework there is just an extra element, the image rejection mixer. This component adds the phase of the DDS signal, $\theta_{\rm DDS}$, to the divided output phase $\theta_{\rm OUT}/{\rm M}$. The resulting second-order systems has complex poles at 1.7 MHz and a phase margin of 54°.

III. Experimental Results

Measurements were performed on a prototype mounted on FR-4 two-layered PCBs. Fig. 3 shows the output spectrum. The spurs due the PFD lie at 70 MHz from the carrier and, given their high-frequency offset, they are strongly attenuated by the loop bandwidth. Closer spurs are due to the LO feedthrough in the mixer, whose maximum rejection is about 30 dB respect to the wanted sideband. The worst case is when the DDS generates the lower frequency, 8 MHz, as in Fig. 3. In this case the spurs at 8 MHz are very close to the carrier and are not much filtered by the loop. According to the linear model in Fig. 2(b), a phase modulation at 8 MHz at the mixer output transfers to the PLL output attenuated by 27 dB. This figure is evaluated by considering that the feedthrough gives rise to a single-sideband signal. The phase modulation in Fig. 2(b) is therefore reduced by 6 dB, then transferred to the output. The 8-MHz spurs in Fig. 3 are at -53 dBc, close to the expected value of (-30 -27) dBc = -57 dBc. The DDS also creates close-in spurs, mainly due to the truncation of the phase word, the so-called truncation spurs [9]. In our case, the length of the phase word is 14 b, that gives a worst case level for the spurs close to -84 dBc, about -6.02 times the number of bits [9]. Another kind of spurs comes from the finite-amplitude wordlength in the ROM. In our case, the amplitude of the sinewave is quantized with 12 b, which again limits the worst case spurs to -72 dBc. Both of these kinds of spurs are, therefore, lower than the feedthrough tones in Fig. 3, even if they fall within the PLL band and are not filtered by the loop transfer function. Also, these spurs are single sideband, and the 6-dB reduction must be taken into account. Fig. 4 shows the measured output phase noise $\mathcal{L}(f_m)$. In order to assess the level of this noise, the transfer of the various noise sources in the PLL was analyzed. It results that the main contribution to the output phase spectrum is the noise of the PFD output stage, sketched in Fig. 5. The operational amplifier makes this stage very noisy. Its output current noise was measured with an instrumentation amplifier, and features a white spectral density $\sqrt{S_I(f_m)} \cong 250\ {\rm pA}/\sqrt{\rm Hz}$, which is equivalent to an input phase-noise $S_I(f_m)|Z(j2\pi f_m)|^2/K_{\rm PFD}^2$, where $Z(j2\pi f_m)$ is the *RC* filter impedance. The input–output transfer function of this noise is low-pass shaped with a 1.7-MHz bandwidth, leading to a prediction of $\mathcal{L}(300\ {\rm kHz}) \cong$ -99 dBc/Hz, as experimentally obtained, see

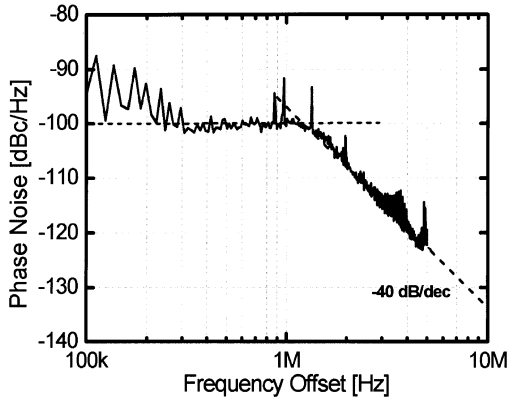

Fig. 4. Phase noise versus the frequency offset f_m from the carrier.

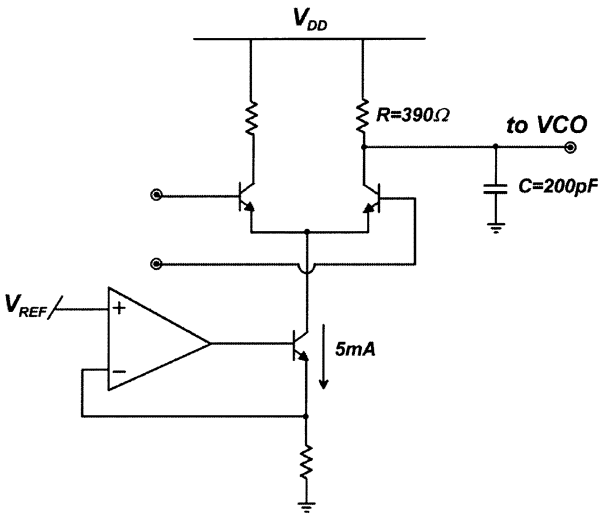

Fig. 5. Output stage of the phase-frequency-detector.

Fig. 4. The integral noise in the 1 kHz–1 MHz band is about 0.9 ° rms. We report in Fig. 6 the relative contribution of the other building blocks to the output spectrum. The VCO noise measured on the stand-alone oscillator is very low. The noise of the chain composed by the two dividers, M-divider and N-divider, was measured using the correlation technique described in [10]. This noise power is reported in Fig. 6 already multiplied by $({\rm MN})^2$, that is the amount of amplification within

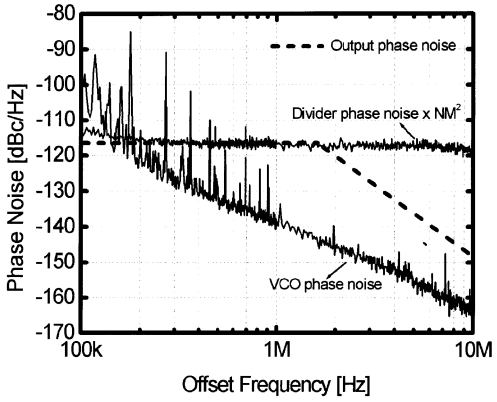

Fig. 6. Contribution of the VCO and of the dividers to the PLL output phase noise.

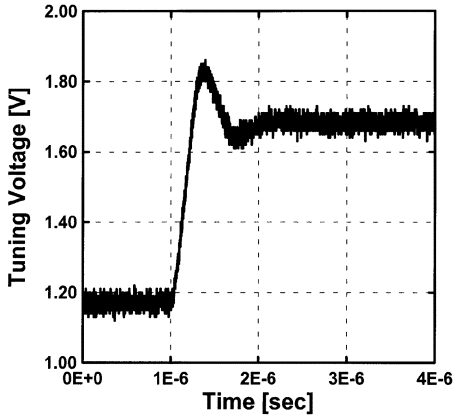

Fig. 7. Measured tuning voltage time transient, for 80-MHz step at output frequency.

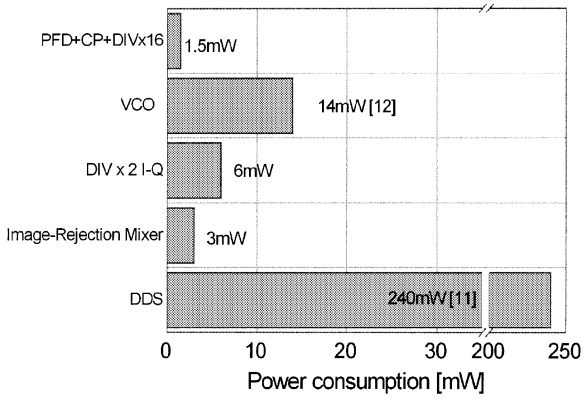

Fig. 8. Power budget for an integrated implementation.

the PLL band. The dashed curve shows the sum of the two contributions transferred to the PLL output, in practice only the divider term matters. The noise of the IRM and the phase noise of the DDS were instead obtained from data sheets and results negligible. This demonstrates the dominant role of the PFD noise.

Finally, Fig. 7 shows the time-domain waveform of the VCO tuning voltage, for an 80-MHz output frequency step. It is the step response of the PLL for the maximum input signal. The spurs at $\pm f_{\mathrm{REF}}$ from the carrier causes a modulation that makes impossible to evaluate the 0.1 ppm settling time, since it would imply to resolve a 1.5-μV signal. After numerical filtering, the settling time for 1000 ppm was estimated to be 0.9 μs in good agreement with the linear model. The same model gives a 3-μs settling-time for 0.1-ppm accuracy.

IV. Conclusion

This transactions brief presents a frequency synthesizer at 2.4 GHz, which achieves at the same time high-frequency resolution (1 kHz), fast switching (3-μs settling-time at 0.1 ppm) and good spectral purity (spurs $<$-50 dBc). The inband phase noise is not limited by the DDS and could be easily reduced using/designing a less noisy PFD. The architecture can be also profitably used in transmitters, when direct frequency modulation schemes are adopted. Finally, concerning a possible fully-integrated implementation of the system, the main weakness is the power consumption of the DDS-DAC blocks. Recently, some low-power solutions have been presented, for instance [11], that adopts a ROM-less DDS and nonlinear DAC and consumes 240 mW with a 300-MHz clock. Fig. 8 presents a possible power budget for an integrated implementation, based on data reported in literature.

References

[1] B. G. Goldberg, *Digital Techniques in Frequency Synthesis.* New York: McGraw-Hill, 1986.
[2] F. M. Gardner, *Phaselock Techniques*. New York: Wiley, 1979.
[3] W. F. Egan, *Frequency Synthesis by Phase Lock*, 2nd ed. New York: Wiley, 2000.
[4] W. Rhee, B. S. Song, and A. Ali, "A 1.1 GHz CMOS fractional-N frequency synthesizer with a 3-b 3rd-order delta sigma modulator," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1453–1460, Oct. 2000.
[5] T. Yamawaki *et al.*, "A 2.7-V GSM RF transceiver IC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2089–2096, Dec. 1997.
[6] A. N. Hafez and M. I. Elmasry, "A low monolithic subsampled phase-locked loop architecture for wire less transceivers," in *Proc. IEEE Symp. Circuits Systems*, vol. 2, May–June 1999, pp. 549–552.
[7] T. K. K. Kan, G. C. T. Leung, and H. C. Luong, "A 2 V 1.8 GHz fully integrated CMOS dual-loop frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1012–1020, Aug. 2002.
[8] D. McMahill and C. Sodini, "A 2.5-Mb/s GFSK 5.0-Mb/s 4-FSK automatically calibrated $\Sigma-\Delta$ frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, pp. 18–26, Jan. 2002.
[9] H. T. Nicholas III and H. Samueli, "An analysis of the output spectrum of direct digital frequency synthesizers in the presence of phase accumulator truncation," in *Proc. 41st Annu. Frequency Control Symp.*, 1987, pp. 495–502.
[10] W. F. Egan, "Modeling phase noise in frequency dividers," *IEEE Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 37, pp. 307–315, July 1990.
[11] J. Jiang and E. K. F. Lee, "A ROM-less direct digital frequency synthesizer using segmented nonlinear digital-to-analog converter," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2001, pp. 165–168.
[12] A. Zanchi, C. Samori, S. Levantino, and A. L. Lacaita, "A 2-V 2.5-GHz–104-dBc/Hz at 100 kHz fully integrated VCO with wide-band low-noise automatic amplitude control loop," *IEEE J. Solid-State Circuits*, vol. 36, pp. 611–619, Apr. 2001.