A Dead-Beat Adaptive Hysteresis Current Control

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***Abstract*—This paper proposes a new digital algorithm for the implementation of the fixed-frequency adaptive hysteresis current control for voltage-source inverters. The key features of the new algorithm are the minimization of the analog external circuitry, the capability to automatically compensate for the inverter deadtime effects without appreciable delay and a tight synchronization of the inverter voltage pulses with an external clock. The synchronization is actually inherent in the implemented algorithm and does not require additional control loops; the stability problems affecting all the solutions proposed so far are, therefore, avoided and a steady switching frequency is achieved. Even though the complexity of the algorithm is compatible with many conventional microcontrollers' performance level, the implementation with a commercial digital signal processor is considered in order to achieve ultrasonic operating frequency and to test the effectiveness of the solution in more demanding conditions.**

***Index Terms*—Current control, digital signal processor, hysteresis control, voltage-source inverter.**

I. Introduction

THE hysteresis current control technique [1]–[3] has proven to be the most suitable solution for all the applications of current controlled voltage source inverters where performance requirements are more demanding, such as active filters and high-performance ac power conditioners. As it is well known, the hysteresis control is characterized by unconditioned stability, very fast response, and good accuracy. On the other hand, the basic hysteresis technique exhibits also several undesirable features, such as variable switching frequency and heavy interference among the phases in case of three-phase systems with isolated neutral. Much research work has been done in past and recent years to eliminate such drawbacks and many effective solutions have been found [4]–[8], which essentially improve the performance controlling the hysteresis band width by means of additional regulators. Although the core of the hysteresis control is inherently analog, the digital implementation of the hysteresis band regulators is not only possible, but strongly recommendable to exploit the well known advantages of the digital control techniques over the analog ones. In previous research work, the possibility of achieving at least a stable switching frequency by means of digital algorithms controlling the hysteresis band has been demonstrated [6], [7]. However, a satisfactory solution for the problem of keeping a stable and controllable phase shift between the inverter phase voltage pulses, which is automatically solved by conventional control strategies (e.g., space vector modulation), and which is often recommendable in case of three-phase applications, has not yet been found. This paper presents an effective solution to this problem, proposing a new digital dead-beat synchronizing algorithm. With only minimal external analog circuitry, essentially reduced to three comparators, and with a simple digital implementation, the algorithm achieves a stable switching frequency in the steady state and a high speed of response in the presence of step variations of the current reference or other similar transients. Moreover, the generated switching pulses are inherently locked to an external reference clock, thus allowing to achieve a minimum ripple condition in three phase applications with isolated neutral [2]. Finally, the proposed control is apt to automatically achieve inverter deadtimes' compensation, thus allowing to correct the induced current waveform distortion without appreciable delay. Of course, as any hysteresis current control, also the proposed algorithm requires only time measurements, thus avoiding A/D conversions and the related delays, which limit the performance of other control techniques (e.g., dead-beat current control). Even if the required calculations could be easily performed by means of conventional microcontrollers, the considered implementation adopts a fixed-point digital signal processor (DSP) (TMS320F240) which allows it to achieve ultrasonic switching frequency.

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II. Proposed Digital Control Principle

The operating principle of the new algorithm can be described referring to Fig. 1, where a single-phase voltage-source inverter with digital hysteresis control is shown. For the sake of generality, the load is assumed to include also a resistive impedance and a voltage source so as to represent a wide variety of possible applications, from adjustable speed drives to active filters or pulsewidth modulation (PWM) rectifiers. The explanation of the control algorithm is done in two different cases: initially, an ideal operating condition is considered where the converter deadtimes are neglected; afterwards, the effect of the converter deadtimes is taken into account and the necessary modifications to the control algorithm, which compensate for that, are presented.

A. Control Operation Neglecting Deadtimes

The control principle, in this case, is shown in Fig. 2, where some relevant waveforms and control variables are depicted.

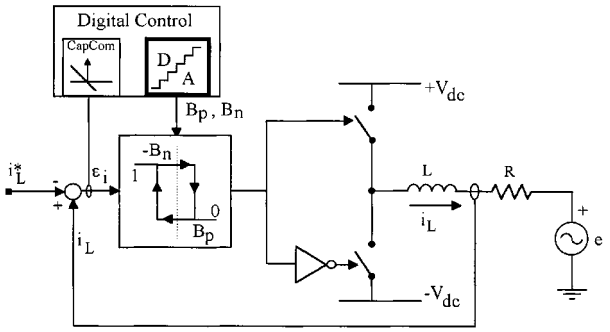

Fig. 1. Simplified schematic of the hysteresis current control.

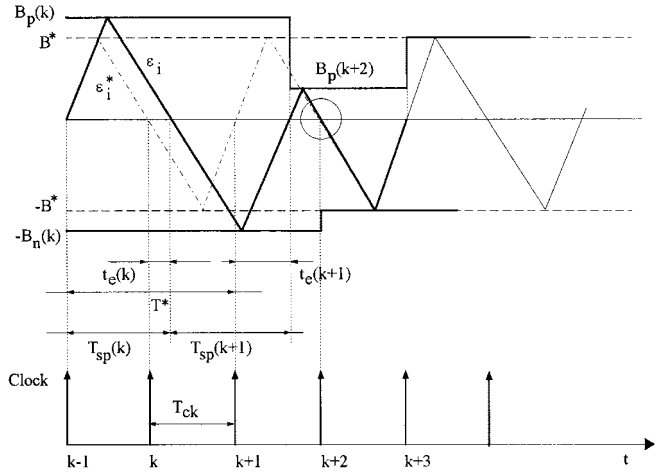

Fig. 2. Principle of control operation with negligible deadtimes.

As usual in any hysteresis current control, the current error ε_i is compared to the hysteresis bands B_p and $-B_n$. These are automatically adjusted by the digital control so as to keep the switching frequency stable at the desired level. In order to do that, the control algorithm operates considering as an input the time distance t_e between the current error zero crossing and the occurrence of the pulse of a synchronization external clock. Referring to a steady-state condition, where the slopes of the current error can be considered constant, there is a certain amplitude of the hysteresis bandwidths B_p and $-B_n$ (B^* and $-B^*$, respectively, in Fig. 2) which corresponds to the desired switching frequency [4]. The figure assumes an initial error in the value of B_p and $-B_n$ with respect to the correct hysteresis bandwidth, which causes the behavior of the current error ε_i to differ from the desired one ε_i^* (dashed-dotted line). As a consequence, at the first current error zero crossing, the control algorithm *measures* $t_e(k)$, with respect to the last clock pulse, which is supposed to take place at instant $k \cdot T_{\rm ck}$ (from now on indicated simply as instant k), and then *estimates* the expected time error in the following modulation half-period $t_e(k+1)$ according to

$$t_e(k+1) = t_e(k) + T_{\rm sp}(k+1) - \frac{T^*}{2} \tag{1}$$

where

$$T_{\rm sp}(k+1) = \frac{B_n(k)}{B_p(k)} \cdot T_{\rm sp}(k) \tag{2}$$

is the *estimated* duration of the following modulation half-period and T^* is the desired modulation period, of course equal to $2 \cdot T_{\rm ck}$. As can be seen, (2) is based on the *measured* duration of the last half-period $T_{\rm sp}(k)$ and on simple geometrical considerations. In this calculation, the value of B_n taken into account is the one resulting from the calculations based on the previous zero crossing of ε_i. This avoids timing problems related to the calculation delay because, at any zero-crossing, the algorithm modifies the hysteresis band the current error is not going to. This gives it enough time to complete the calculations.

The control algorithm can now determine the new value of the hysteresis band $B_p(k+2)$, which will force the time error $t_e(k+2)$ to go to zero. In order to do that, at first, the value of the correct hysteresis band $B^*(k)$ is derived, as in

$$B^*(k) = \frac{T^*}{2} \cdot \frac{B_p(k)}{T_{\rm sp}(k)}. \tag{3}$$

Then, $B_p(k+2)$ is calculated as

$$\frac{B_p(k+2)}{B^*(k)} = \frac{\frac{T^*}{2} - t_e(k+1)}{\frac{T^*}{2}} \tag{4}$$

and, therefore,

$$B_p(k+2) = B_p(k) \cdot \frac{T^* - t_e(k) - T_{\rm sp}(k) \cdot \frac{B_n(k)}{B_p(k)}}{T_{\rm sp}(k)} \tag{5}$$

where all the variables in the right-hand side of the equation are known to the algorithm from measurements or previous calculations. According to this strategy, which can actually be considered a dead-beat control of the switching pulses phase error, the timing error $t_e(k)$ at instant $k+2$ (i.e., the end of the modulation period following the initial current error zero crossing) is reduced to zero, as shown in Fig. 2. At the next current zero crossing, based on the *measured* $t_e(k+1)$, the same calculations are performed for the opposite hysteresis band, and so on. Therefore, the two bands can be independently adjusted by the digital control. This allows, theoretically, the ability to get the correct bandwidth in only two control cycles, that is, in a single modulation period. In other words, the control is theoretically capable of eliminating any synchronization error with a two-cycle delay, offering, in principle, an excellent dynamic performance. It is worth noting that this mode of operation implies that the resulting voltage pulses, produced by the corresponding inverter leg, are automatically centered in the modulation period.

B. Control Operation With Deadtimes

Since the band regulations are independent of each other, with this control strategy it is also possible to implement a compensation for deadtimes' effects. In this case, the control algorithm gets to a steady-state condition with unbalanced band widths $(B_n \neq -B_p)$ so as to keep the switching frequency at the required value and the voltage pulses centered in the modulation period and, also, when relevant and even unsymmetrical deadtimes are considered. To explain the compensation strategy we refer to Fig. 3. As can be seen, the presence of a deadtime implies a delay in the current commutation instant which can be interpreted as a difference between the calculated hysteresis band,

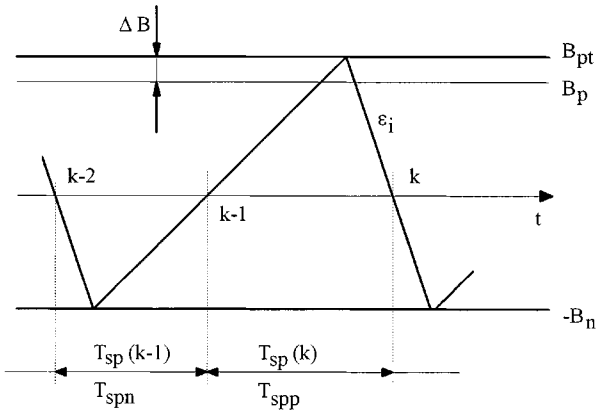

Fig. 3. Control operation with deadtimes.

B_p in this case, and the actual one. This difference ΔB can be calculated by the algorithm based on

$$B_{pt}(k) = \frac{T_{\mathrm{sp}p}}{T_{\mathrm{sp}\,n}} \cdot B_n(k) = \frac{T_{\mathrm{sp}}(k)}{T_{\mathrm{sp}}(k-1)} \cdot B_n(k) \qquad (6)$$

where the actual hysteresis band B_{pt} is determined, given the durations of the positive and negative current half-periods T_{spp} and T_{spn}, respectively. It is worth noting that this calculation expressed by (6) uses data collected in the previous modulation period, from instant $k-2$ to instant k. Therefore, the application of (6) introduces another two cycle delay in the control response. On the whole, the expected delay of the control algorithm in the suppression of any given perturbation is four clock periods, equal to two modulation periods. Of course, the control delay does not affect the average current regulation, which is maintained, as in any conventional hysteresis current control, but only the synchronization of the switching pulses. The algorithm calculates the error in the hysteresis band according to

$$\Delta B_p(k) = B_{pt}(k) - B_p(k) \qquad (7)$$

and applies a correction to the band calculation, substituting to B_p the quantity $B_p + \Delta B_p$ in (2), (3) and (4), so as to get the final expression of the positive band, that is,

$$B_p(k+2) = [B_p(k) + \Delta B_p(k)] \cdot \frac{T^* - t_e(k) - T_{\mathrm{sp}}(k) \cdot \frac{B_n(k)+\Delta B_n(k)}{B_p(k)+\Delta B_p(k)}}{T_{\mathrm{sp}}(k)} - \Delta B_p(k) \qquad (8)$$

where the analogous correction term ΔB_n is also used. It is worth noting that, at any current zero crossing, it is not possible to know which band is the one affected by the presence of the deadtimes, since this depends on the sign of the average inverter current. Therefore, the calculation of ΔB_p and ΔB_n is performed simultaneously; of course only one of them will significantly differ from zero at a given instant. Equation (8) and the obvious symmetrical equation necessary to update the negative band value represent the implemented control algorithm.

C. Extension to Three-Phase Converters

The application of the described control strategy to a three phase converter is almost straightforward, once the decoupling

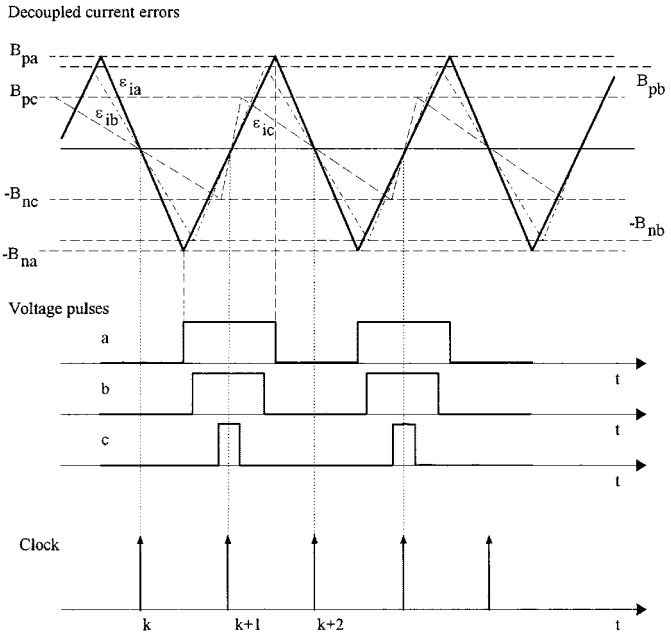

Fig. 4. Expected control operation in a three-phase system.

of the current errors is operated [2], in the case of an isolated neutral three-phase system. The decoupled current errors can then be simultaneously processed by the controller, and the time error with respect to the same synchronizing clock can be evaluated for each phase. The resulting behavior of the decoupled current errors and of the respective inverter voltage pulses is shown in Fig. 4. As can be noted, the synchronization of the current error zero crossings for the three phases with the same clock implies that the converter voltage pulses are centered in the modulation period, which, as is known, reduces the current ripple's amplitude to the minimum.

III. Simulation Results

The presented algorithm has been initially tested by simulation, so as to verify the performed theoretical analysis. In particular, the simulations were focused on the verification of the expected dynamic speed of response of the deadtime compensation strategy and on the validation of the adopted saturation strategy. Indeed, it is always necessary to limit the hysteresis bandwidth between a minimum and a maximum level [4], [5], in order to prevent uncontrolled variations of the switching frequency. In this control strategy, when the minimum band limit is reached, e.g., during inverter operation at high modulation indexes or during transients, the average current error is kept to zero, while the switching frequency is no longer controlled and decreases. Control of the switching frequency is resumed once the saturation is over.

Fig. 5 shows the control's response to a perturbation in the hysteresis bands. As can be seen, similarly to what is described in Fig. 2, the control algorithm is able to reduce the synchronization error t_e to zero in only two control cycles, that is in a single modulation period (50 μs in this case). Of course, the switching frequency reaches the correct value only at the end of another complete modulation period.

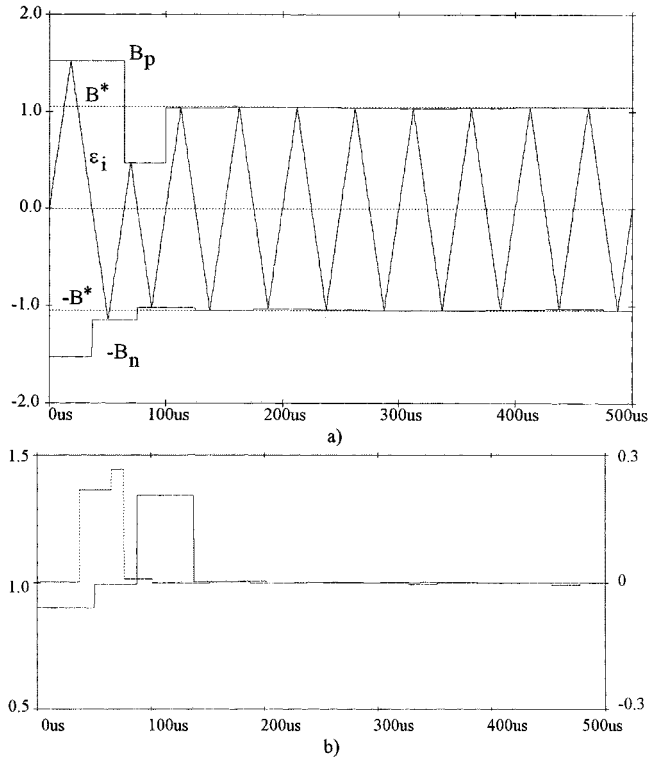

Fig. 5. (a) Bandwidth correction neglecting deadtimes (control's dynamic response). (b) Frequency regulation (solid line: normalized switching frequency) and instantaneous time error t_e (dotted line: normalized to the switching period T^*).

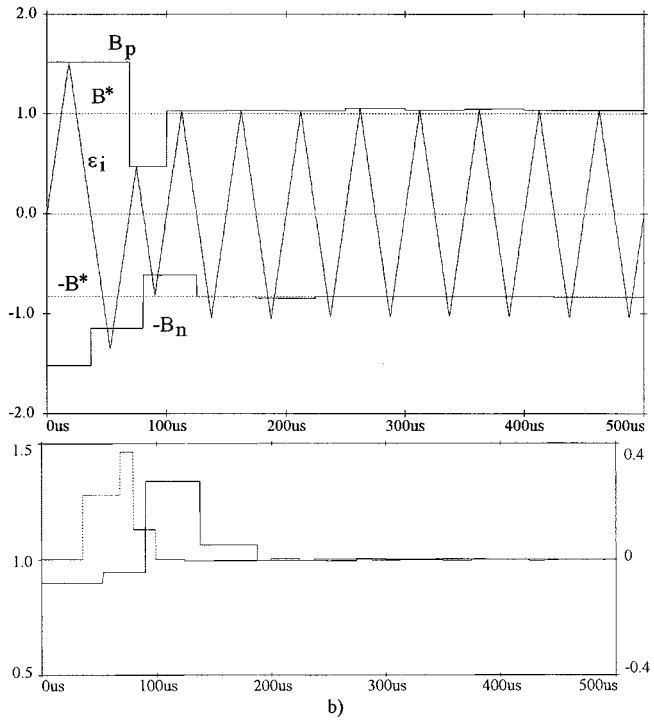

Fig. 6. (a) Bandwidth correction with deadtimes. (b) Frequency regulation (solid line: normalized switching frequency) and instantaneous time error t_e (dotted line: normalized to the switching period T^*).

Fig. 6 describes the control's behavior in the presence of deadtimes. As can be seen, in the steady state the average of the current error is kept to zero by unbalancing the positive and negative hysteresis bands, as predicted by the theoretical analysis. It is also worth noting that the transient duration is now almost doubled because of the deadtimes compensation algorithm. Finally, Fig. 7 shows the control's behavior during saturation. As can be seen, the control keeps the average current error to zero, but the switching frequency is allowed to decrease, in this particular case, down to about the 70% of the nominal value.

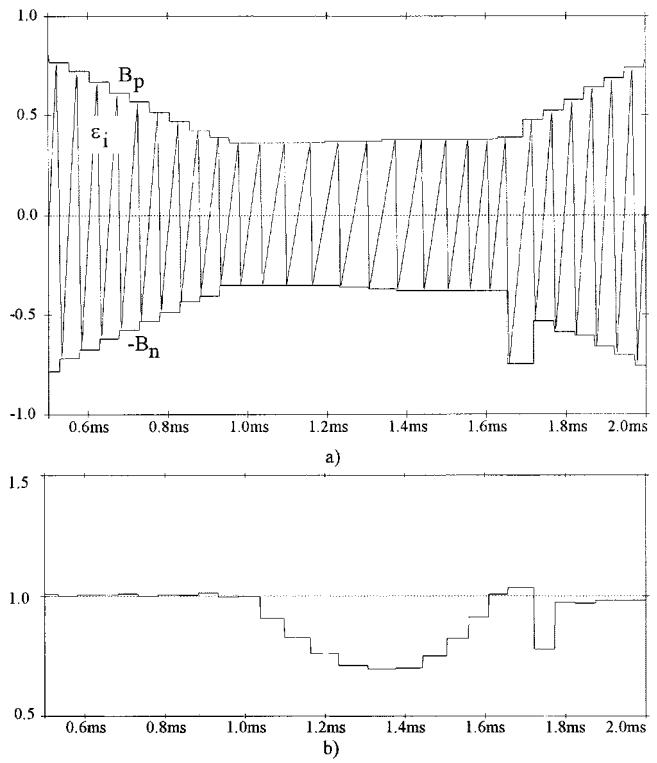

Fig. 7. (a) Control operation in saturated conditions. (b) Frequency regulation (normalized switching frequency).

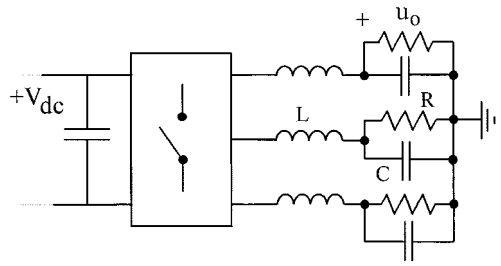

Fig. 8. Simplified schematic of the experimental converter.

IV. Experimental Measurements

The control algorithm discussed so far has been implemented and tested experimentally on a three-phase voltage-source inverter with inductive filter and resistive-capacitive load, as shown in Fig. 8 (R=6 Ω, C=3 μF). The converter's parameters are given in Table I.

As far as the controller implementation is concerned, a fixed-point 16-bit DSP (TMS320F240) has been used. Its peripheral units allowed a straightforward implementation of the control strategy; in fact, being conceived for the control of electrical drives, the chip comprises capture and compare

TABLE I
CONVERTER PARAMETERS

DC Link Voltage V_{dc}	300 V
Output Inductor L	1.8 mH
Switching Frequency	20 kHz
Nominal Output Power	5 kW

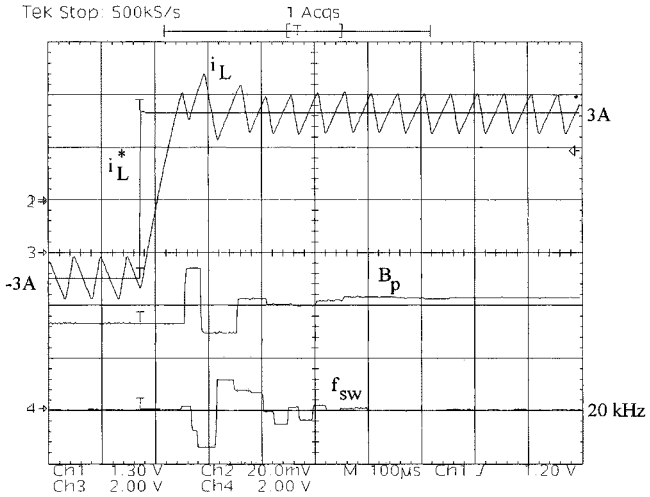

Fig. 9. Phase current step response. From top to bottom: phase current i_L and its reference i_L^* (2 A/div); hysteresis band B_p (0.6 A/div); instantaneous switching frequency $f_{\rm sw}$ (7.5 kHz/div).

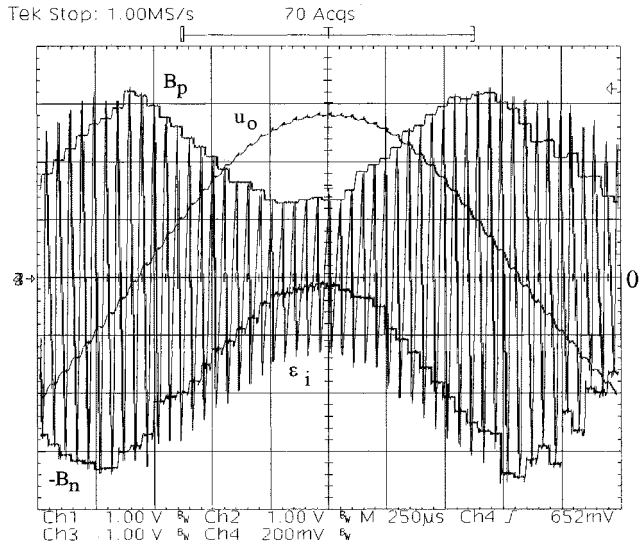

Fig. 10. Phase current in sinusoidal conditions: phase current error ε_i and hysteresis bands B_p and $-B_n$ (0.6 A/div); load voltage u_o (40 V/div).

programmable I/O pins, counters and, on the system's board, digital-to-analog converters (DAC's). The former are used to sense the current zero-crossing signals given by external analog comparators and to measure the time intervals, as required by the control algorithm. The latter are used to generate the hysteresis bands for the analog current controller. Unfortunately, the number of capture and compare units included in a single DSP chip are not enough to allow a three-phase implementation of the control system. Therefore,

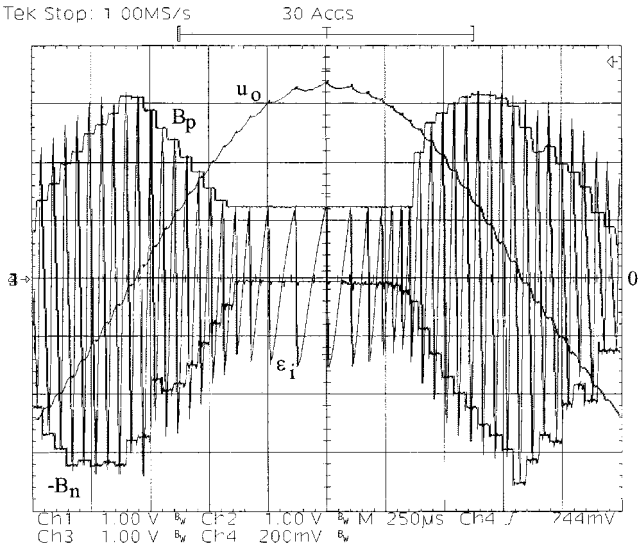

Fig. 11. Phase current in sinusoidal conditions: phase current error ε_i and hysteresis bands B_p and $-B_n$ (0.6 A/div); load voltage u_o (40 V/div).

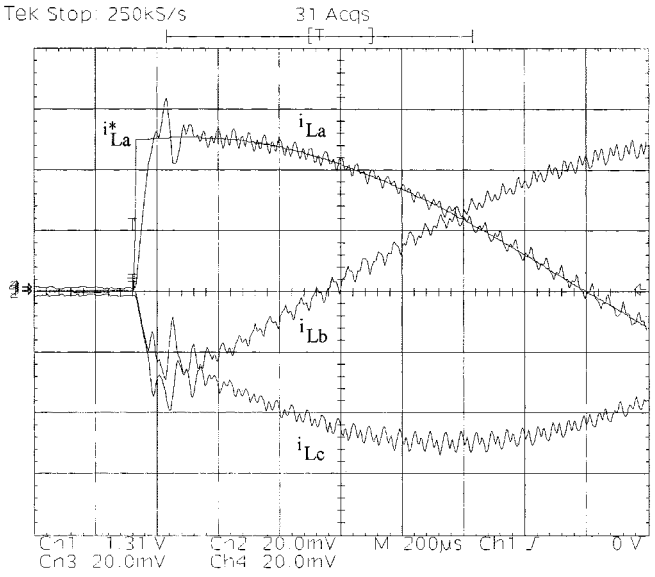

Fig. 12. Phase current step variation: phase currents i_{La}, i_{Lb}, and i_{Lc} (2 A/div); externally generated current reference i_{La}^* (2 V/div).

in the laboratory prototype, three boards were interconnected to allow the control of a three-phase inverter. This solution allowed to minimize the development time of the laboratory prototype. For an industrial implementation, on the basis of our experience, the best solution for this application could probably be represented by a single DSP core, TMS320F240 or similar, interfaced with external peripherals, implemented by means of a suitable application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA).

As far as the experimental activity is concerned, the first verification was done on the dynamic response of the control's system. Fig. 9 shows the system's step response. As theoretically explained, the correct band's amplitude and switching frequency is practically recovered in two modulation periods (another one is needed to measure frequency). The small oscillation in the frequency which can be observed in Fig. 9 is due to the

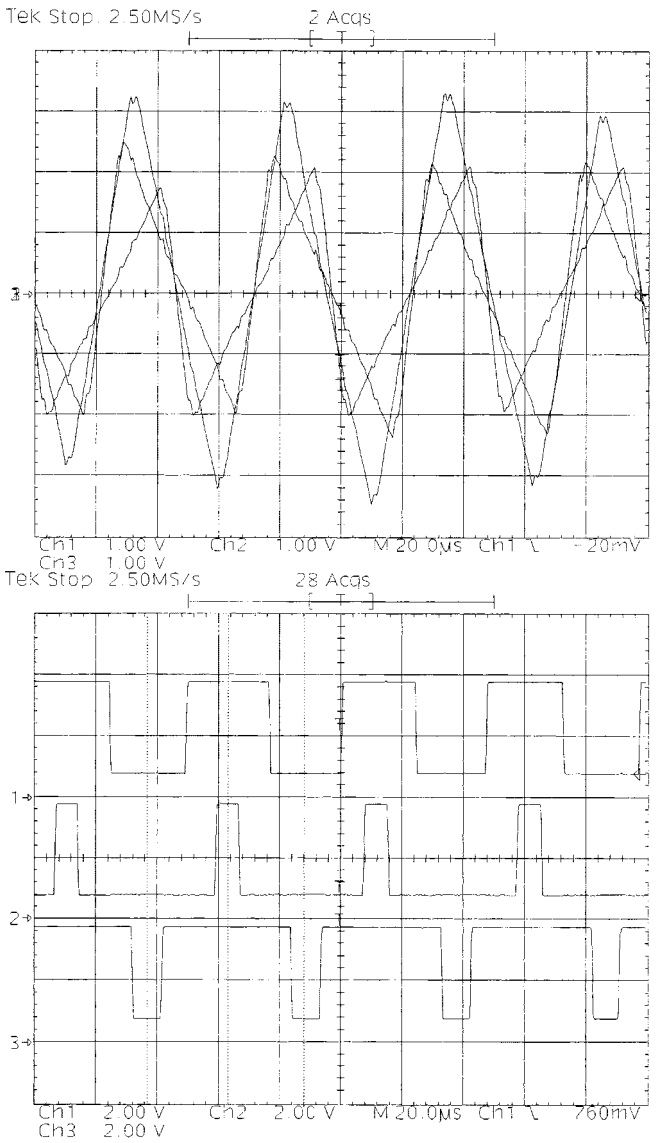

Fig. 13. Top: Phase current errors after decoupling (0.3 A/div); bottom: Gate signals for the power converter (5 V/div).

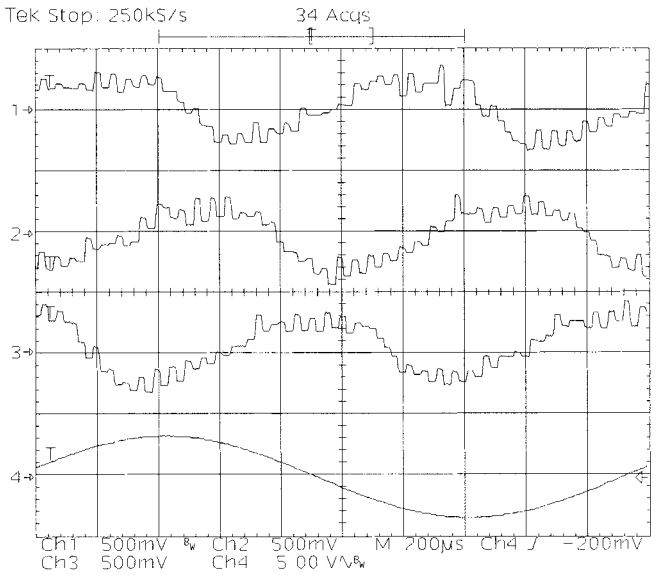

Fig. 14. Phase error (t_e variable) of the voltage pulses (60°/div) and current reference (bottom trace: 10 A/div).

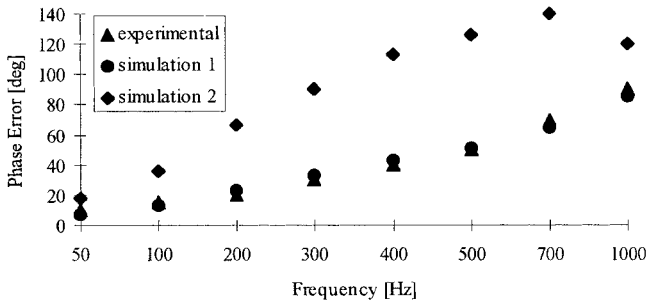

Fig. 15. Phase error in degrees between clock and phase voltage pulses. All plotted data refer to the generation of a sinusoidal current (6-A peak value) with a 0.8 modulation index.

saturation of the hysteresis band controller, which increases the duration of the transient. Instead, the steady-state performance of the system is shown in Fig. 10, where a 300-Hz sinusoidal current is being generated. As can be seen, the control system compensates for the deadtimes unbalancing the two hysteresis bands, as expected. Fig. 11 shows the converter operation in the saturation mode, where the switching frequency is no longer controlled. As can be seen, the ripple frequency decreases but its average value is kept to zero. Therefore, in saturated operating conditions no error is introduced in the replication of the current reference; the only effect of the hysteresis control saturation is a slight decrease in the ripple frequency.

In Fig. 12, the step response for the three phase currents is shown. As with any other type of hysteresis control, this allows a very quick dynamic response. As can be seen, the desired switching frequency is also rapidly recovered. The decoupled current errors are shown in Fig. 13, together with the inverter voltage pulses. As explained in the caption of Fig. 4, the synchronization of the current error zero crossings with the same clock for the three phases implies the centering of the switching pulses in the modulation period, which is fairly important for a significant reduction of the current ripple. Of course, the control delay implies a systematic error in the synchronization of the pulses, which is increasing with the frequency of the current reference. This can be interpreted as an instantaneous phase error for the voltage pulses. This is depicted for each phase in Fig. 14, in the case of a 500-Hz sinusoidal current reference. In practice, the figure shows the plot of the instantaneous value of the control variable t_e, as defined in Section II, for each of the converter's phases. Once turned into degrees, this reveals that the phase error between the voltage pulses and the reference clock, with a modulation index of about 0.8, is limited to about 40°. By measuring the maximum t_e with increasing current reference frequency and keeping the modulation index almost constant to about 0.8, it was possible to derive the diagram presented in Fig. 15. This gives a quantitative evaluation of the control system's tracking capability, in terms of the defined steady-state phase error between the clock pulses and the voltage pulses. Note that on the same diagram the maximum instantaneous synchronization errors estimated by simulation

are also reported. These are in good agreement with the measured ones. Of course, measurements and simulations refer to the same converter operating conditions, i.e., the generation of a sinusoidal current (6 A peak value) with a modulation index of about 0.8. To complete the comparison, the same synchronization error was evaluated by simulations referring to a different fixed frequency hysteresis current control method [4], [5] employing a phase-locked loop (PLL) circuit to control and minimize the phase error. The dynamic performance of this strategy is greatly affected by the PLL bandwidth, which, to obtain the data plotted in Fig. 15, was set to $1/4$ of the required modulation frequency in the worst case (i.e., when the modulation index is equal to 0.9). Again, the simulations were done in the same conditions of the previously discussed cases. As can be seen, the method presented in this paper exhibits a clear performance superiority. Moreover, it is worth underlining that the dead-beat hysteresis controller does not exhibit any of the stability limitations typical of the PLL solutions like the ones discussed in [4] and [5], since, of course, no external regulator design is required. A very smooth and stable frequency control can be achieved in the steady state; in dynamic conditions, the transient duration is very small, compared to any of the referred previous experiences.

V. Conclusion

This paper has presented a novel digital adaptive hysteresis current control, which is shown to be particularly simple and effective in achieving both a stable switching frequency and the phase control of the inverter voltage pulses, which are automatically centered in the modulation period. The control requires only minimal external analog circuitry and does not employ A/D converters. Thanks to a dead-beat approach, the control algorithm exhibits a quite high speed of response and any error in the hysteresis bandwidth can be recovered within a few modulation periods, thus resuming the synchronization of the voltage pulses. The regulation of the average current is in any case very good, as it is for all hysteresis methods. The effect of inverter deadtimes can also be automatically compensated. The effectiveness of the solution has been verified by means of numerical simulations and of experimental tests.

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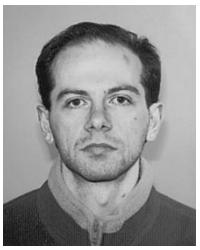

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