A DESIGN AND ANALYSIS OF HIGH PERFORMANCE VOLTAGE CONTROLLED OSCILLATORS

A Thesis

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Master of Science

by

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ABSTRACT

The voltage controlled oscillator (VCO) is one of the most important building blocks in modern communication applications such as microprocessor clock generation, wired and wireless communications, system synchronization, and frequency synthesis. The design of high performance VCOs has been increasingly more important and still is an active research area. Research on VCOs for the past decade has been concentrated in the areas of higher frequency, lower phase noise, low power, low operating voltage, and increased tuning range. However many of these objectives can be only achieved at the expense of some other objectives. This thesis analyzes the design of high performance of inductor-capacitor (LC) tank and ring VCOs. First the basics of both LC and ring VCOs are reviewed. Then through the basics, new LC VCO topologies and circuit tricks are derived and analyzed. The design, simulation, and layout guidelines are also provided. Finally, the circuit techniques used in both regular and quadrature VCOs and simulation results of regular inductor and symmetric inductor designs are compared. Next, the several single-ended and differential ring VCO topologies are reviewed and pros and cons for each type are provided. From the basic topologies, a new ring VCO cell topology is then introduced, along with the bias circuit, output buffers, and divider. A three stage VCO based on the new topology is designed and simulated in both thick-oxide and thin-oxide devices in 65nm CMOS SOI process. The results of thick and thin oxide devices are compared and confirmed the usability of the new ring VCO cell topology. Finally, a conclusion of the design of high performance LC and ring VCOs is drawn and new directions of research are predicted.

BIOGRAPHICAL SKETECH

Bin Wan was born on July 23rd, 1983 in Wuhan, China. He came to the U.S. in 1996 and graduated from J.J. Pearce High School in Richardson, Texas in 2001. He then attended University of Texas at Austin and graduated with Bachelor of Science in Electrical Engineering with High Honors in May 2004. Since June 2004, he is a graduate student in Cornell University, Electrical and Computer Engineering Department.

ACKNOWLEDGEMENTS

I would like first to thank my advisor, Dr. Kornegay, for his advice, and all the past and current members of Cornell Broadband Communication Research Laboratory for their support.

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Chapter 1 Introduction

Oscillators are a fundamental part in many electronic systems. Applications utilize oscillators range from clock generation in microprocessors to frequency translation in mobile phones. Different application also requires different set of oscillator performance parameters. As today's integrated circuits are converging towards CMOS, the design of robust and high-performance CMOS oscillators, more specifically, voltage-controlled oscillators (VCOs), has become extremely important.

1.1 VCO Metrics

The key metrics of a VCO consist of: oscillation frequency, tuning range, phase noise, and power consumption. The frequency of oscillation is determined by the application in which the VCO is used in, such as microprocessor or cellular phone. The tuning range is determined by the necessity of the application and the variation on oscillation frequency due to process and temperature variation. The center frequency of some CMOS oscillators may vary by a factor of two at the extremes of process and temperature [1], thus a wide tuning range is very desirable.

The design of low phase noise VCOs has become another major direction of research. The recent huge growth in wireless communication has demanded more available channels. As a result the phase noise requirement in the local oscillator becomes more stringent. In digital microprocessors, the phase noise of the oscillator will directly affect the jitter of the clock signal and the timing margin, thus limits system performance.

Lastly, power consumption is extremely important for mobile applications such as cellular phones and laptops where a battery supply the power. A low power design

will increase the battery life and low power designs are seen in many of the recent publications.

1.2 VCOs for Phase Locked Loops

Phase locked loops (PLLs) are common applications for VCOs. PLLs can be used for clock generations, such as in a microprocessor, clock and data recovery, such as in an optical transmission system, or frequency synthesis, such as in a wireless radio. The general characteristic for VCOs used in PLLs is wide tuning range so that the entire frequency range is covered. Also the phase noise requirement of the VCO can be loosened due to that when the loop is locked, the noise generated by the VCO at the center of oscillation frequency will be filtered out by the loop bandwidth. As a result, PLLs generally use wide tuning range and noisier ring topology VCO.

1.3 VCOs for Frequency Translation

Another common application for VCOs is frequency translation. In this type of application, such as radio and cellular phone, base band data needs to be up-converted to the carrier frequency for transmission, or received data down-converted to base band for processing. Typically, frequency translation requires the VCO to have very high oscillation frequency, on the order of gigahertz, and more recently, tens of gigahertz, due to the fact that carrier frequencies are becoming higher and higher. As a result, VCOs used for frequency translation typically uses inductor and capacitor (LC) tank VCO topology for its relatively high oscillation frequency and low phase noise.

Chapter 2 VCO Basics

Before venturing onto the more advanced VCO topologies and structures, this chapter briefly describes the basic operation principle behind regular oscillators and the two major VCOs families.

2.1 Fundamentals of Oscillator Operation

A simple oscillator produces a periodic output, usually a voltage. So how can a circuit oscillate? Consider a feedback system in Figure 2.1 with transfer function *H(s)*, in order for steady oscillation to occur, the circuit must satisfy with Barkhausen criteria:

$$|H(s)| \geq 1 \tag{2.1}$$

$$\angle H(s) = 180° \tag{2.2}$$

These conditions are necessary but may not be sufficient to ensure oscillation [2]. Usually the loop gain of the system is twice to three times the required value [1].

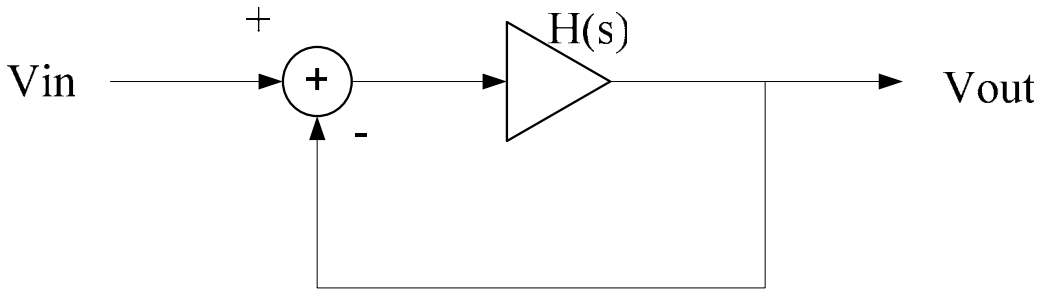


Figure 2.1 Simple Feedback System

CMOS oscillators are typically implemented as ring oscillators or LC oscillators, though there are many other types of oscillators. Another advantage of ring and LC

oscillators is that they can be easily modified to be able to change oscillation frequency for a given control voltage, thus making them prime candidates for VCOs.

2.2 Ring Oscillators

A ring oscillator consists of multiple gain stages within the loop. Each gain stage can be as simple as an inverter, or as complicated as a differential amplifier. Figure 2.2 shows a three-stage ring oscillator architecture.

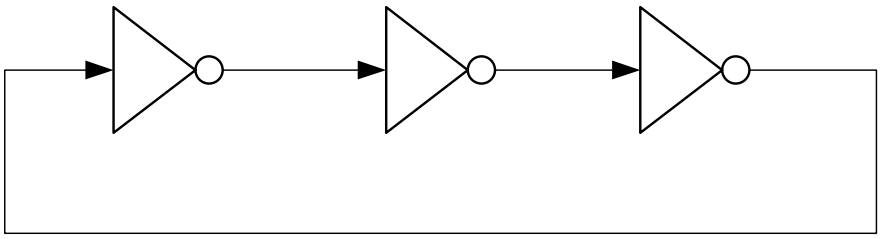


Figure 2.2 Three-Stage Ring Oscillator Architecture

The minimum gain per stage required can be easily derived from the transfer function of each stage and Barkhausen criteria. Assuming the transfer function of an inverting amplifier is

$$A = -\frac{A_0}{1+\frac{s}{\omega_0}} \tag{2.3}$$

Then the loop gain of the system is

$$H(s) = -\frac{A_0^{\,3}}{(1+\frac{s}{\omega_0})^3} \tag{2.4}$$

The system oscillates when the total phase shift equals 180˚ from Barkhausen criteria. Since we have a three stage system, then

$$\tan^{-1}\frac{\omega_{osc}}{\omega_0} = 60° \tag{2.5}$$

Solving for ω_{osc}, the frequency of oscillation

$$\omega_{osc} = \sqrt{3}\omega_0 \tag{2.6}$$

The minimum gain per stage such that the loop gain is equals to unity can be derived from Barkhausen criteria:

$$\frac{A_0^3}{\left[\sqrt{1^2 + \left(\frac{\omega_{osc}}{\omega_0}\right)^2}\right]^3} = 1 \tag{2.7}$$

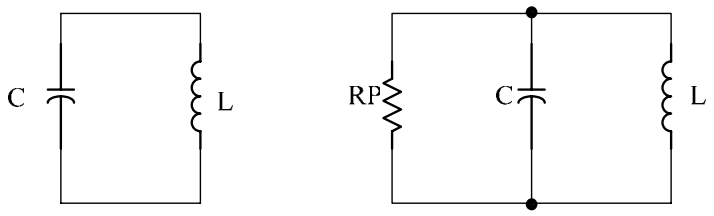
Solving for A_0 we have

$$A_0 = 2 \tag{2.8}$$

In summary, a three-stage ring oscillator can oscillate at $\sqrt{3}\omega_0$, where ω_0 is the 3-dB bandwidth of each stage, and requires a minimum gain of two per stage. Higher number of stage will result in less gain required per stage, but will oscillator at lower frequency, as evident in Barkhausen criteria.

2.3 LC Tank Oscillators

As monolithic inductors have appeared in CMOS and bipolar technologies in the past decade, the design of high frequency monolithic inductor based oscillator has become more and more important. Let us look at the basics of RLC circuits first.



(a) (b)

Figure 2.3 a) Simple LC Circuit in Parallel, b) Equivalent Parasitic Resistance in Parallel

As shown in Figure 2.3(a) an inductor *L* is placed in parallel with a capacitor *C*. The resonance frequency for this setup is

$$\omega_{res} = 1/\sqrt{LC} \tag{2.9}$$

At this frequency, the impedance of the inductor, $jL\omega_{res}$, and capacitor, $1/(jC\omega_{res})$, are equal and opposite, thus yielding an infinite impedance. However in real practices, inductors, and capacitors, suffer from parasitic resistive components, as shown in Figure 2.3(b). Let us define the quality factor of the inductor, Q, as

$$Q = \frac{L\omega}{R_s} \tag{2.10}$$

If we try to convert the inductor-resistor in series circuit in Figure 2.4(a) into the inductor-resistor in parallel form in Figure 2.4(b), as derived in [1], we get

$$L_p \approx L \tag{2.11}$$

$$R_p \approx Q^2 R_s \tag{2.12}$$

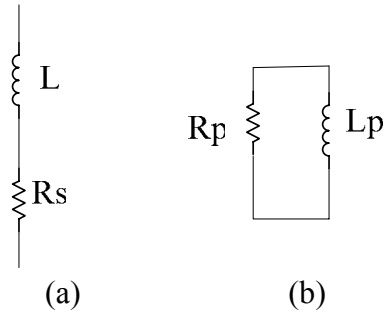


Figure 2.4 a) Inductor with Parasitic Series Resistance, b) Series Resistance Converted into Parallel Resistance

As we can see in equation 2.12, the quality factor of the inductor is very important in determining the amount of energy lost in the tank. Figure 2.5 shows a simple gain stage based on an LC tank.

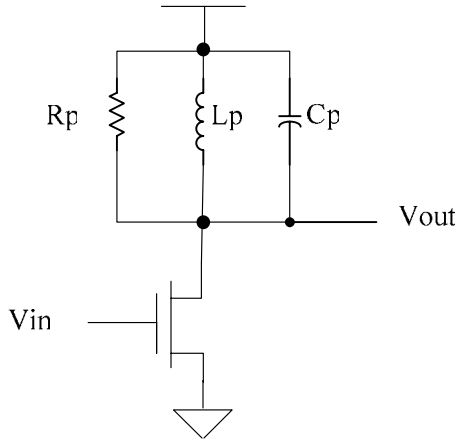
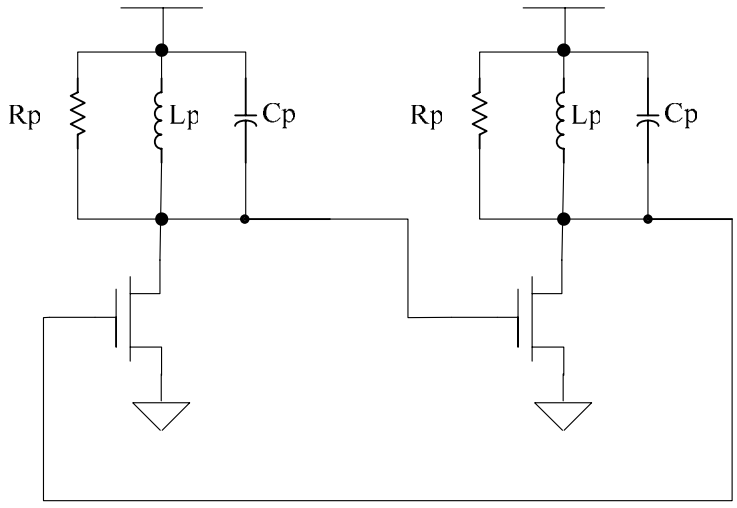
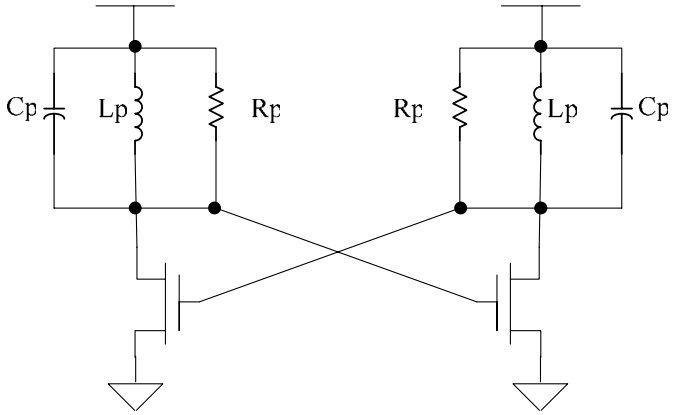


Figure 2.5 Simple RLC Gain Stage

At resonance, $jL_p\omega = 1/(jC_p\omega)$, and the voltage gain equals $-gm_1R_p$. However if we connect the output directly into the input, the total phase shift for this stage is approaching, but never reaches, 180˚. But if we put two gain stages in cascade, as shown in Figure 2.6(a), then the circuit oscillates, given the gain is large enough.



(a)



(b)

Figure 2.6 a) Cascade of Two Simple Gain Stages

b) Redraw of 2.6 a)

If we redraw circuit in 2.6(a) to 2.6(b), this type of oscillator is what we usually called cross-coupled LC tank oscillator. We can also convert the gain stage into a differential pair form by adding a tail current source, as shown in Figure 2.7. This oscillator is the fundamental form of LC tank based VCOs.

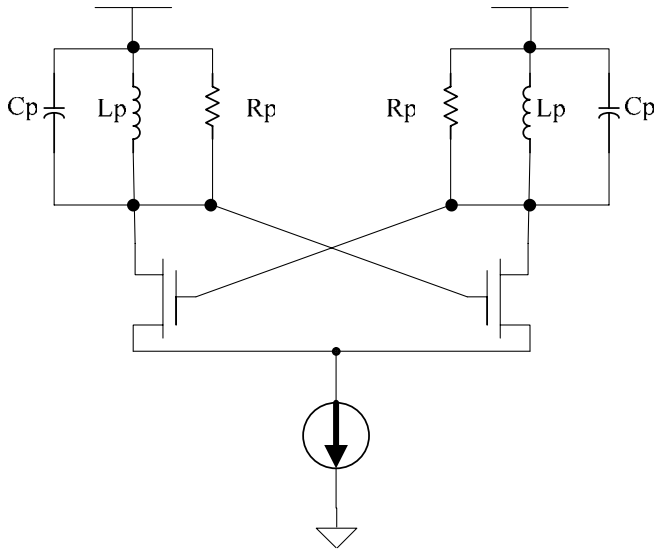
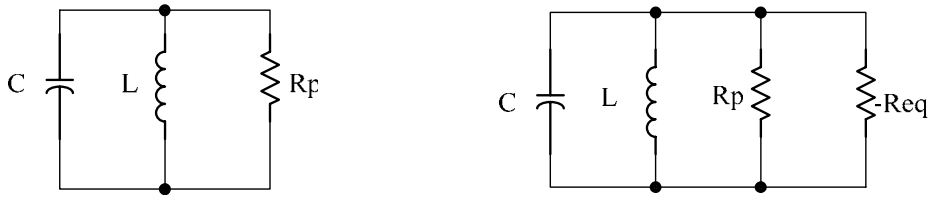


Figure 2.7 Differential Pair with RLC Loads and Tail Current Source

Another simpler way to look at how LC tank based VCO works is negative resistance. Figure 2.8 shows the concept.



(a) (b)

Figure 2.8 a) LC Tank with Parasitic Resistance in Parallel, b) LC Tank with Parasitic Resistance and Negative Resistance in Parallel

Figure 2.8(a) shows the components of our real LC tank. The resistance R_p is a lumped equivalent model of the non-idealities of the inductor and capacitor. The oscillation will not last forever on this tank because the resistor constantly dissipates energy from the tank. However, if we could somehow produce a negative resistor

that can supply the tank with more energy than the tank can dissipate, then the oscillation will sustain.

But how much negative resistance do we need? From Figure 2.8(b), we can see that in order for the overall circuit to have no positive resistance, the negative resistance, $-R_{eq}$, must be less than or equal to R_p so the parallel combination will produce a non-positive resistance. From Appendix A, the equivalent resistance looking into the drains of a crossed-coupled pair is approximately

$$R_{eq} \approx -\frac{2}{gm} \tag{2.13}$$

where gm is the transconductance of each of the NFET.

From Equation 2.13, we can see that in order for the LC tank based VCO to oscillate, we need to *increase* the transconductance of the crossed-coupled NFETs. The analysis using negative resistance method agrees on with what we analyzed before with Barkhausen Criteria, which is to increase the gain of each stage. By increasing the *gm* of each stage, we increased the gain of the stage but also reduced the negative resistance generated from the crossed-coupled pair, thus making $|R_{eq}|$ smaller compared to R_p.

Chapter 3 LC TANK VCO

Figure 2.7 showed a basic LC tank based oscillator, however, the oscillation frequency is not tunable. To make it tunable, let us first look at some of the capacitive devices found in common CMOS process today.

In today's CMOS process, high quality factor monolithic inductors exist in many different sizes, turns, and width. We can readily compute the inductance and Q of these inductors through Cadence and Z-parameter simulations. There are also a few different types of tunable capacitors, or varactors, such as the metal-oxide capacitor (MOSCAP) and hyper-abrupt junction varactor (HAVAR), which are available in many processes. These varactors vary the capacitance based on a different bias voltage, and they typically offer about 20 to 30 percent of tunable capacitance. The following section describes how we can use these varactors to achieve a voltage tuned oscillator.

3.1 LC VCO Circuit Topology

By replacing fixed capacitors with varactors and adding in a control voltage, Figure 3.1 shows the commonly used LC VCO topology utilizing varactors.

The varactors in figure 3.1 are represented as VAR. Keep in mind that the varactors are actually PN junctions so they must be reverse biased in order for them to change their capacitance and avoid DC current. The DC voltage at nodes TANK_OUT and TANK_OUT_BAR is very close to VDD because the inductors serve as short circuit to VDD in DC, minus any parasitic resistance the inductors might have. To keep the varactors reversed biased, the VCO control voltage, Vctrl, can vary from ground to VDD.

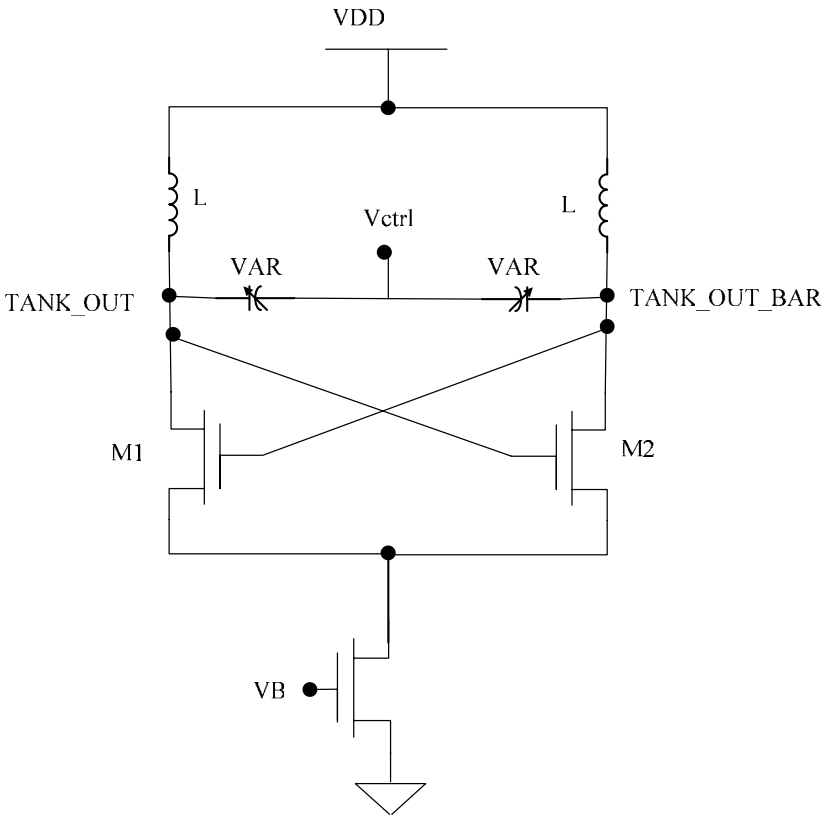


Figure 3.1 Common LC VCO Topology with Varactors

In Figure 3.1, the tail current source is implemented with an NFET with a constant bias voltage, VB. The amount of this current determines the power consumption and oscillation amplitude. The higher the oscillation amplitude will lead to better the phase noise, as predicted by Leeson's Equation:

$$PN(\Delta f) = kTR\frac{F}{V_0^2}(\frac{f_{osc}}{Q\Delta f})^2(1+\frac{f_c}{\Delta f}) \qquad (3.1)$$

As we can see from Leeson's Equation, the oscillation amplitude, V_0, plays a significant role in determining phase noise. However because the low frequency flicker noise, or *1/f* noise from the current source, which will be up-converted [3], and higher *1/f* noise of the N-channel device in general, a current source implemented by an NFET will produce more phase noise than a current source

implemented by a PFET. Thus, some people prefer to implement the VCO in the following way to reduce phase noise:

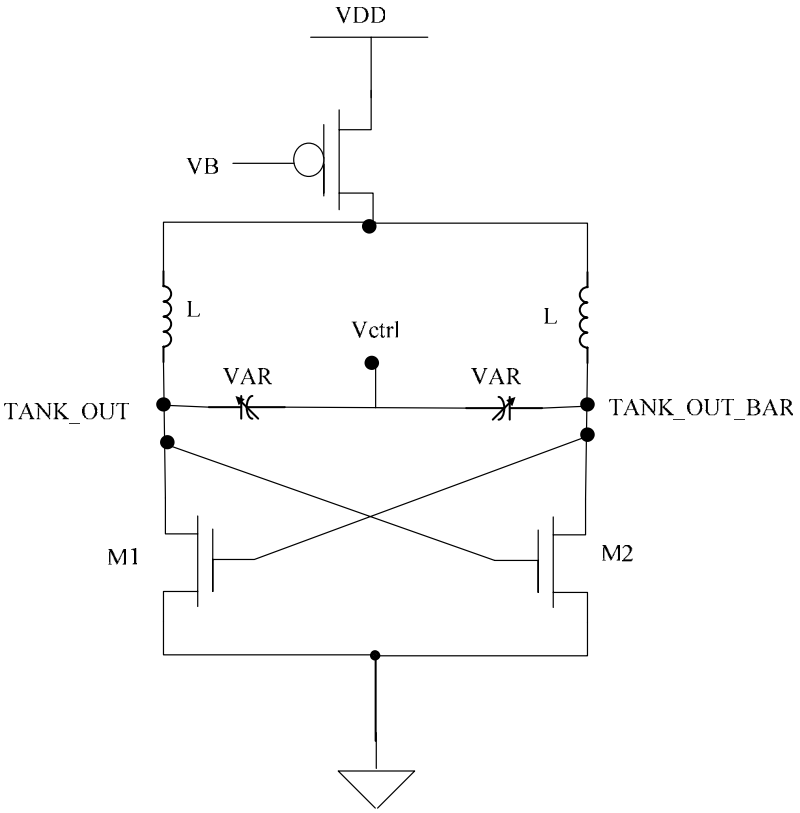


Figure 3.2 LC TANK VCO with PFET Current Source

Figure 3.2 shows the tail current being placed near VDD by a PFET. Although this topology reduces phase noise caused by the higher *1/f* noise of the NFET, however it will cause another problem. The DC voltages at the tank outputs are not at VDD due to the headroom voltage from the PFET tail current. Thus the control voltage, Vctrl, can no long vary from ground to VDD or it might cause the varactors to be in forward bias region and conduct DC current. So the control voltage has a narrower range and will cause the tuning range to shorter.

3.2 Proposed LC VCO Topology

In the proposed VCO topology, as shown in Figure 3.3, the VCO utilizes both the low *1/f* noise aspect of the PFET current source and able to maintain the wide range of the control voltage.

The tail current device is still below the cross-coupled NFET, however it is implemented using a PFET. This may not look like a current source, as the node V_p is the source of the PFET and the current will vary as the oscillation occurs, however, closer examination reveals that a PFET current device is no worse than the traditional NFET version.

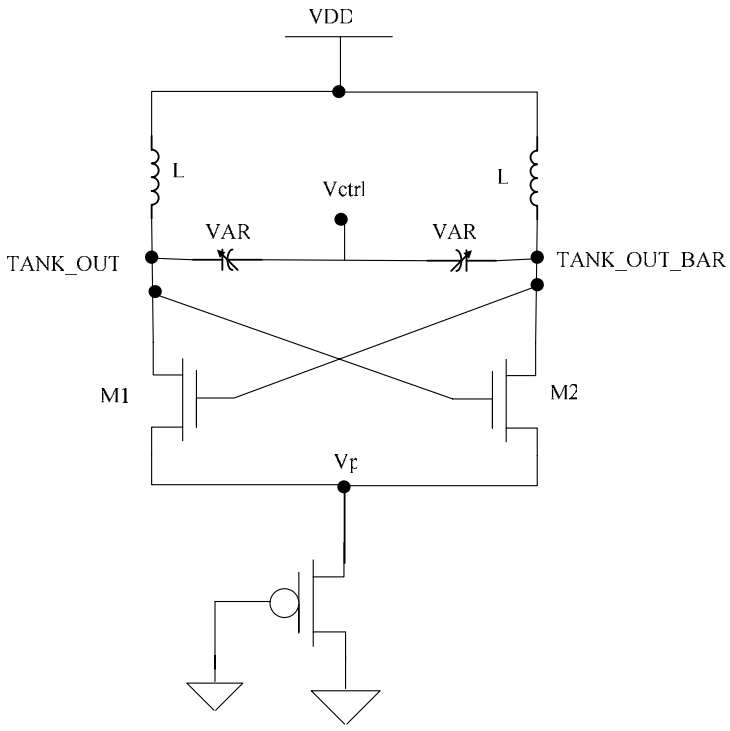


Figure 3.3 Proposed LC VCO Topology

First, as the channel length of modern technology gets shorter and shorter, channel length modulation effect on the drain current become more and more visible. Even an NFET current source with drain attached to the high frequency node V_p will cause the current to change as oscillation occurs. Although the PFET version will cause more current change due to square law in V_{GS}, the overdrive voltage in modern VCOs are small because low supply voltage, and the high frequency oscillations at node V_p can be filtered out by adding a large decoupling capacitor at node V_p.

Second, there is feedback between node V_p and V_b in the NFET current source due to gate to drain capacitance will affect the overdrive voltage V_{GS} of the current source, and it will cause the current to change as the VCO oscillates. However in the PFET current device, there is no node V_b—the gate of the PFET can be directly tied to ground, thus ignoring the effects of the parasitic capacitance.

Third, the PFET version saves the complexity and area needed for biasing. The NFET current source will need a good bias voltage since there isn't much headroom in modern supply voltage to keep the NFET saturated. The PFET version is always saturated as the drain and gate are both tied to ground.

From above arguments, the PFET current device will not perform any worse than an NFET version in terms of transient current stability. Since both the gate and drain of the PFET is tied to ground, the bias current can be designed from the sizing of the PFET, and extra-large PFET device will cause less harm than a large NFET due to no C_{GS} feedback.

3.3 Quadrature LC VCO

Quadrature oscillators produce outputs having a phase different of 90˚. This is very useful in some communication systems where the modulation scheme utilizes both in-phase and quadrature components and can be demodulated easily.

The principle of quadrature generation is to couple two identical oscillators such that they operate with a 90˚ phase shift. The concept behind this is that if we injection a signal into an oscillation that has the same frequency, then we can, and will, shift only the phase of the output of the oscillator. However, we only want to inject a portion of each oscillator's output into the other. As described in [1], if we make the transconductance of the injection mechanisms equal and opposite, or anitphase coupling, then we can have the outputs of the two VCOs 90˚ out of phase.

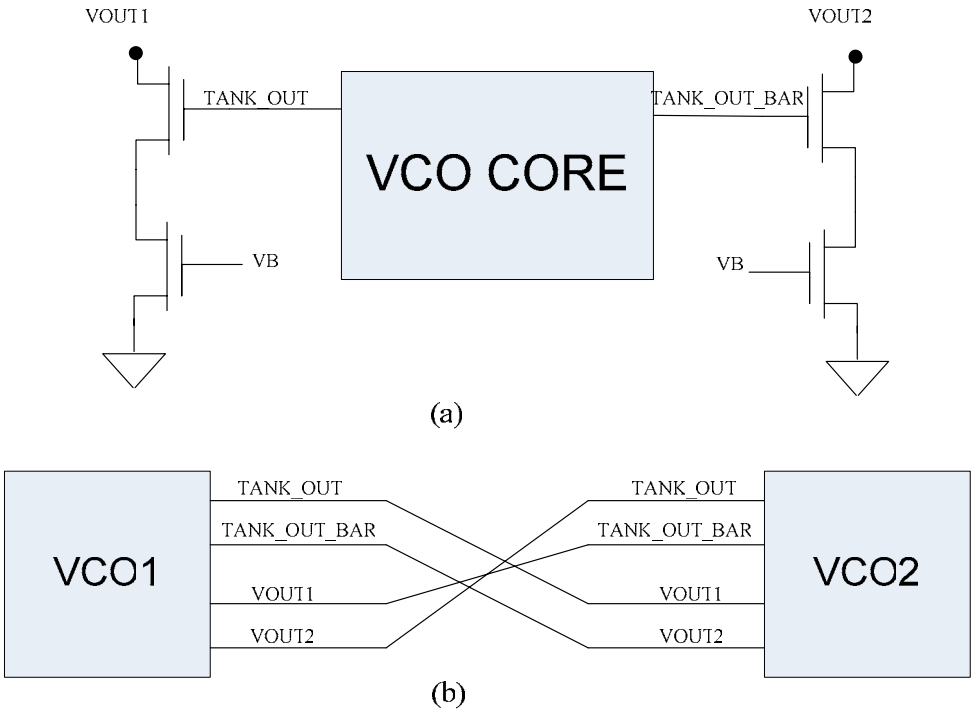


Figure 3.4 a) Quadrature VCO Injection Mechanism, b) Quadrature VCO Injection Topology

The injection mechanism used in Figure 3.4(a) consist of a DC biased NFET current source and an NFET device whose drain connects to one of the output of the other VCO. This injection mechanism is used for each of the VCOs outputs. This kind of single-ended design provides better isolation between the outputs of the VCOs compared to a differential injection mechanism, though it consumes slightly more power. The outputs of the injection mechanism, Vout1 and Vout2, will be connected to the tank outputs of the second VCO, as shown in Figure 3.4(b)

3.4 Symmetric Inductor VCO

In some CMOS process, such as IBM 0.18μm CMOS process, contains symmetric inductors, or differential inductors. The single symmetric inductor of inductance L can replace two asymmetric inductor of inductance L/2, and thus saves about 50% of total layout area due to spacing required between asymmetric inductors. Symmetric inductors also provide higher Q than single-ended inductor [4] when driven by differential stimuli.

In the application of LC tank VCOs, the symmetric inductor can be best utilized. The LC VCO has two differential outputs, and each output has an inductor connected to a DC node, such as VDD. We can replace the two regular inductors with a larger symmetric inductor and bias the center tap of the symmetric inductor to the DC node, as shown in Figure 3.5 below.

The design in Figure 3.5 provides better phase noise, less area, but the tuning range of the VCO may be slightly decreased. This is due to the interwinding or fringe capacitance between the segments of the symmetric inductor, where as in regular inductor, these fringe capacitances can be ignored [1]. However due to the layout

parasitic capacitance resulted from cross coupling of the asymmetric inductors, the fringe capacitance of the symmetric inductor is ignorable.

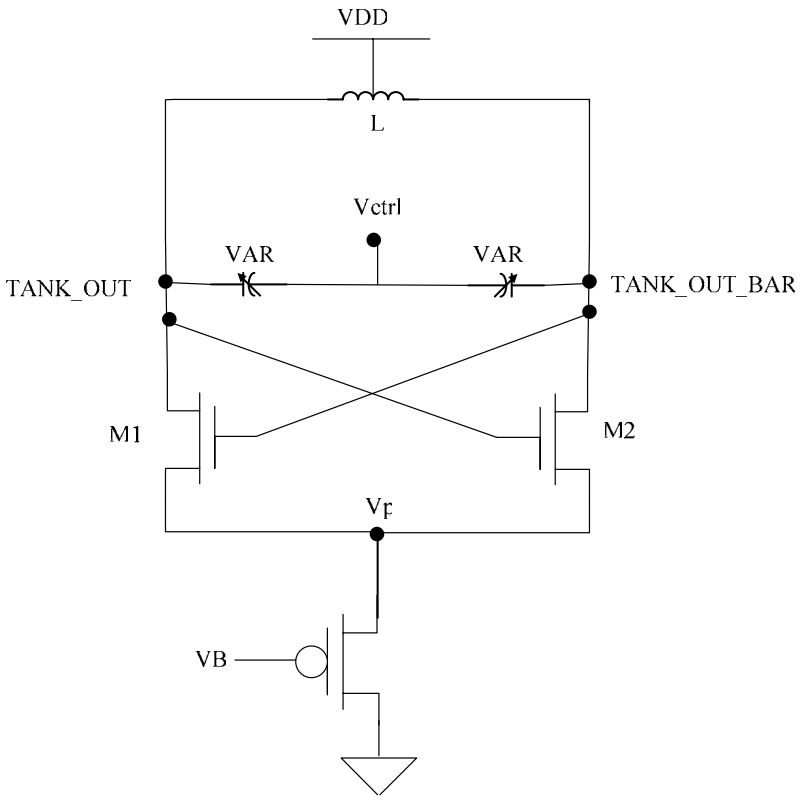


Figure 3.5 Proposed LC VCO Topology with Symmetric Inductor

3.5 Layout Considerations

The layout of LC tank VCOs can get complicated. Since the VCO oscillate at very high frequency, the any parasitic capacitances on the tank will greatly reduce the oscillation frequency and tuning range. To maintain the Q for the inductors, the inductors must be placed at least several tens of microns apart from each other—the actual distance differ from technology, to avoid substrate noise coupling. The wiring resistance will reduce the Q of the inductor and thus cause more phase noise. As a

result, the use of low resistance metal wiring for high frequency paths is highly recommended.

To minimize the effect of parasitic capacitances on the tank, the tank layout should be done first and prioritize high frequency paths layout. In the case of regular inductors, where the inductors must be places a large distance apart and the transistors needs to cross, the wiring of these distances should be done on the top level metal with thick wires to minimize wiring resistance. In the case of symmetric inductors, the wiring resistance is minimal. Expect around 10% extra capacitance and 10% reduction in inductance on the tank after layout of regular VCOs, and more capacitance is expected for quadrature VCOs since the tank needs to drive the capacitance of the extra injection mechanism.

The DC nodes should be done after the high frequency paths. It is very important to keep the potential difference between the ground node and substrate node as small as possible by placing as many substrate contacts as the technology allows on the ground node. The VCO control voltage node should have a large decoupling capacitor on it to minimize effect of DC fluctuation and its effect on VCO oscillation frequency.

3.6 LC VCO Simulation Results

Two designs were taped out using IBM 0.18μm CMOS technology: VCO and quadrature VCO design used single-ended inductors and symmetric inductors. These VCOs are targeted for 5.8GHz WiMAX applications. The simulation results are discussed in the following sections, but first let us look at the inductor selection process.

3.6.1 Inductor Selection

As discusses before and in Leeson's Equation, the quality factor of inductors has a very important role in determining the phase noise. So it is important that we pick inductors that have high Q. Fortunately, in Cadence, there are ways to determine the Q of an inductor through Z parameter simulation. Figure 3.6 shows the setup.

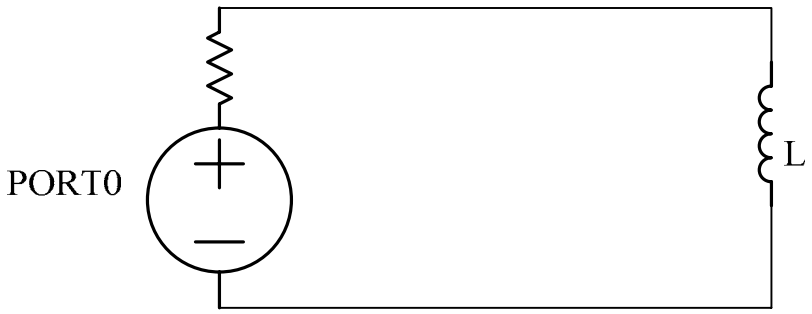


Figure 3.6 Inductor Z Parameter Simulation Setup

Recall from Equation 2.10 that Q is defined to be

$$Q = \frac{L\omega}{R_s} \tag{3.1}$$

In Z parameter simulation as a function of frequency, the real part of Z11 is the series resistance of the inductor, and the imaginary part of Z11 is the actual inductance. So we can computer the Q in the following method:

$$Q = \frac{imag(Z11)}{real(Z11)} \tag{3.2}$$

With this method, we easily can determine the Q of an inductor and design the VCO such that the Q is highest at the frequency of interest. Figure 3.7 shows the Q simulation result of the inductor and symmetric inductor that were used in the design.

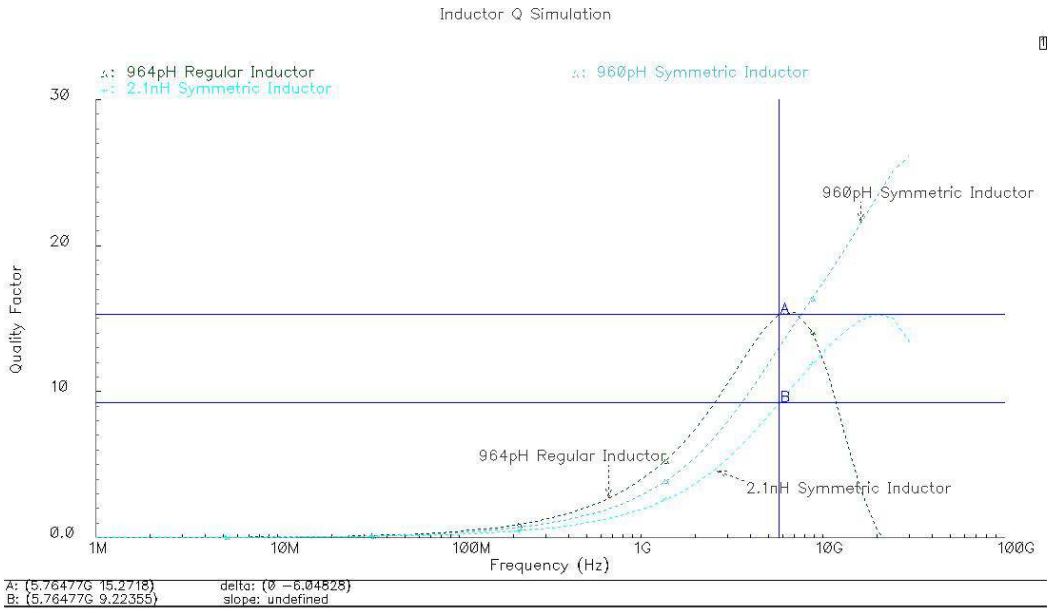


Figure 3.7 Inductor Q Simulations

The Q is around 15 for the regular inductor and 12 for the same inductance symmetric inductor, at 5.8GHz. However, because the symmetric inductor needs to double in size, as it takes over two regular inductors, the Q drops to 9 for symmetric inductor with twice the inductance. This lower Q of the symmetric inductor will hurt some phase noise performance, but as we can see in the Q simulation, the symmetric inductors exhibits much higher Q at higher frequencies. As a result, the symmetric inductors are better for high frequency VCOs.

3.6.2 50 Ohms Output Buffer Design

The output buffers are needed so that they can drive a 50-Ohm off-chip probe, when the hardware is tested. The buffer design is simple, as shown in Figure 3.8:

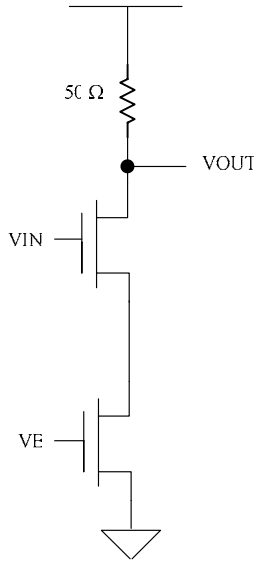


Figure 3.8 50 Ohms Output Buffer Design

Again, singled-ended topology was chosen as compared to differential topology. This is mainly to avoid the inter-coupling between the differential outputs due to parasitic capacitance of the transistors.

3.6.3 Regular VCO Design Simulation Results

Figure 3.9(a) and 3.9(b) shows the topologies for regular LC tank VCO using single-ended and symmetric inductors, respectively. In the final design, de-coupling capacitors were added in to maintain the DC signal integrity.

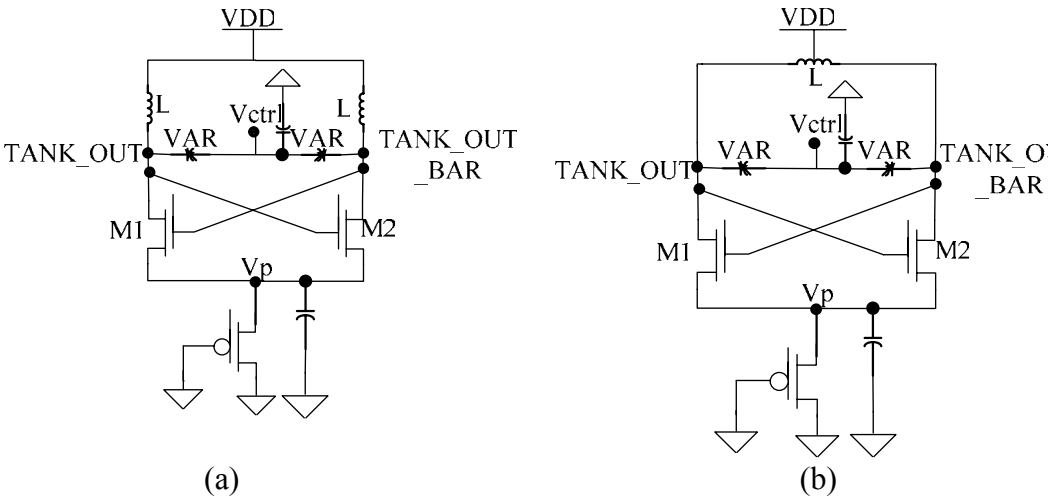


Figure 3.9 a) Final LC VCO Topology with Regular Inductors, b) Final LC VCO Topology with Symmetric Inductor

The designs were simulated through Cadence Spectre simulator, laid out, and extracted with parasitic capacitance and resistance. Figure 3.10 shows the layout photo.

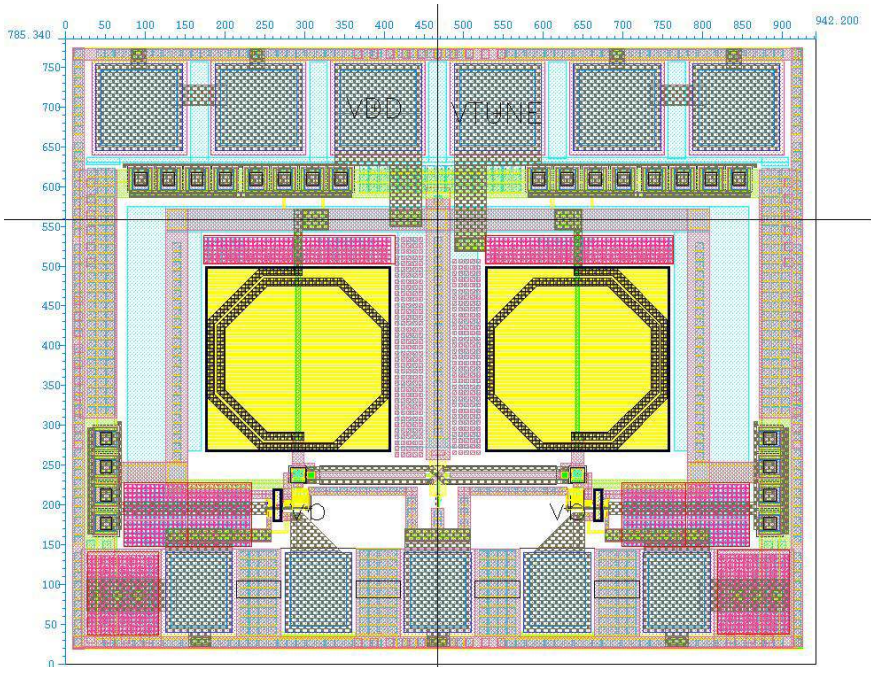


Figure 3.10 a) VCO with Regular Spiral Inductor Layout

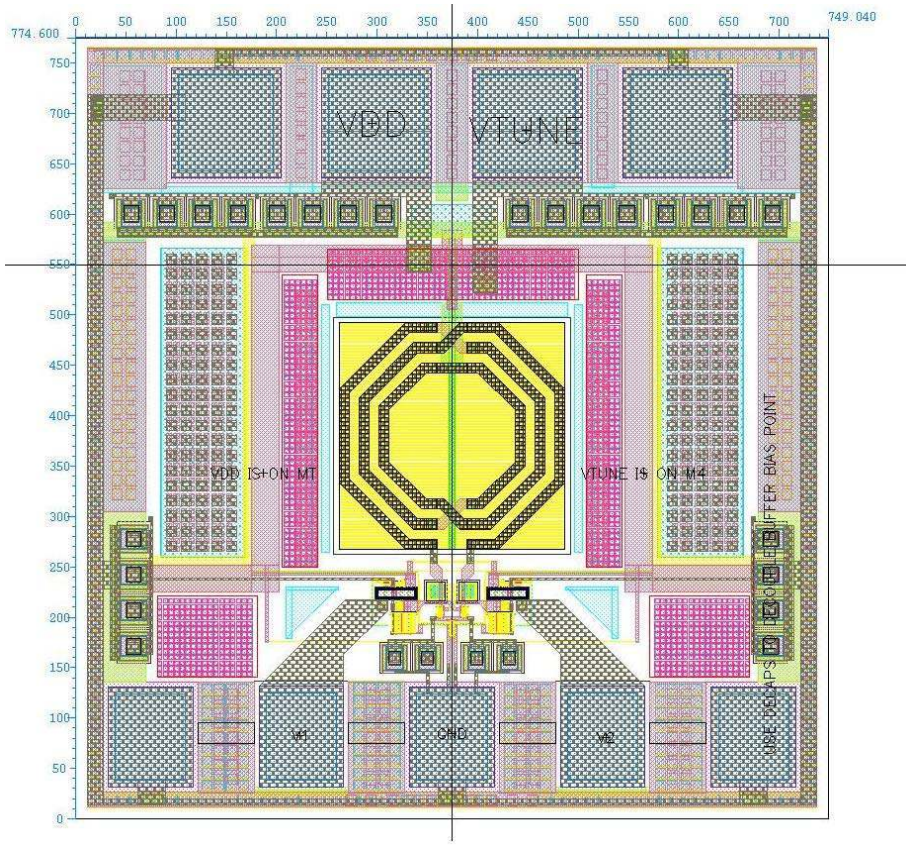


Figure 3.10 b) VCO with Symmetric Inductor Layout

The inductors are obviously taking up the most amount of space in the layout, except for the array of bond pads, and the symmetric inductors in 3.10(b) obviously saved a large amount of space when compared to the regular inductors. Figure 3.11(a) and 3.11(b) shows the transient and phase noise extracted simulation results with parasitic resistances and capacitances of the VCO with regular and symmetric inductor, respectively.

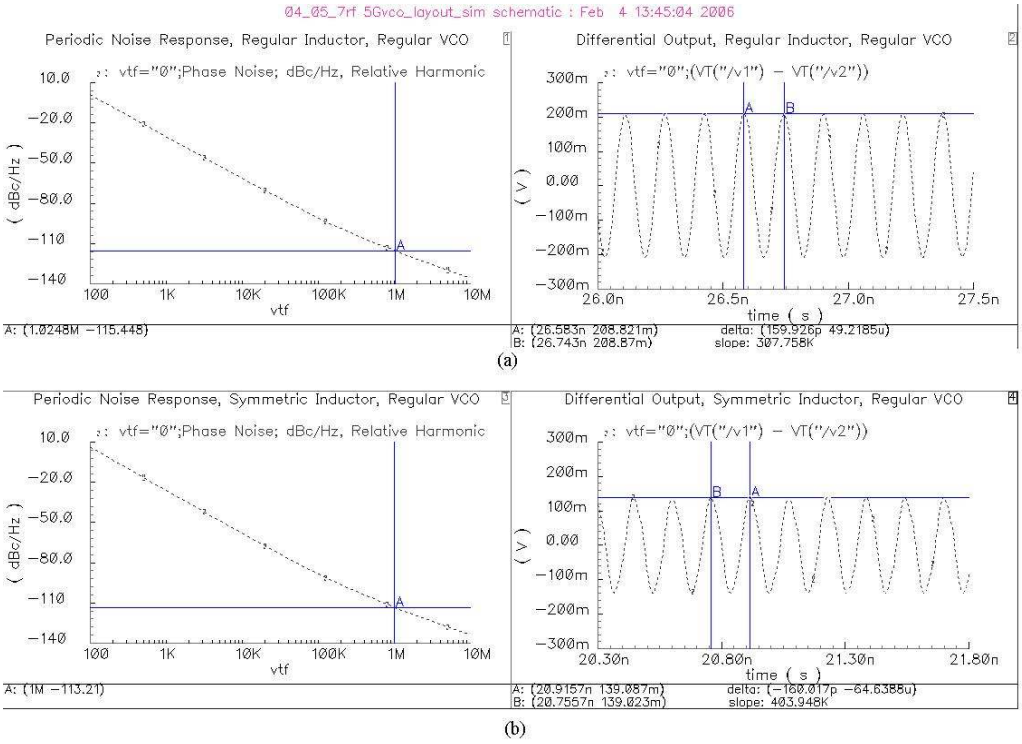


Figure 3.11 Extracted Simulation Results of the VCO at Maximum Oscillation Frequency. a) Regular Inductor, b) Symmetric Inductor

Table 3.1 summarizes the extracted simulation.

Table 3.1 Summary of LC VCO Results

Criteria	**VCO with Regular Inductor**	**VCO with Symmetric Inductor**
Oscillation Frequency/Tuning Range	5.36 GHz ~ 6.36 GHz	5.27 GHz ~ 6.4 GHz
Phase Noise at 1MHz Offset at Max Oscillation Frequency	-115.5 dBc/Hz	-113.2 dBc/Hz
Differential Oscillation Amplitude at Max Oscillation Frequency	410 mV	280 mV
Power Consumption with Buffers at Max Oscillation Frequency	12.4 mW (6.2 mA current at 2V supply)	9.2 mW (5.1 mA current at 1.8V supply)
Figure of Merit (FOM)	180dB	180dB
Core Layout Area	$0.35mm^2$	$0.19mm^2$

The symmetric inductor seems to be the better choice of the two designs—it saved both area and power. It is true that the symmetric inductor showed slightly more phase noise than the regular inductor design, which agrees with the Q simulation, but the overall Figure of Merit (FOM) did not decrease due to the savings in power consumption. The widely used FOM for VCOs is defined below:

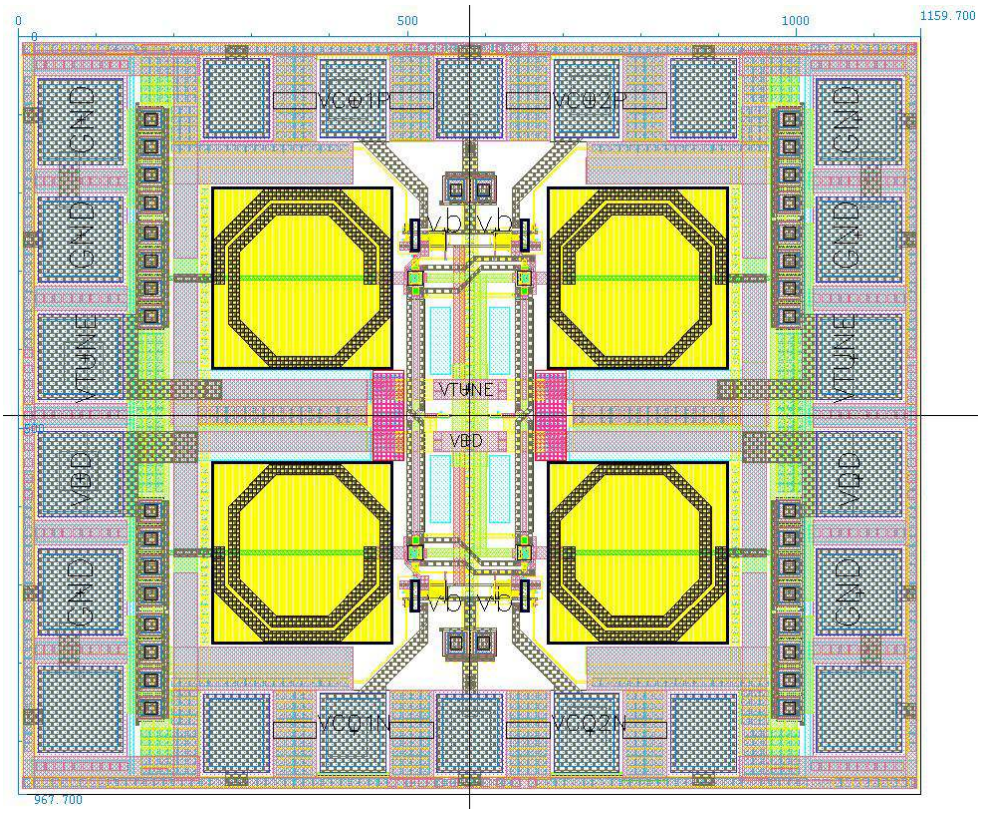
$$FOM = \left(\frac{f_{osc}}{\Delta f} \right)^2 \cdot \frac{1}{P_{DC} \cdot PN} \tag{3.3}$$

Where f_{osc} is the oscillation frequency, Δf is the offset the phase noise is measured at, P_{DC} is the DC power consumption in mW, and PN is the phase noise. Overall, both designs compares favorably with other designs in literature.

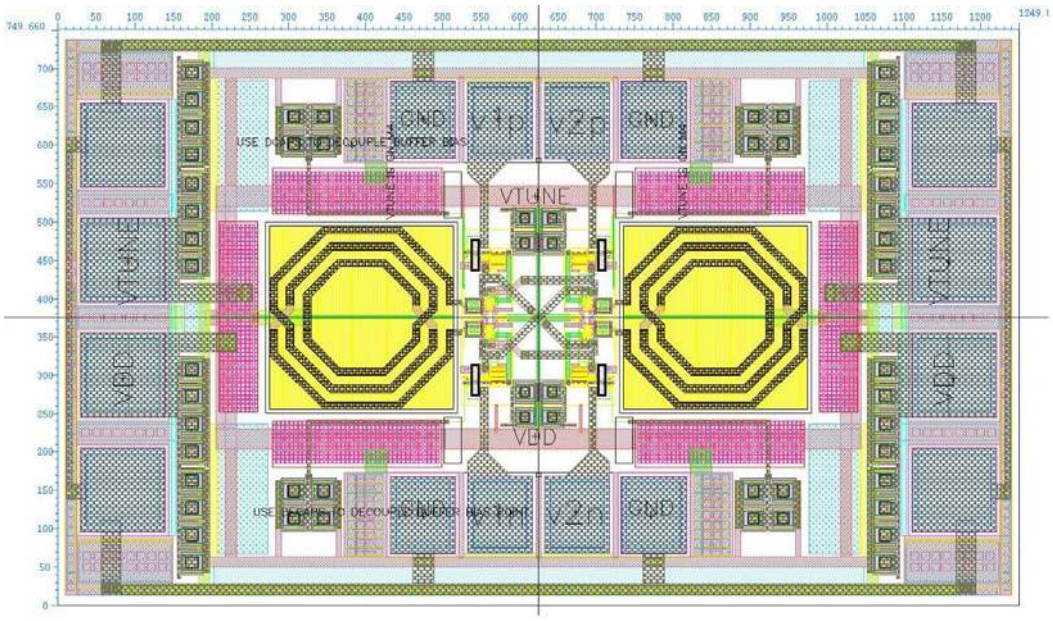
3.6.4 Quadrature VCO Design Simulation Results

Figure 3.4 showed the quadrature VCO injection topology and injection mechanism. The VCO core used is the same as the regular VCO.

The quadrature designs were also simulated through Cadence Spectre simulator, laid out, and extracted with parasitic capacitance and resistance. There are almost twice as much parasitic capacitances in this design because the extra injection mechanism and longer metal routing. Figure 3.12 shows the layout photo of the quadrature VCOs.



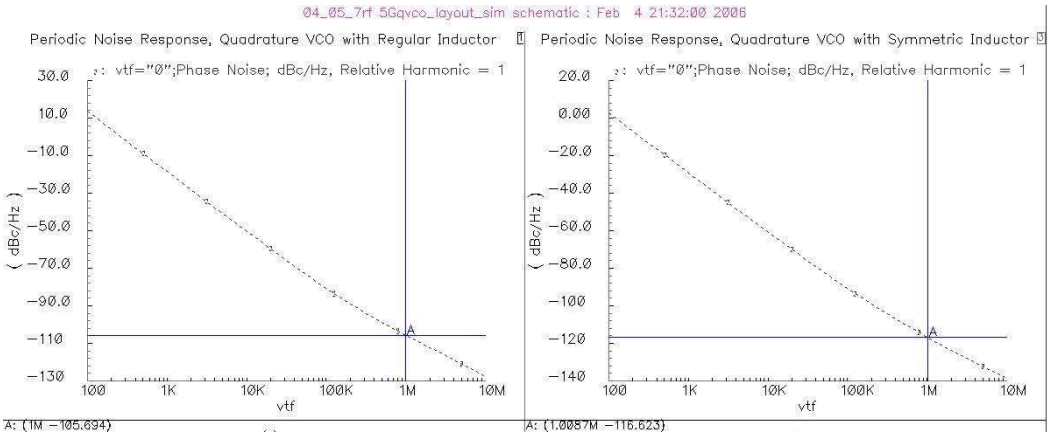
(a)



(b)

Figure 3.12 a) Quadrature VCO with Regular Spiral Inductor Layout, b) Quadrature VCO with Symmetric Inductor Layout

The phase noise simulation results for regular and symmetric inductors are shown in Figure 3.13 (a) and (b), respectively.



(a) (b)

Figure 3.13 Quadrature VCO Phase Noise Simulation Results for a) Regular Inductor, b) Symmetric Inductor

Again, the use of symmetric inductors saved a large amount of area, and in the case of quadrature VCO, improved the phase noise by about 11dB. This is due to the layout complexities of the quadrature VCO involving four inductors. The wiring resistances and capacitance contributed a lot to the phase noise. In addition, due to these parasitic resistances and capacitances, the quadrature outputs are not exactly 90˚ out of phase. Figure 3.14 shows the differential output of the symmetric inductor VCO.

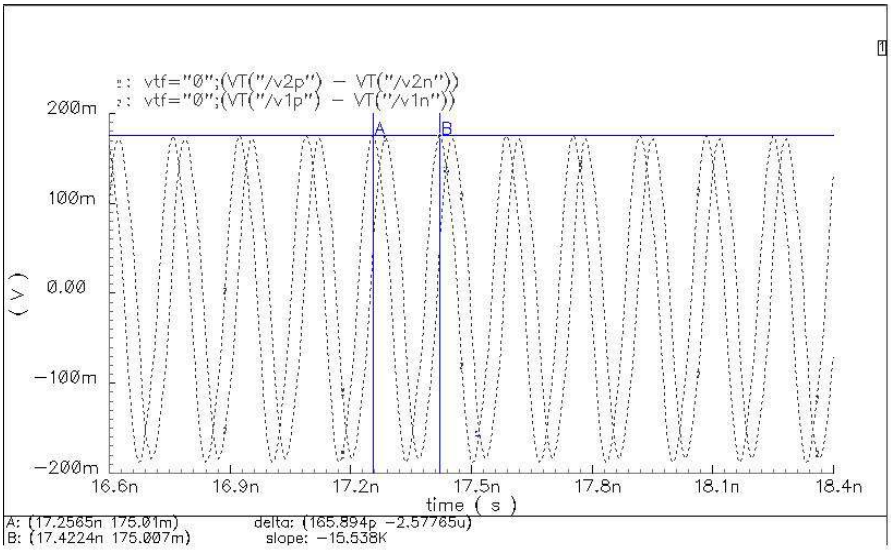


Figure 3.14 Quadrature Outputs of the Quadrature VCO

As observed in Figure 3.14, the outputs are not exactly 90˚ out of phase. This is caused by the wiring parasitics in the layout which affects the *Gm* of the injection mechanism circuit. A work around for this problem is to purposely bend the routing wires so that all four outputs endure the same amount of parasitic resistances and capacitances.

The summary of results of the quadrature VCO designs are listed in Table 3.2.

Table 3.2 Summary of LC Quadrature VCO Results

Criteria	**Quadrature VCO with Regular Inductor**	**Quadrature VCO with Symmetric Inductor**
Oscillation Frequency/Tuning Range	5.48 GHz ~ 6.34 GHz	5.23 GHz ~ 6.05 GHz
Phase Noise at 1MHz Offset at Max Oscillation Frequency	-105.69 dBc/Hz	-116.62 dBc/Hz
Differential Oscillation Amplitude at Max Oscillation Frequency	400 mV	310 mV
Power Consumption with Buffers at Max Oscillation Frequency	26mW (13mA at 2V supply)	19.8mW (11mA at 1.8V supply)
Figure of Merit (FOM)	168dB	179dB
Core Layout Area	$0.53mm^2$	$0.35mm^2$

The complexity of layout of the regular inductor becomes obvious here in the quadrature VCO case. The four regular inductors must be far apart from each other to reduce the substrate noise coupling. The lengthy wirings that are need to cross couple inside the same VCO and injection between the VCOs causes a substantial increase in noise, as appeared in the phase noise result of the regular quadrature VCO. The symmetric inductor is obviously a better choice here, as it saves both area and power, and produces a better phase noise, even with lower Q in the inductor itself.

3.7 LC Tank VCO Summary

In the above sections, LC tank VCOs using regular and symmetric inductors were demonstrated. These VCOs oscillate around center frequency of 5.8GHz with tuning range of around 1GHz. Quadrature versions of these VCOs were also demonstrated. They also operate at 5.8GHz but with a slightly less tuning range than their regular VCO counterparts. The use of symmetric inductors greatly decreased the layout area, saved over 25% of power, and improved the FOM by 10dB for the quadrature VCO.

This design is very comparable with other published VCOs around the same frequency. This design has superb tuning range compared to other designs, which will make this VCO very robust against temperature and process variations. Table 3.3 shows the comparison.

Table 3.3 Comparison Between LC Tank VCOs

	Technology	Frequency/Tuning Range	Power/Supply	Phase Noise at 1MHz Offset	Note
This Work, Simulation	0.18um CMOS	5.27~6.4 GHz	9.2 mW @ 1.8V Supply (with Buffers)	-113.2 dBc/Hz	Symmetric Inductor
This Work, Simulation	0.18um CMOS	5.23~6.05 GHz	19.8 mW @1.8V Supply (with Buffers)	-116.6 dBc/Hz	Symmetric Inductor, Quadrature
[5]	0.18um CMOS	8GHz ± 250MHz	30mW @ 4V Supply (with Buffers)	-117 dBc/Hz	Transformer, Quadrature
[6]	0.18um CMOS	4.6~5 GHz	4.5mW @ 1.5V Supply (Core only)	-120 dBc/Hz	Differential Colpitts
[7]	2um InGaP/GaAs HBT	4.39 GHz ± 6%	42mW @ 3V Supply (with Buffers)	-117.8 dBc/Hz	

Chapter 4 RING VCO

Chapter 3 described the LC tank based VCO. Now let us look at another popular form of VCO, ring VCOs, commonly found in microprocessors, where monolithic inductors are not readily available in high quality format.

4.1 Basic Single-ended Ring VCO topology

From section 2.2 we know that a simple chain of odd number of digital inverters can oscillate, but that oscillation frequency is fixed. How do we make it such that we can change the oscillation frequency via a voltage? We will look at several different VCO cell topologies and their pros and cons.

4.1.1 Current-Starved Inverter

The simple way to control the charge and discharge time of an inverter is to control the current through the inverter, via a voltage controlled current source, as depicted in Figure 4.1. This current source is driven by the control voltage, Vctrl, and the current will determine the charge up and discharge time of the inverter. This topology is called current-starved inverter, as the regular inverter is short of the current they are normally allowed to consume.

With correct sizing and current levels, an odd number of stages of these current-starved inverters can make a decent VCO. This design is simple and the oscillation frequency can achieve reasonably fast, and tuning range is great, due to the square-law change in current levels in the footer device. We can size the footer device wider so that it doesn't affect the output swing much. However there are several problems with this design. First, the inverter doesn't work at very low bias voltages, such as zero, when the current in the inverter is been shut off. Second, the DC level of the VCO output is not constant; this can cause problems at high frequency when

trying to amplify the VCO output to full swing. Third, the output of each stage drives two gates, which limits the maximum oscillation frequency.

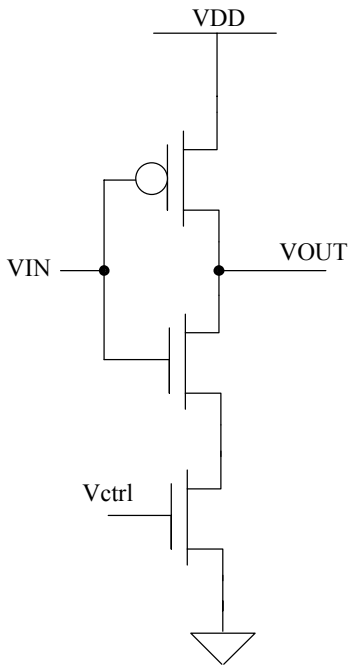
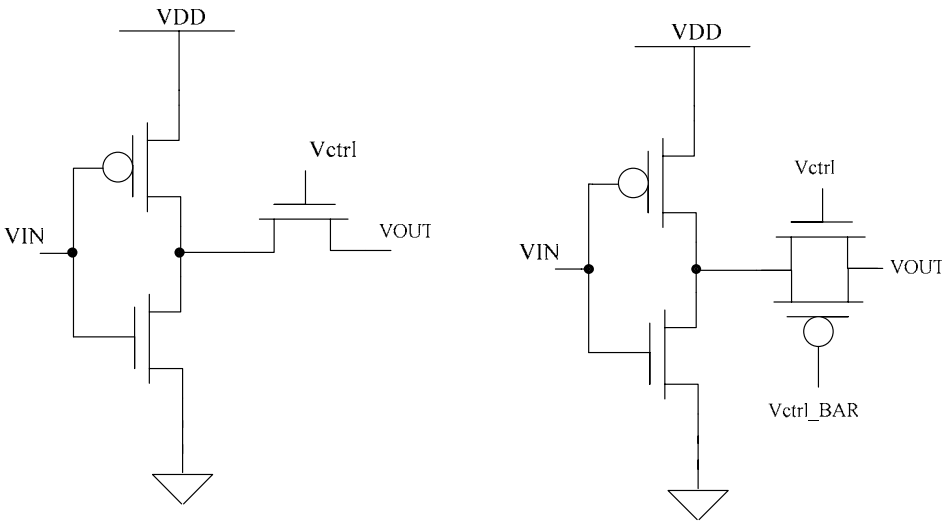


Figure 4.1 Current Starved Inverter

4.1.2 Inverter with Pass/Transmission Gate

Instead adjusting the current level through the inverter, we can also adjust the charge up and discharge time of the inverter by putting a pass gate as a delay and adjust this delay at the output of the inverter, as shown in Figure 4.2(a).



(a) (b)

Figure 4.2 a) Inverter with Voltage Controlled Pass Gate, b) Inverter with Voltage Controlled Transmission Gate

In this pass gate design, the control voltage, Vctrl, adjusts the pass gate strength and thus varies the charge up and discharge time of the delay cell as a whole. This is very effective in adjusting the delay and thus can control the frequency of oscillation very well, however, this design has several drawbacks. First, the maximum frequency of this design is very low, this is due to the extra capacitance and extra delay from the pass gate even at the maximum control voltage. Second, the output will not be at full swing due to a threshold drop across the pass gate. Third, the output of the inverter will be distorted when the control voltage is lower than the threshold of the pass gate. To solve some of the problems, we can replace the pass gate with a transmission gate, as shown in Figure 4.2(b). This does take care of the problem of inverter not function correctly when control voltage is low, however generating an exact inverted version of Vctrl will be another complexity.

The advantage of singled-ended ring VCO design is its simplicity and high output swing, when compared to differential design. However differential designs can have a faster oscillation frequency due to its current mode logic. Let us look at several traditional differential designs.

4.2 Basic Differential Ring VCO topology

Differential VCO cells can usually oscillation than the singled ended versions and noise performance, due to their current mode logic and native differential noise rejection. In theory, the minimum stages required for oscillation of differential cell design is two, as you can cross the outputs of the second cell to get additional 90˚ phase shift. Let us start with the very basic differential amplifier as the VCO cell.

4.2.1 Differential Pair with Resistive Loads

Figure 4.3 shows the basic differential amplifier with resistive loads, while the bias current is controlled by the VCO control voltage.

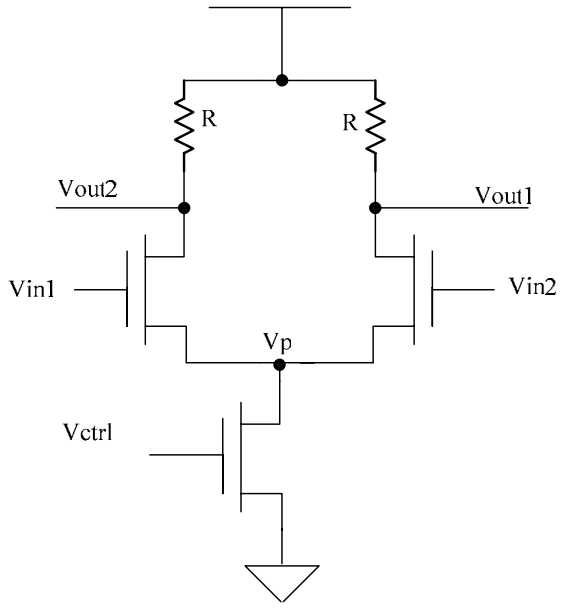


Figure 4.3 Differential Amplifier with Resistive Loads

In this amplifier, the oscillation frequency can achieve very fast due to the current mode logic in the differential pair. The major problem with this design is that the tuning range is very small. The bias current is determined by the tail current source, and it is controlled by the VCO control voltage only. Given the design is current mode logic and resistive load is constant, then as long as the differential pair has enough current to operate, giving extra currents to the differential pair will not dramatically speed up or slow down the operation. Also, a change in the control voltage will not change the current level in its full effect due to node Vp will counter-adjust itself due to the constant load R. As a result the tuning range of this design is extremely low when compared to other ring oscillators. Current reported tuning range in literature is around 12% only.

4.2.2 Differential Pair with PFET Loads

In this design, we replace the resistors with DC biased PFET devices, and biased as shown in Figure 4.4.

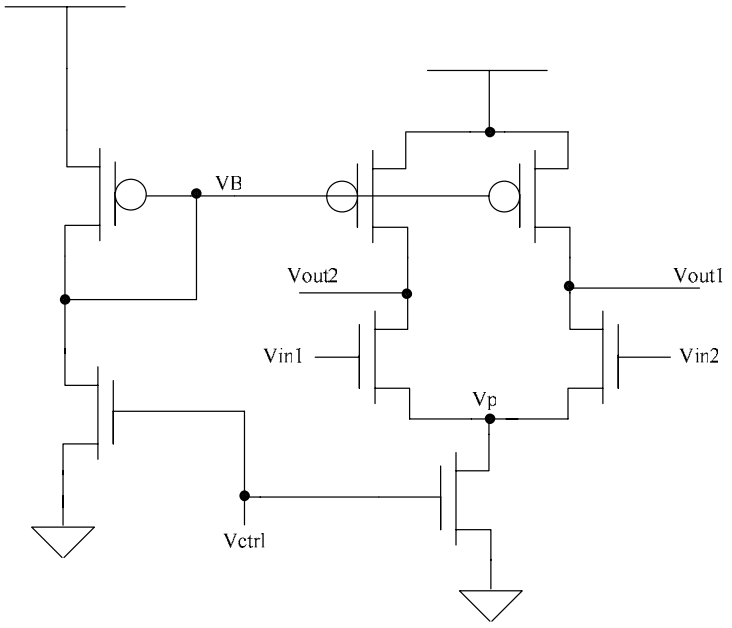


Figure 4.4 Differential Amplifier with PFET Loads

The goal of this design is to increase the tuning range. Consider the PFET device as voltage controlled resistors and the bias circuit VB as an inverted version of Vctrl. As the VCO control voltage changes, the resistance of the PFET device also changes, thus varying the gain of the differential pair. Additionally, node Vp will not adjust itself as much as in Figure 4.3 due to a variable load. This method can increase the tuning range dramatically, close to the tuning range of current starved inverters. The drawbacks of this design are the small output swing and varying DC offset at the output, as current mode logic tends to produce much smaller swings.

In summary differential VCOs tends to be faster than their singled-ended parts due to their current mode logic nature. However differential VCOs have smaller output swing, and suffers the same problems of not being able to operate at low bias voltage and varying DC offset in the singled-ended versions.

In the next proposed VCO topology, we try to maintain the maximum oscillation frequency advantage of the differential pair, high output swing of the singled-ended version and try to solve the problem of operating in low bias voltage and varying DC offset.

4.3 Proposed Ring VCO topology

Let us begin by summarizing the advantages of both differential and single-ended topologies. First, differential topology has fast oscillation frequency due to its current mode logic, or looking from a different point of view, the output of the differential topology drives only one gate, while the output in the singled-ended case, drives both the gates of an NFET and a PFET. This indicates that we want the output to drive as less capacitance as possible to achieve maximum speed.

Second, the current source in the differential design seems to have no major effect on the tuning range, as long as we have a voltage controlled load device, which controls the gain, while the current source in the singled-ended design is necessary because it is the only tuning mechanism. If we can get rid of the current source AND have a voltage controlled load device, then it will help to boost the output swing while maintain the tuning range. With that in mind, a proposed VCO cell topology is shown in Figure 4.5.

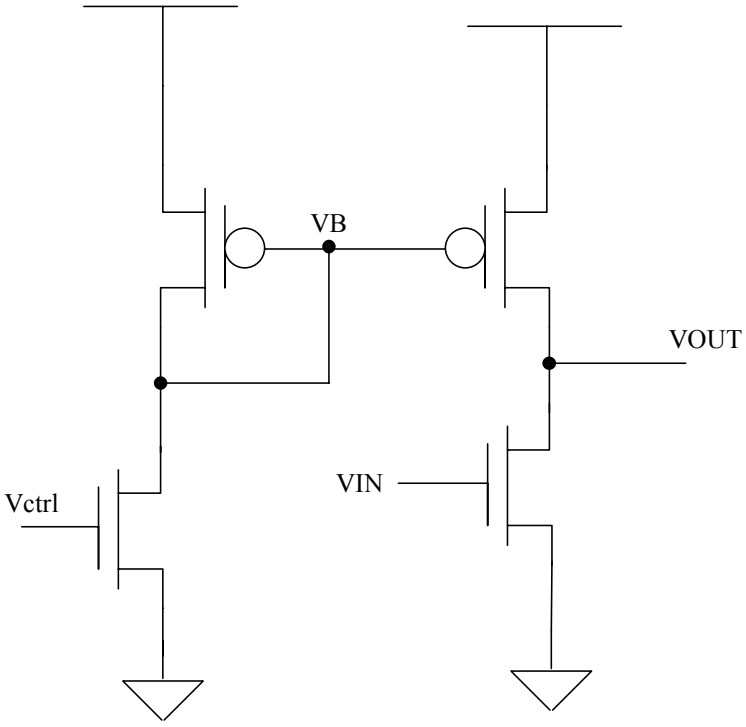


Figure 4.5 Proposed Ring VCO Cell Topology

This topology looks very simple. The core "inverter" consists only of a common source amplifier, while the load device is biased by the inverting scheme from the control voltage. As we have seen in the differential pair with PFET loads, this

biasing scheme will produce a large tuning range. Also the output of the VCO cell drive only another gate, thus can achieving maximum frequency.

However, there are still two old problems within this design: the DC offset problem and small swing at low control voltage problem. In the next sections, we will look at an experimental VCO design that utilizes several circuit tricks to solve these problems.

4.4 Proposed Ring VCO Design

A three-stage ring VCO was designed in 65nm SOI CMOS partially depleted technology, using the VCO delay cell in Figure 4.5. Let us first look at the bias circuit, output buffers, and divide by 2 circuits in this design.

4.4.1 Bias Circuit Design

As we discussed in section 4.3, the VCO output swing becomes smaller and smaller as control voltage goes to near zero. This is due to the fact that as Vctrl goes close to zero, the voltage at node VB becomes close to VDD. This will put the PFET load into subthreshold region. Though this circuit will still oscillate, but the output swing will be extremely small and will not be able to drive any outputs. As a result, the VCO does not work at low control voltages.

To let the VCO to oscillate at low control voltage, we can add an extra diode connected NFET to the bias circuit, as shown in Figure 4.6. This diode connected NFET serves as a feedback device that let the current pass through it whenever the voltage at node VB becomes too high. We can size the NFET device much smaller compared to the main NFET so that it has little effect when the control voltage is high.

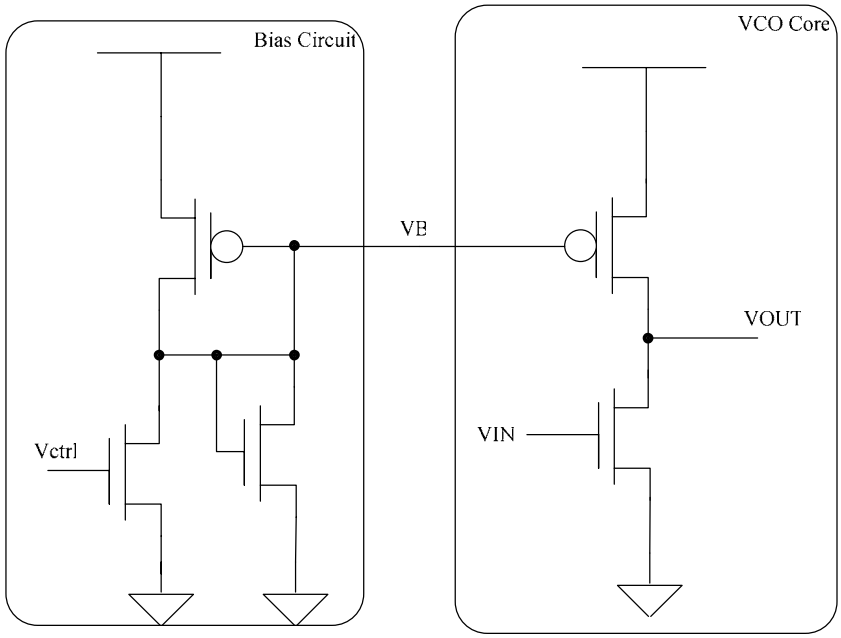


Figure 4.6 Proposed Ring VCO Topology with Bias Circuit Control

Figure 4.7 shows the simulated resulting VB as a function of control voltage when adding an NFET one-tenth the size of the main NFET. As clearly visible, The original VB get closer and closer to VDD while adding a diode-connected NFET prevented VB approaching VDD. With this method, we can choose the size of the diode-connected NFET so that we achieve manageable VCO swing at low control voltages.

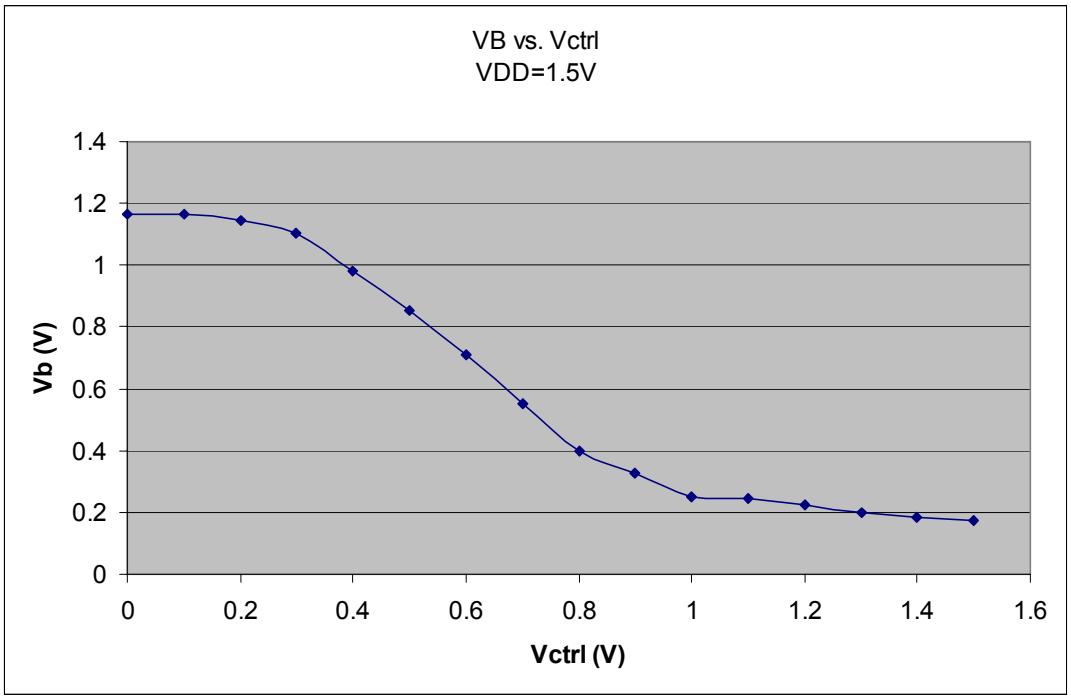


Figure 4.7 Simulated VB vs. Vctrl

4.4.2 VCO Output Buffer Design

One problem with VCO delay cell in Figure 4.5 is that the common mode voltage of the output is not constant, especially when the control voltage is low. This is due to that when the control voltage is low, the inverting bias produces a high voltage at node VB. This high voltage place the PFET load into subthreshold or just above threshold region, which limits it current conducting abilities. As a result, the common mode voltage at output of the VCO will have to go down to decrease the current of the NFET, and the swing at the output will also decrease. Since this occurs at the relatively low frequency end of the tuning range, the low swing can be amplified by the output buffers in the later stage. However the common mode voltage needs to be adjusted so that one design of output buffers can satisfy all frequencies of the VCO output. As a result, a buffering stage will be included at each of the VCO's delay cell.

Since this ring VCO is singled ended, the output buffers will utilize simple digital inverters. However, extra components can be added to them. First since the common mode voltage at output of the VCO varies greatly when the control voltage is low, we can add in a device to reduce this effect, as shown in Figure 4.8(b).

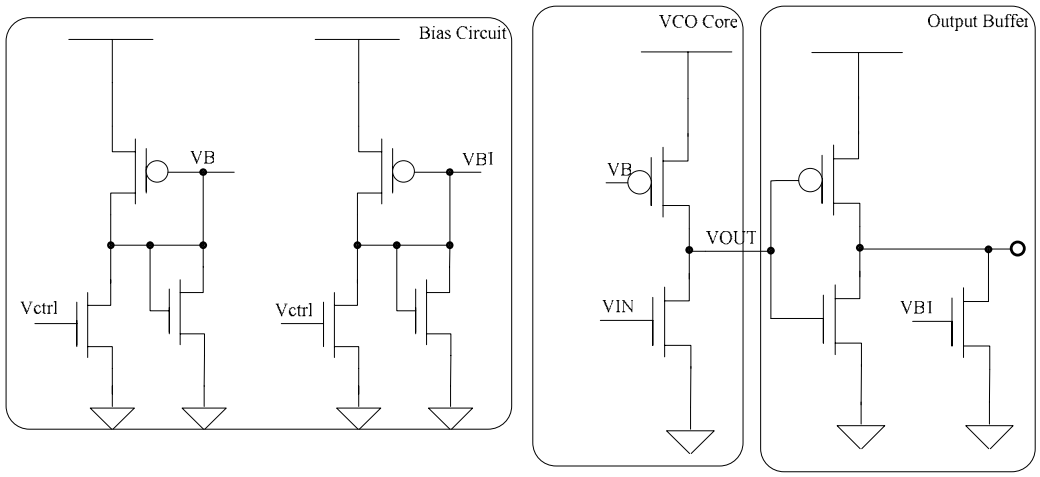


Figure 4.8 a) Proposed Bias Circuit, b) Proposed VCO Core Cell with Output Buffer

As we can see in Figure 4.8(b), the output of VCO delay cell drives an inverter. Naturally if the inverter is unbiased, the common mode voltage at the inverters output would be high when the common mode voltage at VCO output is low. However if we add in the extra NFET, which serve as a leak against the PFET, and we bias the leaking NFET so that it turns on when the common mode voltage at VCO output is low, then we can balance the common mode voltage at output of the first buffer.

The leaking NFET reduces the strength of the PFET and thus lower the common mode voltage at the output of the first buffer. However we only want it to leak at

low control voltages, and we have to design a bias circuit to shut it off when the control voltage is high. Luckily this bias circuit is just the same as the bias circuit for the VCO core, as shown in Figure 4.8(a), though we cannot directly use the bias from the VCO core because the feedback parasitic capacitor can feed noise back onto the core.

Figure 4.9 shows the common mode voltage at the output of the first buffer with and without the leaking NFET. As we can see, the leaking NFET greatly stabilizes the common mode voltage at low control voltages.

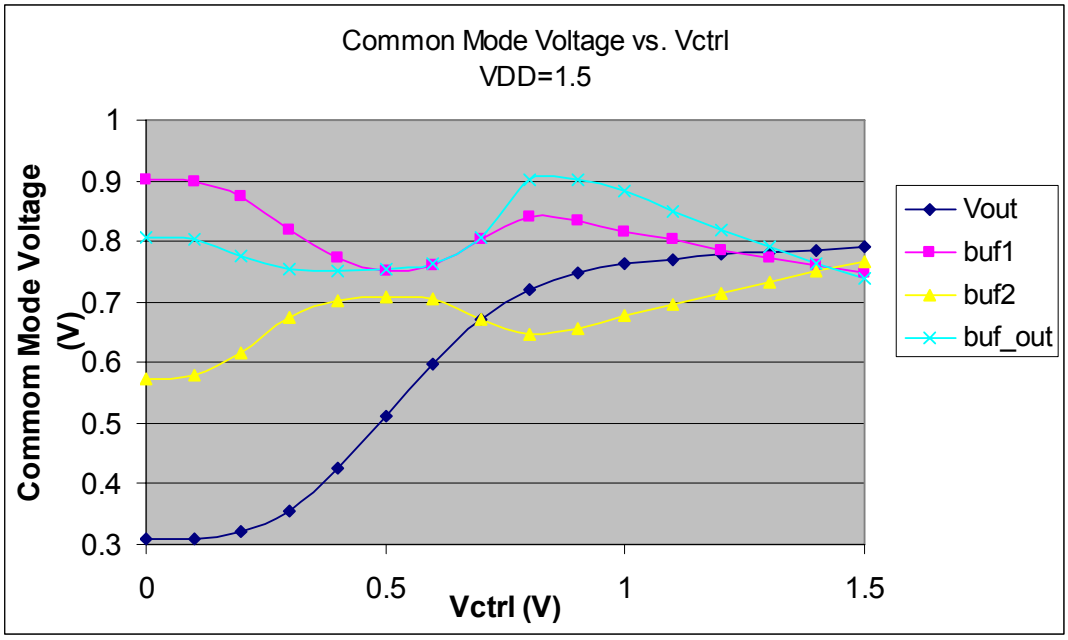


Figure 4.9 Common Mode Voltages of the VCO Buffer Stages vs. VCO Control Voltage

Another problem with high-tuning range VCOs is that the threshold voltages of buffers are not constant for all of VCO's frequencies. This means that at low frequencies, the threshold voltage of the buffers are around VDD/2, but at high

frequencies, even with an input common mode voltage near VDD/2, the output of the buffer does not maintain that common mode voltage. This can cause a serious problem if a chain of inverter is used to amplify a signal. But with the use of resistive feedback between the input and output of an inverter, we can set the common mode voltage at the output of an inverter so that it does not drift too much from VDD/2, as shown in Figure 4.10.

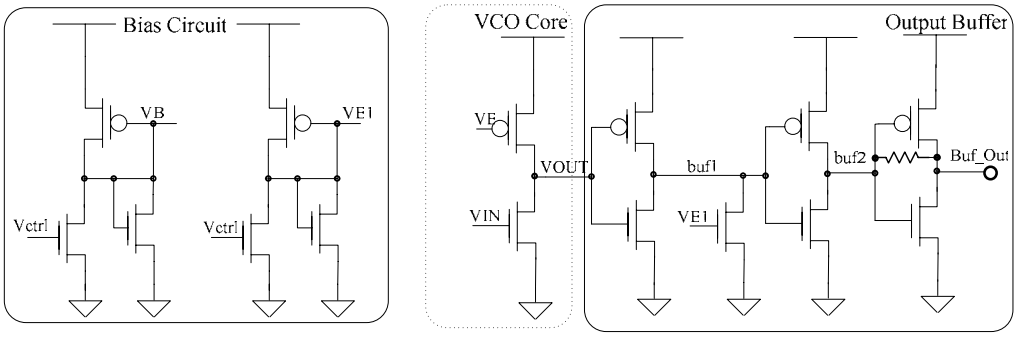


Figure 4.10 Proposed VCO Cell with Bias Circuit and Output Buffer Stages

With this feedback resistor between the input and output of an inverter, the common-mode voltage at the output is sort of "set" to the common mode voltage at the input, though depend on the resistance. The lower the resistance, the more accurate the common mode voltage is, but the gain of the inverter drops with lower resistance. Considering the trade offs here, the final three-stage buffer design for this VCO consists of an inverter with a leaking NFET, a regular inverter, and an inverter with resistive feedback and approximately unity gain.

4.4.3 Divider Design

In most PLLs, the output of the VCO usually drives a VCO divider circuit, as the frequency of the VCO is often too fast for the programmable feedback divider or the phase detector. The design of a divider that is capable of divider very fast signal is

another challenge. Let us look at a divide by two circuit that is capable of dividing the VCO output after the buffering stage.

Since the ring VCO is single-ended, we cannot use the current mode logic divider. Single-ended divider by two circuit such as digital D flip-flop may not be fast enough for the highest frequency of this VCO. To ensure the divider that can divide for all frequencies, we decided to use the extended version of True Single Phase Clock (TSPC) circuit, proposed first by Yuan and Svensson in [8] and discussed in details by Soares and Noije in [9]. The divider is shown in Figure 4.11.

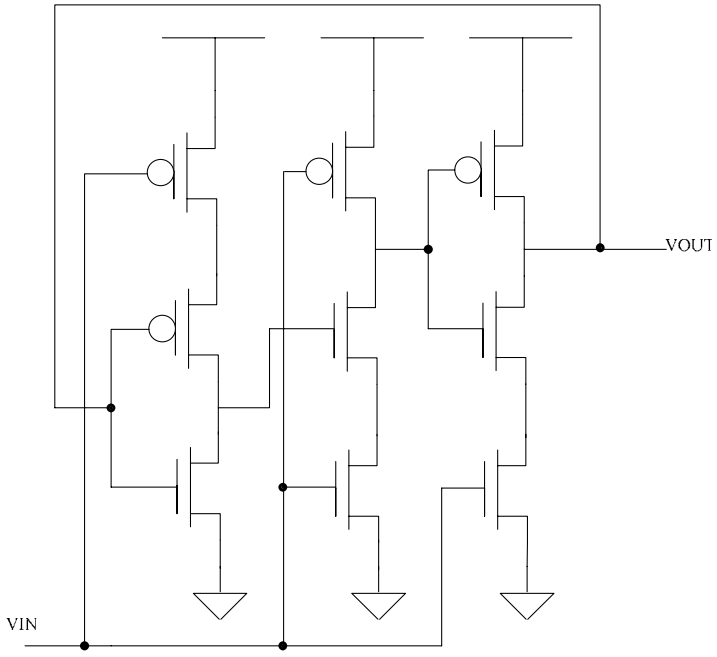


Figure 4.11 TSPC Divider by 2 Circuit

This divider is simply a D flip-flop using precharge and NMOS like blocks. The detailed explanation of how TSPC circuit works and the rules to construct the blocks can be found in [8] and [9]. However, [8] and [9] assumes the input of the TSPC divider by two has full swing, but since the output of the VCO does not have

full swings, the TSPC divider must be tweaked in size and skewed so that it can function in non-full swing mode. Because of this, the output of the TSPC also does not have full swing and the common mode voltage is highly skewed to ground. As a result, additional common-mode adjusting and buffering are needed at the output of the divider. Figure 4.12 shows the divide by two circuit with buffering stages.

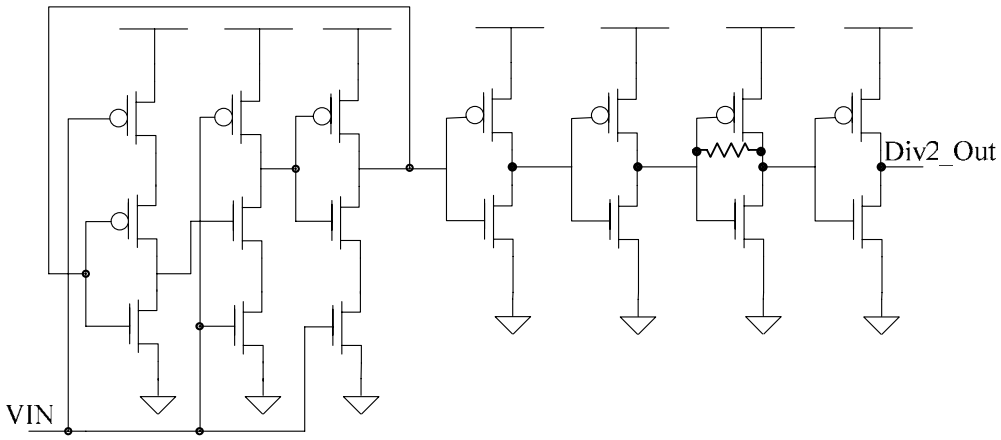


Figure 4.12 Divide by 2 Circuit with Output Buffers

4.5 Experimental VCO Simulation Results

An experimental three-stage VCO design using the proposed delay cell was simulated through PowerSPICE simulator. Figure 4.13 shows the setup. But first, let us look at a brief overview at what devices the technology offers.

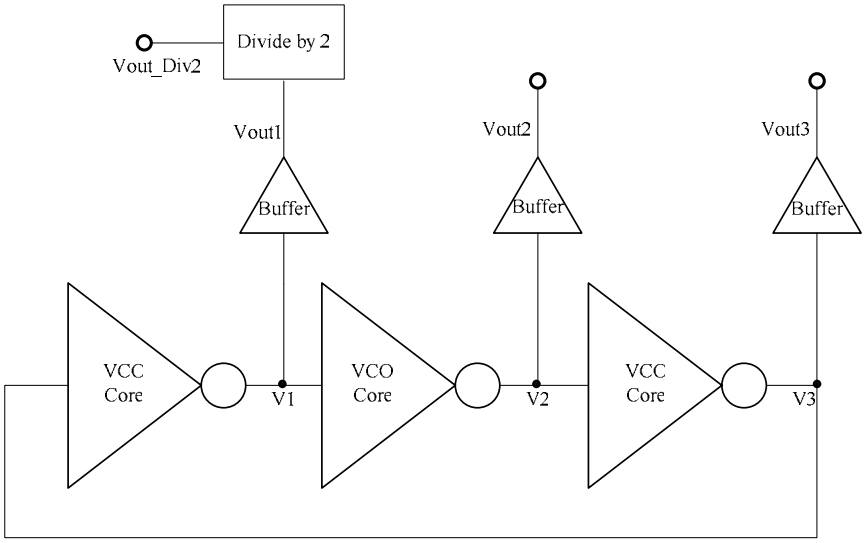


Figure 4.13 Experimental Three-Stage VCO Topology

4.5.1 Technology Overview

The 65nm SOI CMOS technology offered two kinds of devices: thick-oxide device, which are intended for slower, high voltage operations, and thin-oxide device, which are intended for faster, low voltage operations. The nominal supply voltage for thick-oxide devices is 1.5V and, for thin-oxide, 1.0V. The body of these devices is floating, so it is important to initialize these devices so that they have the same body potential to avoid any change in threshold devices when the oscillation begins.

4.5.2 Thick-Oxide Ring VCO Simulation Results

The thick-oxide devices have longer channel length and thicker gate oxide compared to the thin-ox devices. They can sustain higher supply voltage but will be slower. Figure 4.14 shows the oscillation frequencies and tuning range of the VCO simulated using PowerSPICE.

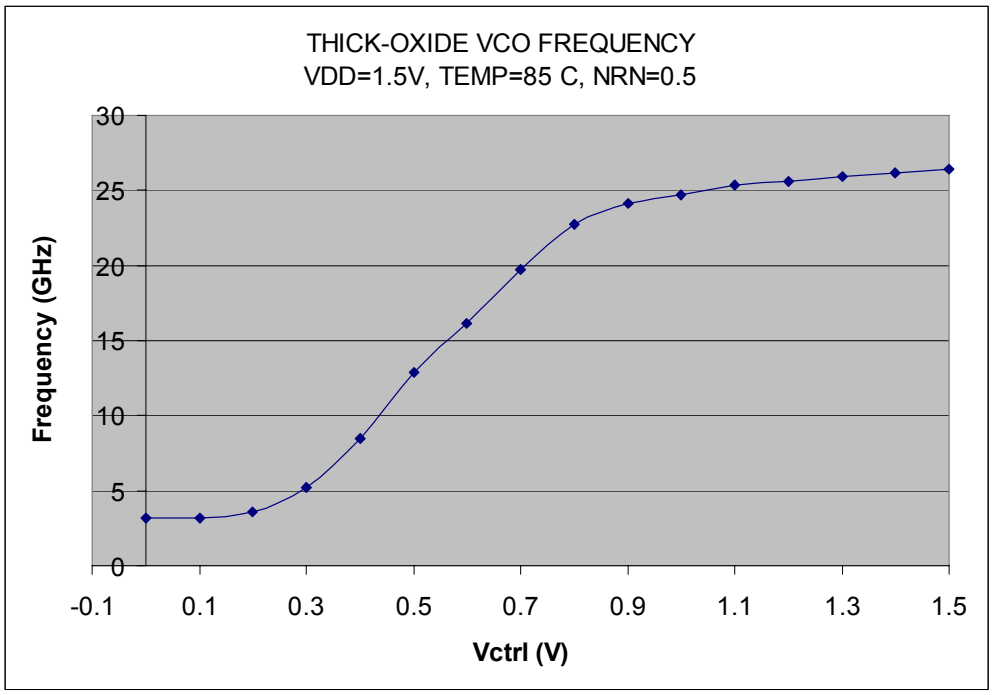
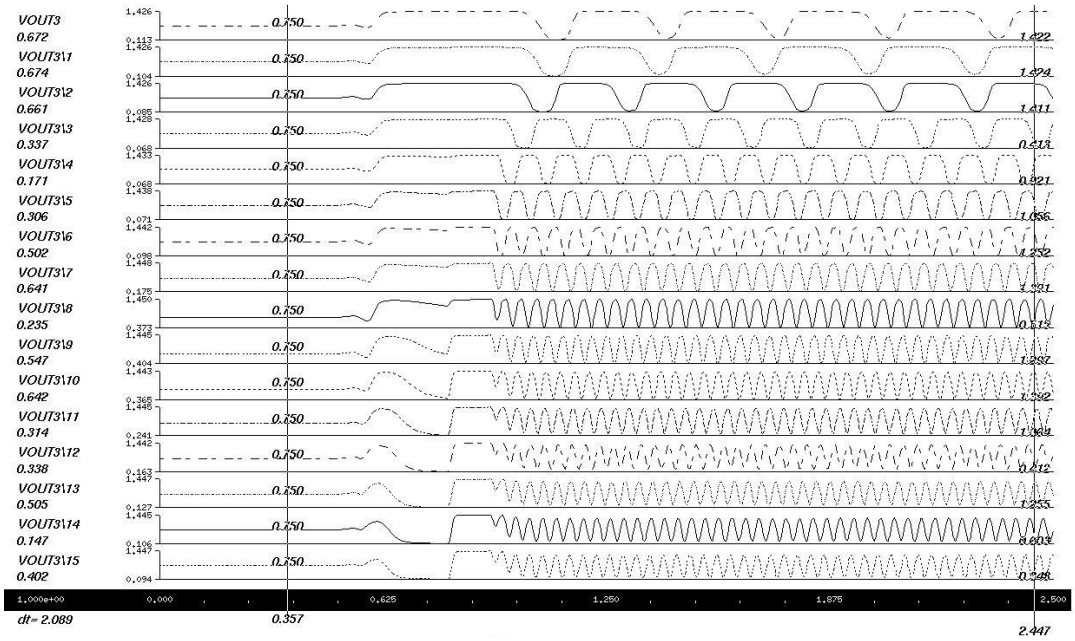


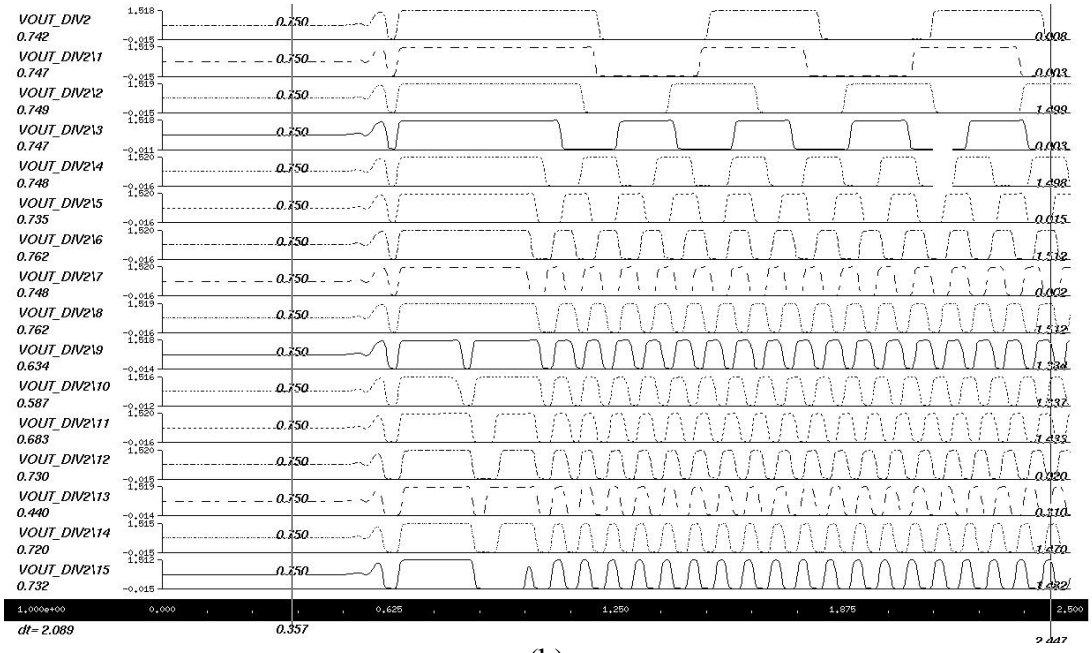
Figure 4.14 Simulated Thick-Oxide VCO Frequency vs. Control Voltage

The frequencies measured in Figure 4.14 were at the output of the VCO buffer. The output swing at the VCO buffer is not fully rail to rail, but at rather around 70% of rail to rail. However this swing is sufficient to drive the divide by two circuit, where at its output, the swing is fully rail to rail.

Another distortion at the output of the VCO buffer is that the signal does not have 50% duty cycle at the low end of the frequency. This is because when the control voltage is low, the load PFET device does not charge up fast enough, thus distorts the VCO output signal. However after the divide by two circuit, the duty cycle is corrected to about 50%, as demonstrated in Figure 4.15 (a) and (b).



(a)

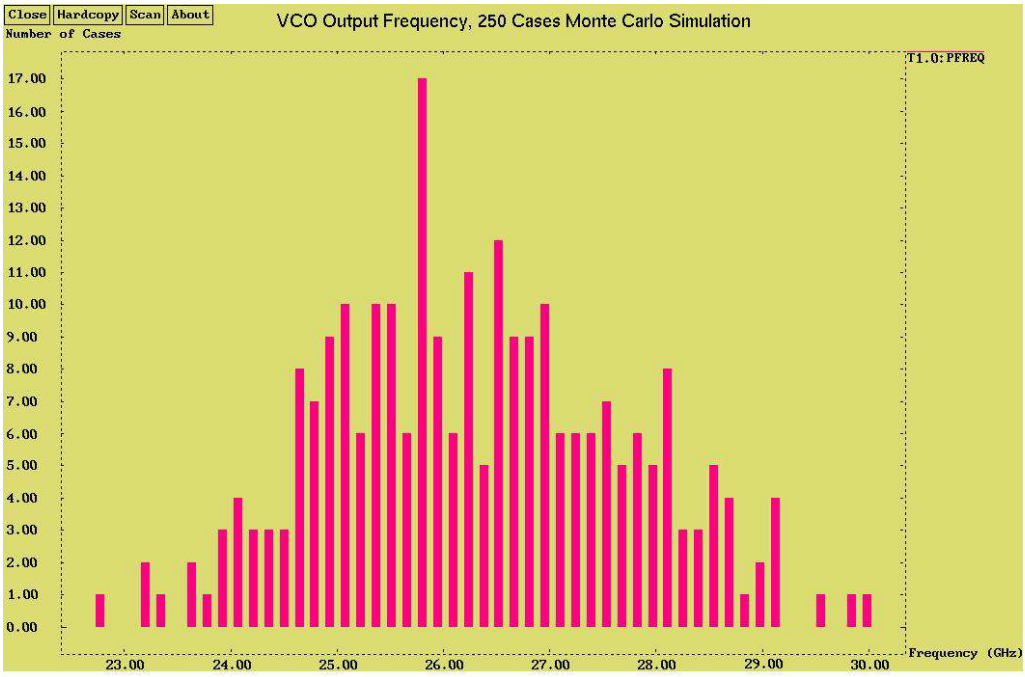


(b)

Figure 4.15 PowerSPICE Simulation Results of Thick-Oxide VCO at a) Output of VCO Buffer, b) Output of Divide by Two Circuit

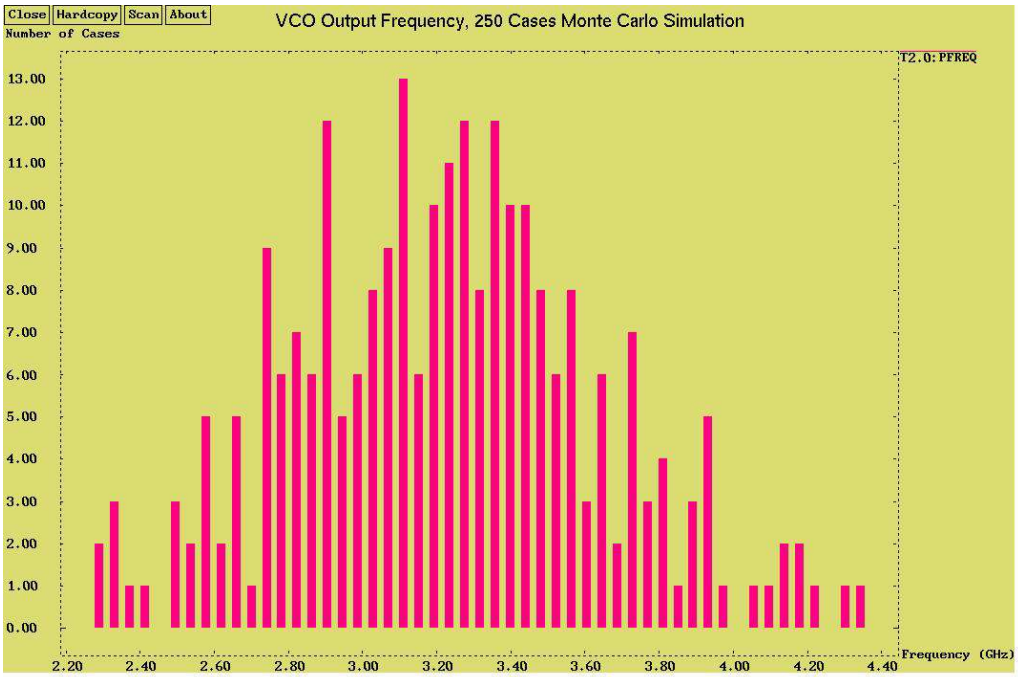
Figure 4.15 (a) shows the output of the VCO buffer at control voltage from zero to VDD, with step of 0.1V in each row, and Figure 4.15 (b) shows the output at the divider with the same setting. The first nanosecond in the simulation is body contact initialization. As we can see in Figure 4.15 (a), the duty cycle of the signal is obviously not 50% at the lower oscillation frequency, but after the divider, the duty cycle become almost 50%.

The frequency of oscillation can greatly vary as temperature and process change. Figure 4.16 (a) and (b) shows the maximum and minimum oscillation frequency for a Monte-Carlo simulation of 250 cases each.



(a)

Figure 4.16 a) Monte-Carlo Simulation 250 cases for Thick-Oxide VCO, Maximum Oscillation Frequency Vctrl=VDD,



(b)

Figure 4.16 b) Monte-Carlo Simulation 250 cases for Thick-Oxide VCO, b) Minimum Oscillation Frequency Vctrl=0

As we can observe from the Monte-Carlo simulation, the maximum frequency of oscillation can vary from 22.6GHz to 29.8GHz, while the minimum can vary from 2.3GHz to 4.3GHz. The mean value of the oscillation frequency is 3.22GHz to 26.3GHz, which agrees with the nominal condition of 3.17GHz to 26.27GHz. The 250-case Monte-Carlo simulation covers 96.3% of the population with 99.5% confidence.

The phase noise performance is shown in Figure 4.17. The top curve is the phase noise at Vctrl=VDD while the bottom curve is at Vctrl=VDD/2. Predicted by Leeson's Equation, the phase noise is better when the oscillator is running at lower frequency.

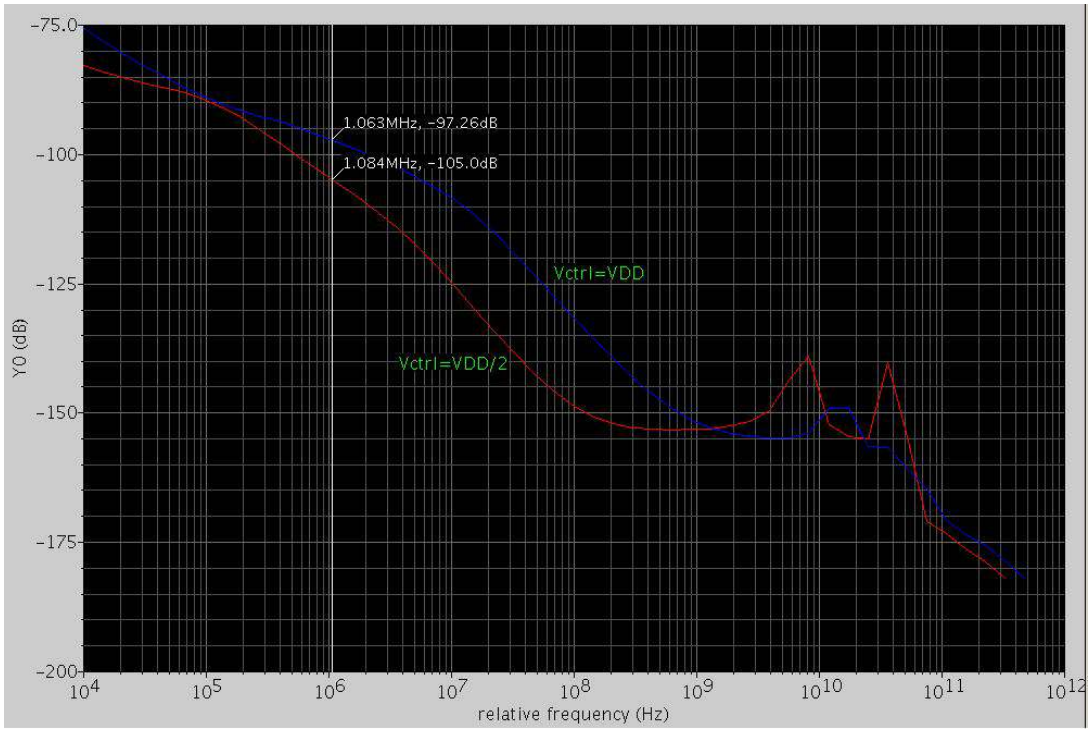


Figure 4.17 Phase Noise Performance of Thick-Oxide Ring VCO

4.5.3 Thin-Oxide Ring VCO Simulation Results

The thin-oxide devices have shorter channel length and thinner gate oxide compared to the thick-ox devices. They can sustain lower supply voltage but will be faster. Figure 4.18 shows the oscillation frequency and tuning range.

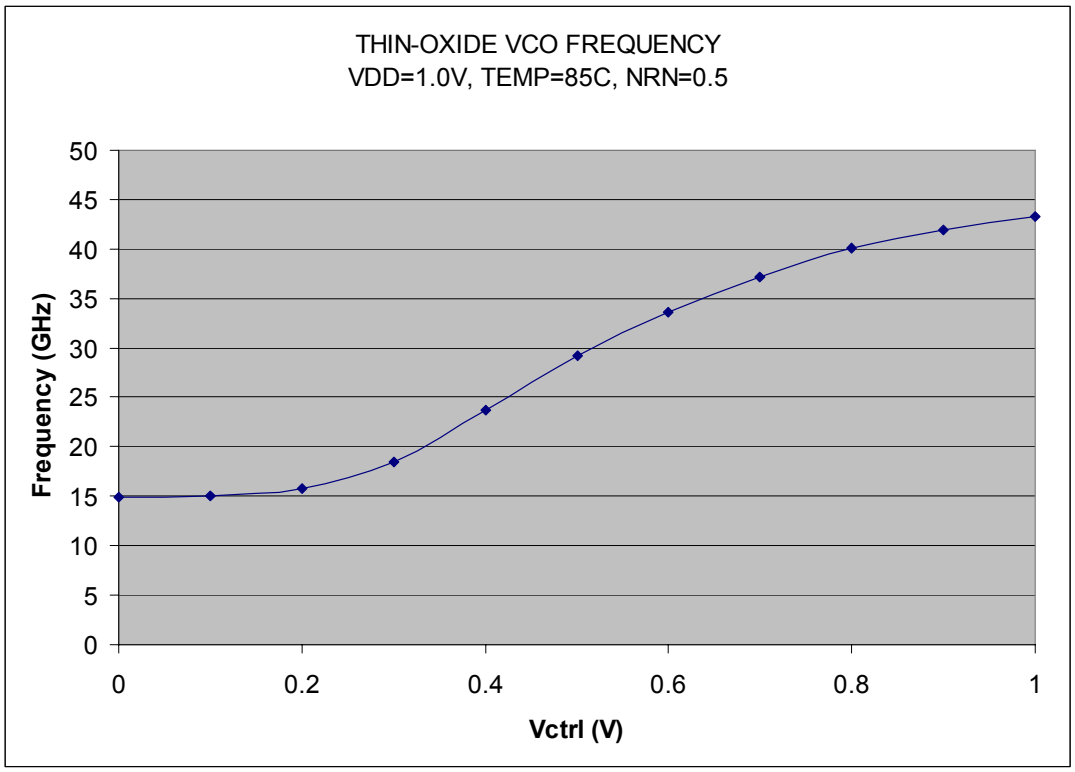
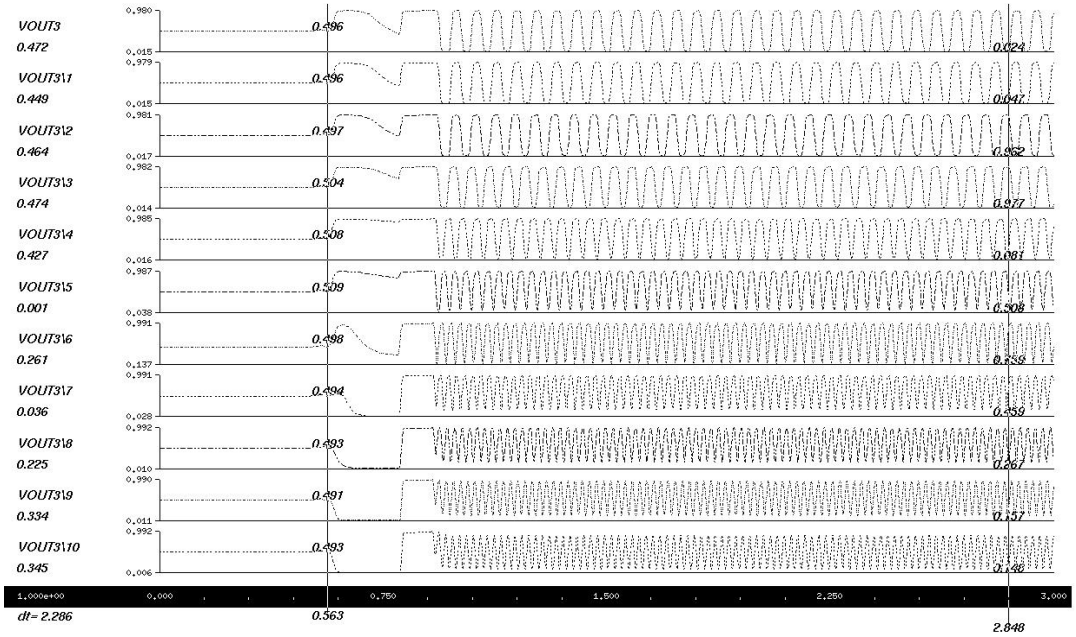


Figure 4.18 Simulated Thin-Oxide VCO Oscillation Frequency vs. Control Voltage

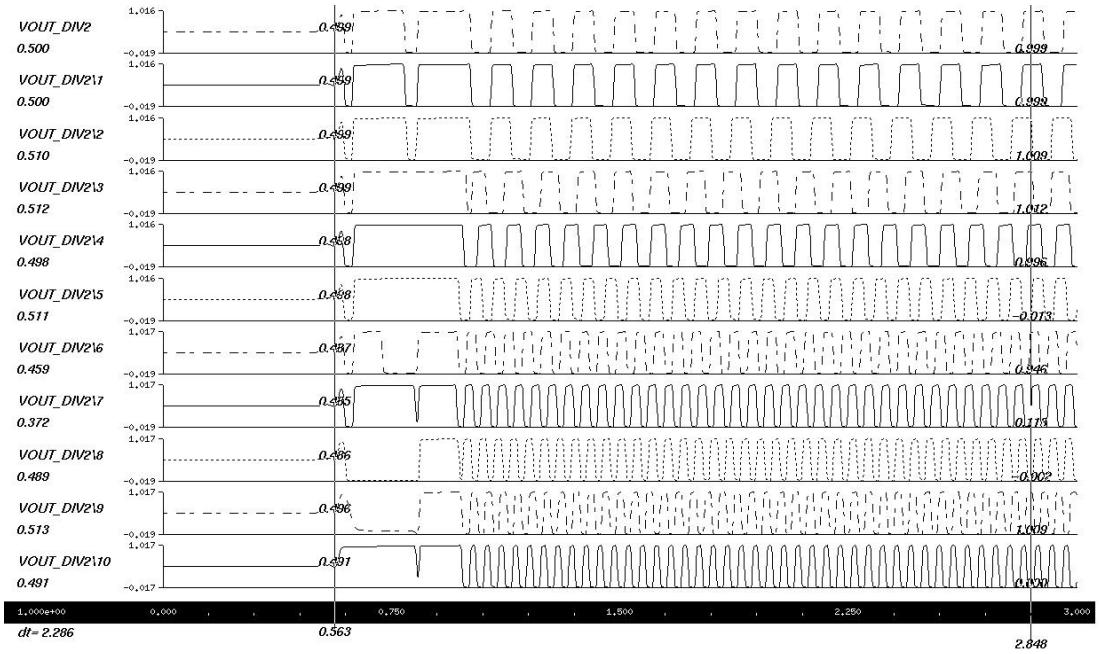
The thin-oxide VCO core can actually oscillate up to 60GHz and as low as 3GHz. However, output swing limits the usability of frequency at both ends. At the high end, the output buffer fails to amplify the signal that is large enough for the divider to function correctly. This is mainly due to that fact that the supply voltage is lowered to 1V, while the threshold voltage of the devices remains relatively unchanged. At the low end of the oscillation, the PFET load device is biased in subthreshold such that both the swing and common mode voltage at the output of the VCO core is so low that no buffers with static sizing can successfully amplify them while still work at higher frequencies. As a result, the bias circuit has to be adjusted so that both high and low frequency ends of the VCO core to be avoided in order for the VCO to be usable in applications.

With the bias circuit adjusted so that the VCO core gives out acceptable levels of swing and common mode voltage, the three-stage buffer shown in Figure 4.9 works very well. The output of the buffer achieved full swing at low end of oscillation frequency and 80% of rail to rail swing at high end of oscillation frequency. These swings are just enough to let the divider to function properly. In contrast to the thick-oxide device, the duty cycle of the signal is about 50% for all frequencies of oscillation at the VCO buffer output. Figure 4.19 (a) and (b) shows the output of the buffer and divider, respectively.



(a)

Figure 4.19 a) PowerSPICE Simulation Results of Thin-Oxide VCO at Output of VCO Buffer,

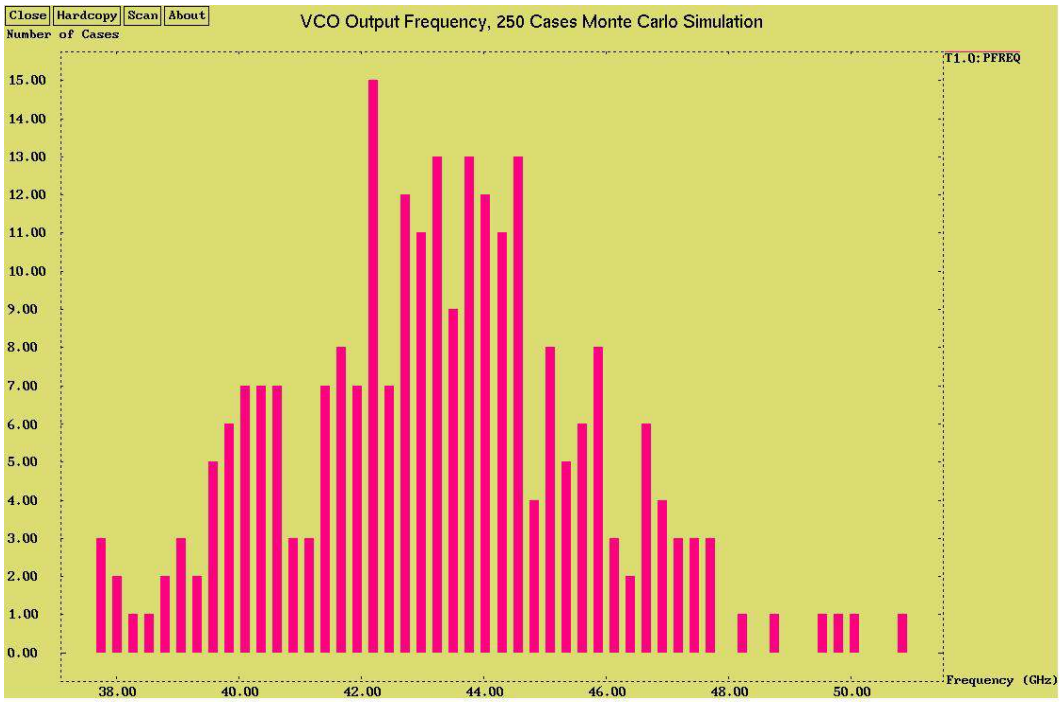


(b)

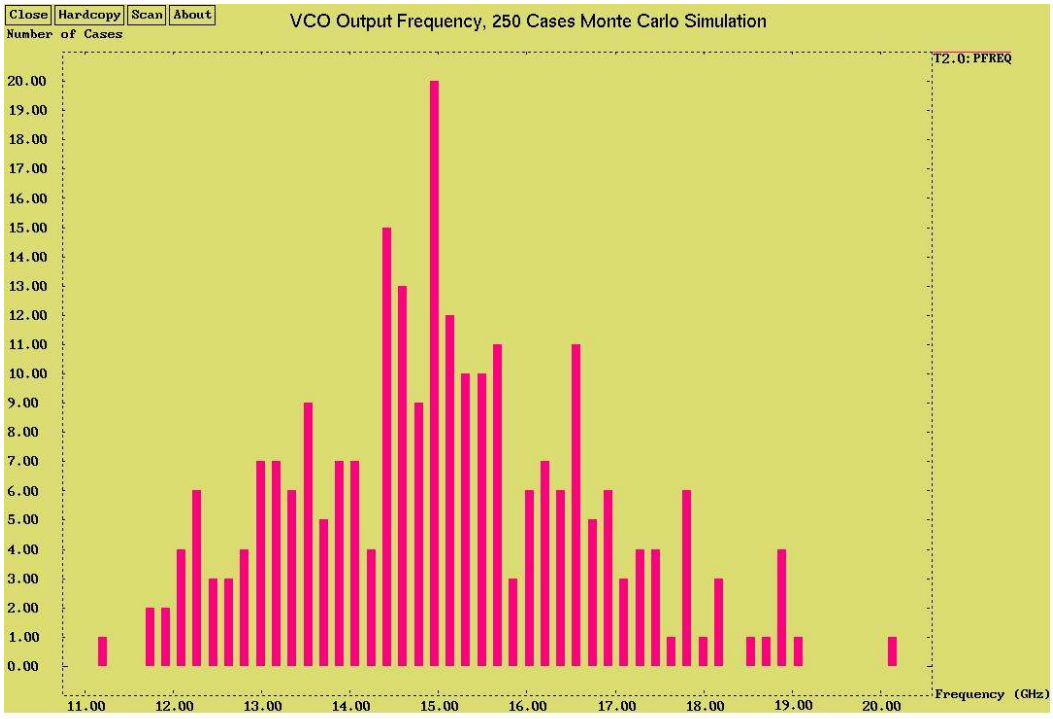
Figure 4.19 b) PowerSPICE Simulation Results of Thin-Oxide VCO at Output of Divide by Two Circuit

Figure 4.19 (a) shows the output of the VCO buffer at control voltage from zero to VDD, with step of 0.1V in each row, and Figure 4.19 (b) shows the output at the divider with the same setting. As we can compare to figure 4.15, in strong contrast to thick-oxide devices at the low end of oscillation frequency, the output of the thin-oxide devices produces great duty cycle at the output of the VCO buffer. This is due to that the bias circuit was biased so that the VCO doesn't oscillate into the distorted region, but at the cost of tuning range.

Like with thick-oxide devices, the thin-oxide devices can suffer even more from temperature and process variations. Figure 4.20 (a) and (b) shows the 250-case Monte-Carlo simulation results of the maximum and minimum VCO output frequency, respectively.



(a)



(b)

Figure 4.20 Monte-Carlo Simulation 250 cases for Thin-Oxide VCO, a) Maximum Oscillation Frequency Vctrl=VDD, b) Minimum Oscillation Frequency Vctrl=0

As we can observe from the Monte-Carlo simulation, the maximum frequency of oscillation can vary from 37.4GHz to 50.6GHz, while the minimum can vary from 10.9GHz to 19.9GHz. The mean value of the oscillation frequency is 15.04GHz to 43.23GHz, which agrees with the nominal condition of 14.93GHz to 43.15GHz. The 250-case Monte-Carlo simulation, again, covers 96.3% of the population with 99.5% confidence.

The noise models for the thin-oxide devices were not available at the time of simulation. Therefore the phase noise results are not available. However the phase noise performance should be in-line with the thick-oxide design as the topology is the same.

4.6 Ring VCO Summary

A ring VCO with proposed delay cell along with bias circuit, buffers, and divide by two circuit was designed and simulated in 65nm SOI CMOS technology. Both the thick-oxide and thin-oxide devices demonstrated very high frequency oscillation and wide tuning range. Table 4.1 shows the summary of the results.

Table 4.1 Summary of Ring Oscillator Result

Criteria (Nominal Condition, 85˚C)		**Thick-Oxide**		**Thin-Oxide**	
		VDD=1.5V	**VDD=1.7V**	**VDD=1.0V**	**VDD=1.2V**
Oscillation Frequency/ Tuning Range		3.17GHz ~ 26.27GHz	5.11GHz ~ 27.46GHz	14.93GHz ~ 43.15GHz	21.75GHz ~ 48.27GHz
Output Swing at Max Frequency	At Core	930mV	1100mV	590mV	720mV
	At Buffer	1020mV	1180mV	790mV	870mV
Power Consumption at Max Frequency	Core Only	7.44mW	10.83mW	6.65mW	12mW
	With Buffers	12.08mW	17.83mW	10.28mW	19.3mW
Phase Noise	Vctrl=VDD	-97dBc/Hz		Model Unavailable	
	Vctrl=VDD/2	-105dBc/Hz			

Both the thick-oxide and thin-oxide ring VCO based on the same design achieved a very wide tuning range. The thick-oxide achieved a tuning ratio of more than 8 at 1.5V supply voltage, while the thin-oxide, due to low supply voltage headroom problems, achieved tuning ratio slightly less than 3. From the table, we can see that both VCOs perform the best at the supply voltage in which it was designed for (1.5V for thick-oxide and 1.0V for thin-oxide). The VCOs are fully functional at higher supply voltage, but the power consumption also goes up exponentially. If we run the VCOs at a lower supply voltage, the VCO cores and buffers will still function properly, but the output swing will decrease to a point where the divider will fail start failing.

In comparison with other published ring VCOs, this design compares very favorably. Few of the published designs have the same tuning range as this design while consuming small amount of power. Table 4.2 shows the comparison.

Table 4.2 Comparison Between Ring VCOs

	Technology	Frequency	Power/Supply	Phase Noise at 1MHz Offset	Note
This Work, Simulation, Thick-Oxide	65nm SOI CMOS	3.2~26.3 GHz	7.4mW @1.5V Supply (Core)	-97 dBc/Hz	Long Channel, Thick Oxide Devices
This Work, Simulation, Thin-Oxide	65nm SOI CMOS	14.9~43.2 GHz	6.65mW @ 1V Supply (Core only)	N/A	High VT Devices
[10]	180nm CMOS	2.5~5.2 GHz	17mW @1.8V Supply	-90.1 dBc/Hz	Two-Stage
[11]	180nm CMOS	5.16-5.93 GHz	1.8V Supply	-99.5 dBc/Hz (Simulated)	Three-Stage
[12]	120nm SOI CMOS	31GHz ± 10%	22.5mW @ 2.5V Supply	-95.9 dBc/Hz @ 10MHz Offset	Inductive Peaking, Three-Stage
[13]	120nm CMOS	8.4~10.6 GHz	52.5mW @ 1.5V Supply	-85 dBc/Hz	Five-Stage, Differential
[14]	180nm CMOS	8.5~14 GHz	146mW @ 1.8V Supply	-95.35 dBc/Hz	Four Stage Multi-Pass

Chapter 5 CONCLUSIONS

VCO is a very important building block in modern communication systems. This thesis analyzed the design of high performance LC tank VCO and a ring VCO. Through simulation, we demonstrated great results from both designs.

Four different LC tank VCOs were designed using IBM 0.18μm CMOS technology: regular VCO and quadrature VCO using single-ended inductors and symmetric inductors. By carefully choosing the components, these VCOs oscillate around center frequency of 5.8GHz with tuning range of around 1GHz. The use of symmetric inductors greatly decreased the layout area, saved power, and improved the FOM, especially noticeable in quadrature VCOs. This family of VCOs would perform well in a narrow band PLL for WiMAX applications.

The design of ring VCO is concentrated from maximum oscillation frequency and tuning range perspective. The use of common source amplifier with PFET load as the main delay cell satisfied both high oscillation frequency and tuning range superbly. The use of additional bias circuit and resistive feedback balanced the common-mode voltage. Also a high speed divide by two circuit was designed to see that the VCO can drive loads properly with acceptable duty cycle. Both the thick-oxide and thin-oxide ring VCO based on the same design achieved a very wide tuning range with full swing at the output of the divider. Overall, both the thick-oxide and thin-oxide ring VCOs are great for wide band PLL applications.

Chapter 6 APPENDIX A

Derivation of Equivalent Resistance of a Crossed-Coupled Pair

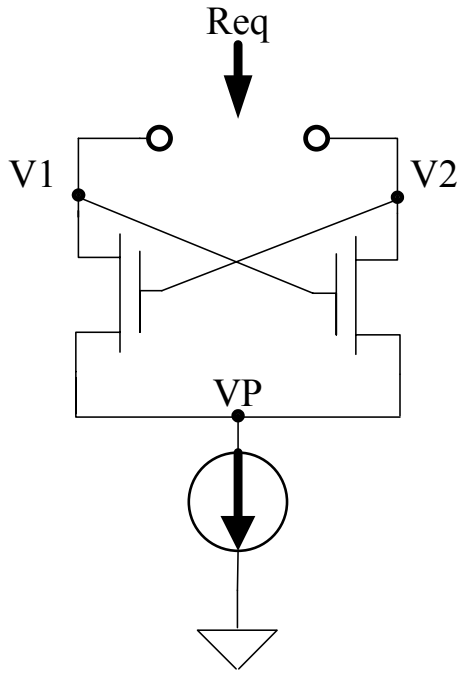


Figure A.1 Crossed Coupled Pair

Let us first begin by realizing the node *Vp* is a common ground for the NFET pair, and let us put a test voltage source across the input and measure the test current coming out of the test voltage source to get the equivalent resistance, as shown in Figure A.2.

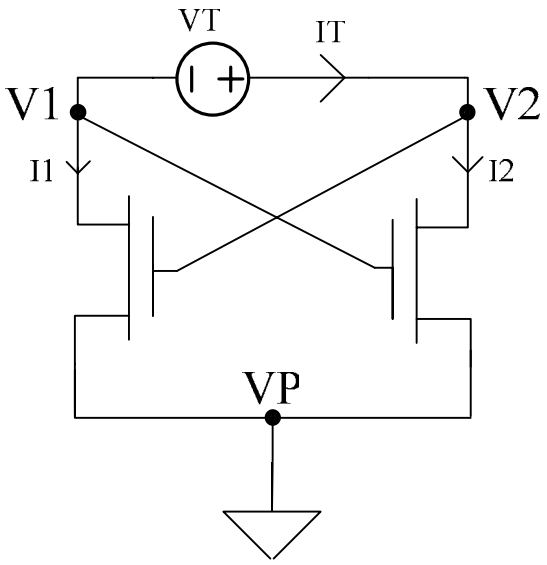


Figure A.2 Crossed Coupled Pair with Test Voltage Source

Let us draw the small signal model of the cross-coupled pair, assuming the devices are matched, no back-gate effect and ignoring parasitic capacitances, as shown in Figure A.3.

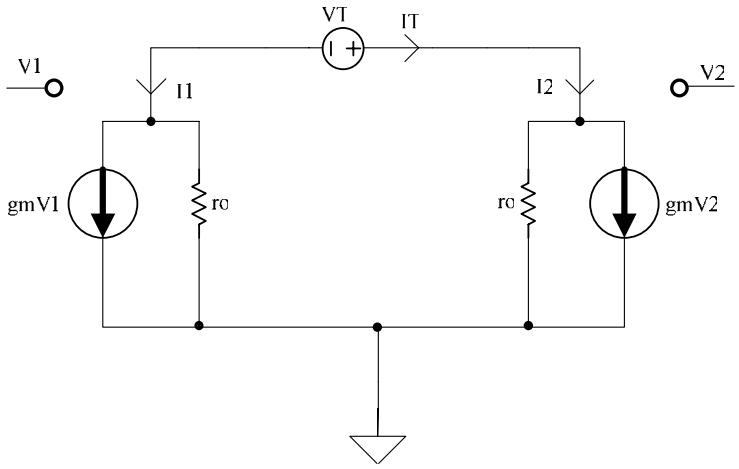


Figure A.3 Small Signal Model for the Crossed Coupled Pair

From the small signal model, we can derive the following four equations:

$$V_T = V_2 - V_1 \tag{A.1}$$

$$I_T = -I_1 = I_2 \tag{A.2}$$

$$V_1 = (I_2 - gmV_1)r_o \tag{A.3}$$

$$V_2 = (I_1 - gmV_2)r_o \tag{A.4}$$

Substituting Equation A.3 into Equation A.4 and vice versa, we get

$$V_1 = (I_1 - gm(I_2 - gmV_1)r_o)r_o \tag{A.5}$$

$$V_2 = (I_2 - gm(I_1 - gmV_2)r_o)r_o \tag{A.6}$$

Expanding Equation A.5 and A.6 and solving for V_1 and V_2

$$\begin{aligned} V_1 &= I_1 r_o - gmI_2 r_0^2 + gm^2 r_0^2 V_1 \\ V_1 &= \frac{-(1+gmr_o)I_2 r_o}{1-(gmr_o)^2} \end{aligned} \tag{A.7}$$

$$\begin{aligned} V_2 &= I_2 r_o - gmI_1 r_0^2 + gm^2 r_0^2 V_2 \\ V_2 &= \frac{-(1+gmr_o)I_1 r_o}{1-(gmr_o)^2} \end{aligned} \tag{A.8}$$

Substituting Equation A.2 into Equation A.7 and A.8 and solve for V_1 and V_2 in terms of I_T, we have

$$V_1 = \frac{-(1+gmr_o)I_T r_o}{1-(gmr_o)^2} \tag{A.9}$$

$$V_2 = \frac{(1+gmr_o)I_T r_o}{1-(gmr_o)^2} \tag{A.10}$$

Substituting Equation A.9 and A.10 into Equation A.1, we have

$$V_T = \frac{2(1+gmr_o)I_T r_o}{1-(gmr_o)^2} \tag{A.11}$$

The equivalent resistance, R_{eq}, looking into the drains of the cross-coupled pair, is then

$$R_{eq} = \frac{V_T}{I_T} = \frac{2(1+gmr_o)r_o}{1-(gmr_o)^2} \tag{A.12}$$

If we approximate that the intrinsic gain of the transistors, gmr_o, is much greater than unity, then we have

$$R_{eq} \approx \frac{2gmr_0^2}{-(gmr_o)^2} = -\frac{2}{gm} \tag{A.13}$$

Thus, the equivalent resistance looking into the crossed-coupled pair is approximately equals to *-2/gm*.

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