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A Design Methodology and Device/Circuit/Architecture Compatible Simulation Framework for Low-Power Magnetic Quantum Cellular Automata Systems

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Abstract– CMOS device scaling is facing a daunting challenge with increased parameter variations and exponentially higher leakage current every new technology generation. Thus, researchers have started looking at alternative technologies. Magnetic Quantum Cellular Automata (MQCA) is such an alternative with switching energy close to thermal limits and scalability down to 5nm. In this paper, we present a circuit/architecture design methodology using MQCA. Novel clocking techniques and strategies are developed to improve computation robustness of MQCA systems. We also developed an integrated device/circuit/system compatible simulation framework to evaluate the functionality and the architecture of an MQCA based system and conducted a feasibility/comparison study to determine the effectiveness of MQCAs in digital electronics. Simulation results of an 8-bit MQCA-based Discrete Cosine Transform (DCT) with novel clocking and architecture show up to 290X and 46X improvement (at iso-delay and optimistic assumption) over 45nm CMOS in energy consumption and area, respectively.

I. INTRODUCTION

Parameter variations and leakage current are increasing every new technology generation, making it harder to scale CMOS devices. Thus, alternative technologies such as magnetic logic are being developed to overcome the limitations to CMOS devices. Magnetic logic, memories and its variants have been theoretically studied and experimentally demonstrated over the past 30 years as a viable replacement for CMOS [1-6]. Interestingly, the energy required for switching a single nano-magnet at room temperature is on the order of zepto-Joules (10^{-21} J). A system with 1 million such nano-magnets can switch with a theoretical limit of 1fJ and when compared with the ITRS projections for double gate CMOS transistors at the 15nm technology node, this is an improvement of 4 orders of magnitude [7].

Magnetic Quantum Cellular Automata (MQCA) was proposed in 2000 by Cowburn and Welland to demonstrate the use of magnetic polarizations for logic computations [3]. In MQCAs, directions of magnetic polarizations of nano-magnets represent binary states. The axes along these directions represent the low energy polarizations. The axes along directions of highest energy polarizations are the hard axes. The implementation of logic operations utilizes the magnetic coupling between these nano-magnets aided by a clocked external magnetic field. However, this magnetic field needs to be suitably clocked to properly operate a chain of nano-magnets with high reliability. The generation and distribution of such magnetic fields would require additional CMOS circuitry and interconnects that consume large amounts of power. Niemier et al used current through parallel wires to generate these magnetic fields [8]. Results show that the energy consumed by the clocking circuitry is significantly greater than the energy dissipated by the nano-magnets. Hence, efficient clocking strategies and architectures are needed to make MQCA systems feasible.

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MQCAs have shown good scalability [1], making them promising for replacing standard CMOS designs. Although basic MQCA logic implementations were experimentally demonstrated [3], their adoption in commercial products has been hindered by the continued scaling of CMOS transistors and lack of system design methodologies, system level simulators and efficient and reliable manufacturing techniques for MQCAs. With the current development of efficient fabrication techniques for nano-magnets, there is a need to explore MQCA circuits and architectures, and compare them to their CMOS counterparts. As such, we developed a design methodology with which MQCA systems can be designed. As we will show in this paper, the design of MQCA systems requires techniques to mitigate design issues arising from the dynamics of MQCA nano-magnets. Hence, to evaluate the power-performance limits of MQCAs, an integrated device/circuit/system simulation framework is needed and we developed such a framework. To that effect, we also show how novel clocking strategies and architectures mitigate MQCA system design issues.

The rest of the paper is organized as follows. Section II introduces the basics of MQCA and proposes suitable architecture for MQCA systems. Section III describes novel clocking architectures and strategies for logic isolation and noise immunity in MQCA systems. In order to evaluate the power-performance limits of an MQCA system, an integrated device/circuit/architecture simulation framework, which we present in Section IV, is needed. Section V discusses our MQCA design methodology, including the synthesis of an MQCA cell library. An MQCA based implementation of DCT was synthesized using the proposed design methodology and evaluated using our simulation framework. The simulation results and comparisons with standard CMOS based DCT design in 45nm predictive technology [9] is discussed in Section VI. Finally, Section VII concludes this paper.

II. BASICS OF MAGNETIC QUANTUM CELLULAR AUTOMATA

The basics of MQCAs were presented in [1,3]. Fig. 1 shows the majority logic gate developed in [1]. The easy axes are along the directions in which the nano-magnets tend to be polarized in equilibrium. The hard axes are along directions in which the polarizations of nano-magnets have the highest energy and are perpendicular to the easy axes for implementing binary logic. The easy axis is taken to be the y-axis (vertical) in fig. 1. The magnetic field lines show that dipolar coupling between magnets in the x-direction (horizontal) is anti-ferromagnetic and that between magnets in the y-direction is ferromagnetic. The compute nano-magnet is magnetically coupled to all four surrounding nano-magnets.

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However, the output and compute nano-magnets can be first driven into the hard axis using an external magnetic field, and then allowed to relax. Dipolar coupling in the hard axis is very weak; therefore, the compute nano-magnet couples more strongly to nano-magnets A, B and C. As such, its polarization will align itself with the effective magnetic field due to nano-magnets A, B and C but not the output nano-magnet. The majority effect determines the polarization of the compute nano-magnet and this realizes majority logic. By biasing nano-magnet B, the gate can be configured as an OR or AND gate. Using the notation in fig. 1 and using nano-magnets A and C as primary inputs, fixing nano-magnet B as '1' ('0') realizes an OR (AND) gate. Also, MQCAs work like a pipeline since they need clocks to propagate data.

MQCA data propagation is done using chains of nano-magnets [8]. These chains need to be short to realize compact MQCA systems. Thus, a near neighbor architecture is best suited for MQCA systems. We propose implementing MQCA systems as systolic arrays [10], especially for digital signal processing applications which are well-suited for systolic architectures.

Also, an external magnetic field is needed to isolate the output from the inputs and is clocked to enable computations every cycle. Hence, MQCA systems synthesized from these gates needs be properly clocked for reliable and higher performance operation. The design of clock architectures and strategies are discussed in the next section.

III. Clocking Architecture and Strategies

We have seen in Section II that clocks are needed in MQCA systems for input-output isolation and/or computation robustness. Even though basic MQCA cells are very low-power, the clock network may not be [8]. Thus, efficient clock architectures and strategies are needed to make MQCA systems feasible. Current technology uses CMOS circuits to generate clock signals for switching current sources. The current is then converted to magnetic fields. In this section, we propose different clocking technologies and strategies, and power-efficient clock architectures to trade-off computation robustness and speed.

A. Clocking Strategies

As mentioned in Section II, MQCAs work like a pipelined circuit where computations on different data and data transfer are synchronized by clock signals. Another purpose of the MQCA clock is to control dataflow. Thus, the basic idea for clocking an MQCA logic pipeline can be described as follows: 1) Current stage is clocked in preparation for computation. 2) The following stage is clocked. 3) The previous stage is not clocked while the next stage is, and the magnetic field to the current stage is switched off. 4) The previous stage is clocked since data from the previous stage is not needed. Hence, multiple clocks are needed for high-throughput, robust MQCA systems and the following section describes proposed clocking strategies.

A.1 4-Phase Overlapping Clocks

Fig. 2 shows the operation of a 5-stage MQCA inverter chain using 4-phase overlapping clock scheme. It is clearly shown that data is properly propagated along the chain. The propagation delay of each stage depends on the settling time of the nano-magnets. This strategy requires 50% overlap between clocks of consecutive stages. However, the clocking circuit may consume too much power generating four clocks.

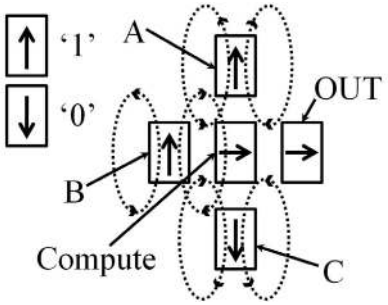

Figure 1. An MQCA Majority logic gate is shown along with the magnetic field lines of the nano-magnets. Magnets along the x-direction has anti-ferro-magnetic coupling and those along the y-direction has ferro-magnetic coupling. The effective magnetic field felt by the compute nano-magnetic is the sum of all the fields. The magnetic fields of nano-magnets A and C combine to align the compute magnet to '1'

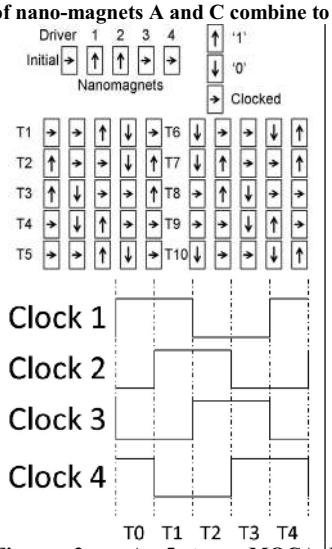

Figure 2. A 5-stage MQCA inverter chain implemented with 4-phase overlapping clocks. When clock is high, the external magnetic field is on. The hard and easy axes of the magnets are in the horizontal and vertical directions respectively. The driver and magnet 4 uses the same clock. T1 to T10 are time steps shown below. The chain is fed a '1' followed by a '0' at T2 and T6 respectively.

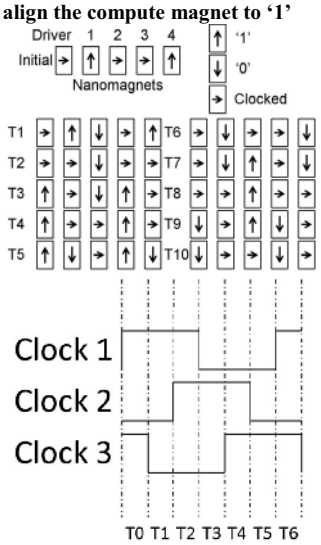

Figure 3. A 5-stage inverter chain operating with 3-phase overlapping clocks. The external magnetic field is on when clock is high. A '1' is propagated first followed by a '0' at T3 and T9 respectively. T0 to T10 mark time instances shown below. Note that there is an extra latency of 1 clock cycle in propagating data. The hard and easy axes of the magnets are in the same directions as in Figure 2.

A.2 3-Phase Overlapping Clocks

A less power hungry alternative is the 3-phase overlapping clock scheme shown in fig. 3. This strategy requires 33% overlap between clocks of consecutive stages. Compared to the 4-phase scheme, the clock frequency needs to be lowered to maintain the clock overlap time. The overlap time ensures that nano-magnets of consecutive stages are fully aligned along the hard axis before computation occurs. A longer pulse and lower frequency implies that computation robustness is maintained at the expense of speed and power. Thus, power, speed and robustness of the circuit can be traded-off by choosing between 3- and 4-phase clocking schemes.

B. Clock Architectures

Current Phased-Locked Loop (PLL) circuits are able to generate the clock signals described in section III-A. Thus, we only focus on technologies to convert current into magnetic fields and discuss their power efficiency.

B.1 Parallel Wires

Alam et al showed how current through parallel resistive wires is used to generate magnetic fields for clocking MQCA nano-magnets [11]. Nano-magnets between adjacent clock zones might be incorrectly clocked due to variations and current noise in wires. Furthermore, large current might be required to generate sufficient magnetic field strength and power efficiency is compromised. Niemier et al showed that clock energy using this scheme can be 100X of nano-magnet switching energy [8]. The clocking energy will increase if our proposed clocking strategies are used to guarantee computation robustness. Hence, more power efficient technologies are needed for better control of nano-magnet clocking in MQCA systems.

B.2 Spin-Transfer Torque Magnetic Tunneling Junctions

By placing individual nano-magnets above the tunneling layer of spin-transfer torque magnetic tunneling junctions (STT-MTJ), the magnetic field from MTJ can be used to clock the nano-magnets. Fig. 4 illustrates how the parallel or anti-parallel arrangement of the hard and free layers of the MTJ is able to generate a magnetic field in the region above the tunneling layer. The arrangement is switched by passing a minimum current through the MTJ layers. 6μA of current is needed to switch an MTJ with t_{ox}=10nm and 10X15nm^2 cross-section in 3.3ns. A 250mV current source would use 5fJ of energy to deliver this current [12]. However, the spacing between the nano-magnet and the MTJ needs to be very small (~1nm) for the magnetic field to be large enough to clock the nano-magnet.

B.3 Nano-coils and Solenoids

Alternatively, the nano-magnet can be wrapped inside nano-coils or solenoids for clocking. The strength of the magnetic field can be increased by replacing the core material with high permeability material or increasing the current. Table 1 lists the permeability of suitable core materials. Possible remnant polarization in high permeability materials requires a second solenoid or depolarizing current to eliminate it. The impact of core material permeability on the solenoid current and energy requirements are shown in fig. 5. Fig. 6 illustrates how a solenoid can be used to clock MQCA nano-magnets. The drawback of coil based clocks is the inductive coupling between them, which can generate voltages in non-switching coils. This coupling can be reduced by larger spacing between coils.

Each of the clocking strategies and techniques discussed has different power requirements. Thus, they need to be considered to accurately estimate the power consumption of the MQCA system. The next section proposes an integrated device/circuit/system simulation framework that does this.

IV. Device/Circuit/System Compatible Simulation Framework

The dynamics of MQCAs presented in Section II can be described by a set of equations describing the interactions between MQCA nano-magnets. The Landau-Lifshitz-Gilbert (LLG) equation [17,18] describes the dynamics of a magnet and can be modified to include the dipolar interactions between magnets; hence, a system of these equations can be derived to describe any MQCA system. The stable orientation of magnetic moment in a MQCA nano-magnet depends on its

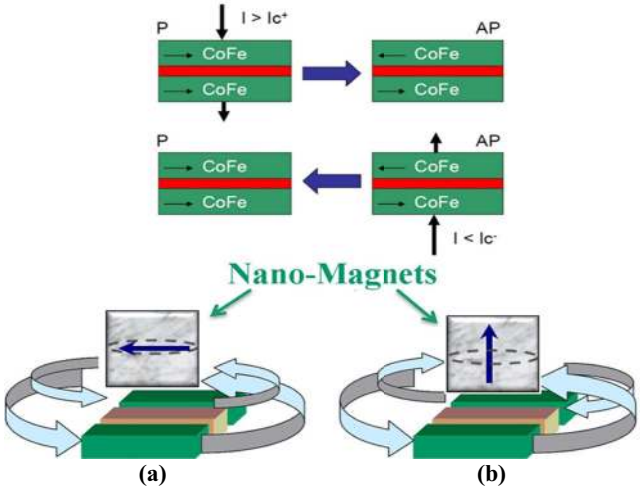

Figure 4. MTJs as magnetic field generators in MQCA systems. The nano-magnet with a vertical easy axis is located directly above the tunneling layer of the MTJ. Current through the tunneling layer via the fixed layer determines the free layer polarization (top). (a) A parallel configuration imposes a magnetic field on the MQCA nano-magnet while (b) the anti-parallel case imposes no magnetic field on the nano-magnet

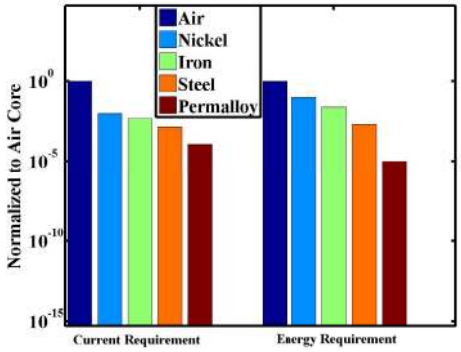

Figure 5. The relative permeability of the material around the MQCA nano-magnets affects the electrical current and energy requirement of MQCA systems using solenoid magnetic field generators

built-in anisotropy energy (Ku_2), its saturation magnetization and the effective magnetic field ($\overrightarrow{H_{tot}}$) it experiences as in (1). $\overrightarrow{H_{tot}}$ consists of the clocked magnetic field ($\overrightarrow{H_{ext}}$), the anisotropy field ($\overrightarrow{H_{ani}}$) and the dipolar interaction field ($\overrightarrow{H_{dip}}$) as shown in (2). $\overrightarrow{H_{ani}}$ of a nano-magnet is related to its saturation magnetization (M_S) by (3). The magnetic moments of other nano-magnets, the spacing between nano-magnets and $\overrightarrow{H_{dip}}$ generated are related by (4). An MQCA system can be simulated by initializing the nano-magnets to an initial state and numerically solving (1-4) and the LLG equation in (5) for each nano-magnet in a time-domain to yield the system performance. The power dissipated is computed using (6) as discussed in [13]. Increasing the ramp time of the clock signals beyond the critical ramp time (τ_C), given by (7), can reduce energy dissipation [12] and fig. 5 shows the use of this technique on an MQCA based inverter.

As Niemier et al show in [8], the clock circuitry can consume significantly more power than the MQCA magnets. Hence, the clocking circuitry has to be modeled and its power consumption estimated. The lumped circuit model of fig. 6 models each magnetic field generator and its energy consumption during each clock cycle is given by (8). The power used to generate the clocked magnetic fields is

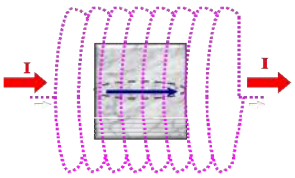

Figure 6. A nano-magnet encompassed by a coil MQCA clock field generator. Electrical current through the solenoid generates a magnetic field in the region enclosed by it. The strength of the magnetic field generated can be increased using higher permeability cores. Coupling between coils is reduced by larger spacing between the coils

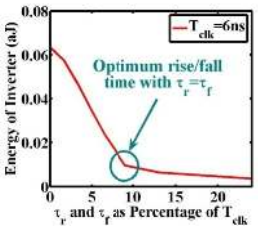

Figure 7. The ramp time (τ_r and τ_f) of the clock signal with 6ns period (T_{clk}) is increased as a percentage of T_{clk}. The energy consumed by an MQCA inverter clocked by this signal is reduced. This optimum point is selected because increasing the ramp time beyond this point introduces functional failures to the system and the reduction in energy is less

TABLE 1
RELATIVE PERMEABILITY OF MATERIALS FOR SOLENOID CORES

Material	Air	Nickel	Iron	Steel	Permalloy
μ_r, Relative Permeability	1	100	200	700	8000

TABLE 2
MQCA SYSTEM AREA ESTIMATION EQUATIONS

Stacked layout area = Max(CMOS Area, MQCA Area)

CMOS area can be obtained from commercial design tool

MQCA area = Layer Width × Layer Height

N = number of magnets along layer width or height

Layer width = N × magnet width + (N - 1) × magnet spacing

Layer height = N × magnet height + (N - 1)× magnet spacing

TABLE 3
MQCA SYSTEM POWER ESTIMATION EQUATIONS

$$\vec{M}(spin)_{nm} = f(H_{tot}, Ku_2) \quad (1)$$

$$\overrightarrow{H_{tot}} = \overrightarrow{H_{ext}} + \overrightarrow{H_{ani}} + \overrightarrow{H_{dip}} \quad (2)$$

$$\overrightarrow{H_{ani}} = H_C \vec{m}_y \vec{y} = \frac{2Ku_2}{M_S} \vec{m}_y \vec{y} \quad (3)$$

$$\overrightarrow{H_{dip}} = \sum_{n=1, n\neq j}^{N} \frac{(3(\overrightarrow{M_n}\cdot\overrightarrow{r_{nj}})\overrightarrow{r_{nj}} - \overrightarrow{M_n} r_{nj}^2)}{r_{nj}^5} \quad (4)$$

$$(1+\alpha^2)\frac{\partial \vec{M}}{\partial t} = |\gamma|(\vec{M} \times \overrightarrow{H_{tot}}) - \frac{\alpha|\gamma|}{|M|}\vec{M} \times \vec{M} \times \overrightarrow{H_{tot}} \quad (5)$$

$$P_{diss} = \frac{\alpha|\gamma|}{(1+\alpha^2)|\vec{M}|}(|\vec{M} \times \overrightarrow{H_{tot}}|)^2 \quad (6)$$

$$\tau_C = \frac{(1+\alpha^2)}{2\alpha(|\gamma H_C|)} \quad (7)$$

$$\text{Energy Consumed} = \int_0^T i(t) R_{eq}\, dt \quad (8)$$

$$P_{generators} = \frac{1}{T} \sum_{signals}^{all\ clock} \sum_{\substack{generators\ using \\ each\ clock\ signal}}^{all\ field} \int_0^T i(t) R_{eq} dt \quad (9)$$

calculated from (9); the system power consumption is the mean energy consumed by all magnetic field generators in a clock period.

Area Estimation

The MQCA system area depends on the technology used for fabrication. CMOS circuitry and wiring for generating the clocked magnetic field can be fabricated on a substrate and the MQCA nano-magnet layers stacked on top as shown in [11]. Thus, the area is constrained to that of the largest layer. Alternatively, everything is fabricated in one layer and the system area is the sum of the CMOS and MQCA areas. Available commercial design tools are able to estimate the CMOS area from the layout. The MQCA layer area depends on the nano-magnet spacing and size. Table 1 summarizes the equations for area estimation.

The equations in our simulation framework are summarized in Tables 2 and 3. A simulator can be implemented to solve these equations and evaluate the power-performance of MQCA systems. In the following section, we propose a design methodology for synthesizing MQCA systems.

V. DESIGN METHODOLOGY

We have seen in Section II that MQCA systems has to be designed as pipelined systolic arrays controlled using clocking architectures and strategies presented in Section III. However, a fully-customized design can be difficult to synthesize and thus, we propose a cell-library approach to simplify the design process. The design of MQCA cell library is discussed next followed by the MQCA system design methodology using the MQCA cell library.

MQCA Cell Library Design

NAND and NOR gates are needed to implement logic. Imre et al demonstrated a reconfigurable majority logic gate in [1] and this concept can be used to synthesize a library of basic MQCA logic cells. The majority gate can be cascaded and reconfigured to realize higher fan-in logic gates by fixing inputs (Fig. 9). For an n-input MQCA gate, the total number of input magnets (N) and the number of fixed magnets (N_{fix}) that are required to synthesize it are calculated from

$$N = 2n - 2,\ n \geq 2$$
$$N_{fix} = n - 1 \quad (10)$$

Fig. 9 shows the implementation of 2-, 3- and 4-input gates in MQCA. Positions labeled with 'fix' are the fixed inputs whose values depend on the logic implementation. Table 4 gives the configurations of these gates and the logic functions implemented. An MQCA cell library using 10nm side cubic nano-magnets was synthesized. The delay, area and energy consumed by some MQCA gates are listed in Table 5.

System Design Methodology

An MQCA system can now be synthesized using the cell library synthesized from the previous section. However, the power-performance of the system depends on the technology available and the design of basic MQCA logic cells. Thus, we propose a design methodology using the following steps:

1. Given the MQCA technology parameters (anisotropy, nano-magnet material, etc.), choose an initial nano-magnet volume
2. Design an MQCA inverter chain using the initial nano-magnet size and a spacing (t_{dm}) optimized from $\overrightarrow{H_{ani}}$

3. Using a LLG solver to determine the energy delay product (EDP) of the chain, minimize the EDP by iteratively choosing the nano-magnet volume and repeating step 2
4. The nano-magnet volume and spacing obtained at the end of step 3 is used to design a library of basic MQCA logic cells as discussed in the previous sub-section
5. Synthesize an MQCA systolic array based on the targeted application (eg. DCT) using the cell library from step 4
6. Choose a clocking architecture and strategy discussed in Section III
7. Using a LLG solver incorporating clocks, determine if the synthesized design meets power-performance-area specifications. Repeat steps 5 and 6 until specifications are met. Specifications may have to be relaxed if iterations do not yield a feasible design

An MQCA based systolic array 8-bit DCT was synthesized using our design methodology. A MATLAB simulator based on our simulation framework was implemented and used to evaluate the MQCA DCT. Simulation results and comparisons to the standard CMOS technology DCT implementation are presented in the next section.

VI. Simulation Results

A feasibility study of MQCA systems was conducted using the simulation framework and design methodology proposed in Sections IV and V, respectively. An MQCA based 8-bit Discrete Cosine Transform (DCT) based on the unified systolic array architecture of Chang and Wu [14] was implemented using our design methodology. Fig. 10 shows the systolic array implementation of the 8-bit DCT. A MATLAB simulator based on the simulation framework in Section IV was used to simulate the DCT. Since the DCT implementation is made up of a regular arrangement of identical processing elements (PE), we analyzed a single PE and extrapolated the results to the whole system.

The systolic array DCT implementation consists of 16 identical PE. Each PE has sixteen 2-input gates and sixty 4-input gates. The 2-input gates can be built using 4-input gates by fixing the remaining inputs to logic '1'. By using only 4-input gates, we can construct a very regular MQCA DCT implementation. The area overhead due to using only 4-input gates is 4.3%. The advantages of using such a regular layout include 1) ease of fabrication, 2) ease of adding redundancy to the circuit and 3) ease of clock control circuitry design. Furthermore, higher fan-in gates reduce the interconnect delay in MQCA. Table 6 lists the parameters of the MQCA based DCT. The critical path delay in our MQCA DCT is 884ns and the total energy dissipation is 5.1fJ.

Iso-Delay Comparisons with 45nm CMOS

Due to the large delay in MQCA, we analyzed CMOS in sub-threshold operation for iso-delay comparisons [16]. The design parameters for CMOS based DCT is listed in Table 7. Table 8 shows the power-performance numbers of both CMOS and MQCA implementations of DCT. Fig. 11 shows the area and energy consumption of both MQCA and CMOS 8-bit DCT implementations. The MQCA implementation shows 290X energy improvement over 45nm CMOS technology implementation. However, the use of a steel core is an overly optimistic assumption. Using parallel wires in

R_{eq} Of Different Clock Generators

Wire: $\frac{\text{resistivity}\times\text{cross-sectional area}}{\text{wire length}}$

MTJ: $\frac{\text{current source voltage}}{\text{MTJ switching current}}$

Solenoid: $\frac{4L\rho\left(R_o^2-R_i^2\right)}{\varphi^4}$

L=length,ρ=wire resistivity, φ=wire radius,
R_o=outer radius,R_o=inner radius

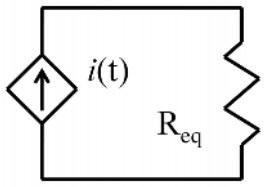

Figure 8. The lumped circuit model shown is used to model the technologies to convert current to magnetic fields

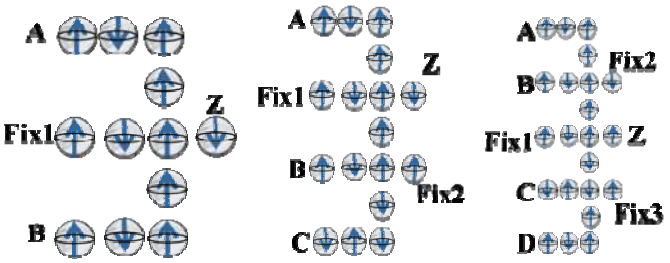

Figure 9. (a) 2-, (b) 3- and (c) 4-input MQCA gates are shown. Fixing different input magnets implements different logic functions. Fix1, Fix2 and Fix3 are used to configure the gates as listed in Table 4. '1' and '0' are as defined in Figure 1.

TABLE 4
MQCA Gate Configurations For Realizing Logic Functions Using Gates Of Figure 9

Gate	Fix1	Fix2	Fix3	$Z=\overline{\text{FUNCTION}}$
2-input gate	1	--	--	A+B
2-input gate	0	--	--	A.B
3-input gate	0	0	--	A.B.C
3-input gate	0	1	--	A.(B+C)
3-input gate	1	0	--	A+B.C
3-input gate	1	1	--	A+B+C
4-input gate	0	0	0	A.B.C.D
4-input gate	1	0	0	A.B+C.D
4-input gate	1	1	0	A+B +C.D
4-input gate	1	0	1	A.B +C+D
4-input gate	0	0	1	A.B.(C+D)
4-input gate	0	1	1	(A+B).(C+D)
4-input gate	0	1	0	(A+B).(CD)
4-input gate	1	1	1	A+B+C+D

TABLE 5
Delay, Energy And Area Of Basic MQCA Logic Cells

Cells	Delay (ns)	Energy (aJ)	Area (μm^2)
NAND 2	11.8	0.07	0.018
NOR 2	11.8	0.07	0.018
NAND 3	15	0.15	0.025
NOR 3	15	0.15	0.025
NAND 4	19	0.26	0.032
NOR 4	19	0.26	0.032
XNOR 2	19	0.26	0.032
Half-Adder	19	0.33	0.050
Full-Adder	38	0.6	0.082

ferrite core to generate magnetic fields, the MQCA DCT energy improvement reduces to 1.6X. Using silicon dioxide core solenoids to generate the magnetic fields, the MQCA DCT consumes 1700X more energy. All three MQCA DCT shows 46X area improvement over 45nm CMOS based DCT.

Technology Implications

The realization of fabricated MQCA systems using our methodology is hindered by difficulties in fabricating good on-chip solenoids and in designing low power clock

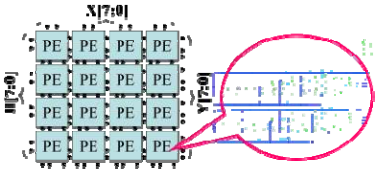

Figure 10. Implementation of 8x8 DCT using systolic arrays. The inset shows the logic gate implementation of a processing element (PE)

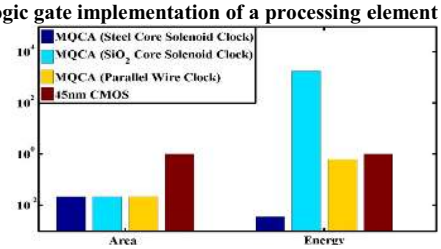

Figure 11. Graphical comparison of simulation results ormalized to 45nm CMOS results

TABLE 6
MQCA DCT DESIGN PARAMETERS

Nano-magnet Material	NiFe
Nano-magnet Anisotropy	1-D
Ku_2 (ergs/cm^3)	$3*10^5$
Alpha, α	0.1
Volume of nano-magnet(cm^3)	10^{-18}
Number of spins per nano-magnet	$8.7*10^4$
Spacing btw Magnets(t_{dm}),cm	$3*10^{-6}$
Clock Frequency	1.1MHz
Clocking Scheme	3-phase
Clock Generator	Solenoid
Solenoid turns per meter	10^9
μ_r, Relative Permeability of MQCA space	700 (Steel)
Number of magnets per generator	1
Magnetic field generated	750Oe
Electrical current requirement	0.2μA

TABLE 7
CMOS DCT DESIGN PARAMETERS

Operating regime	Sub-threshold
Supply Voltage	0.24V
Gate Length	45nm
Operating Frequency	1.1MHz

TABLE 8
DCT PERFORMANCE NUMBERS

	Frequency (MHz)	Power (nW)	Area (m^2)
MQCA (Steel solenoid core)	1.1	5.5	40
MQCA (SiO_2 solenoid core)	1.1	2.7E+6	40
MQCA (Parallel wires)	1.1	977	40
45nm Predictive CMOS Model (Sub-threshold Operation)	1.1	1600	1840

generation circuits. Better lithographic techniques need to be developed so that solenoids can be used to generate and distribute clocks in the MQCA chip. It has been reported that nano-coils as small as 0.2 m can be fabricated using Focused Ion Beam Chemical Vapor Deposition [15]. However, better techniques of fabricating these coils are needed to increase the power efficiency of using these coils to generate magnetic fields in MQCA chips. The use of current sources to generate magnetic fields also means that the clock generation circuit needs to be power efficient for MQCAs to retain their power advantage.

VII. SUMMARY & CONCLUSIONS

In this paper, we developed a device/circuit/system compatible simulation framework for evaluating MQCA systems. Novel clocking architectures and strategies for improving MQCA computation robustness and/or dataflow control were proposed. A design methodology for MQCA systems using novel clocking architectures and strategies was also developed. An MQCA based 8-bit DCT was implemented and evaluated using our simulation framework. Comparisons with 45nm CMOS based DCT show up to 290X energy and 46X area improvements (under optimistic assumptions) in the MQCA DCT implementation using 3-phase clocking with steel core solenoid. Results also show that parallel wire clocking is inefficient and may not lead to any performance/power advantage over standard 45nm CMOS technology.

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