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A Design of 8 fJ/Conversion-Step 10-bit 8MS/s Low Power Asynchronous SAR ADC for IEEE 802.15.1 IoT Sensor Based Applications

DEEKSHA VERMA[1], (Student Member, IEEE), KHURAM SHEHZAD[1], (Student Member, IEEE), DANIAL KHAN[1], (Student Member, IEEE), QURAT UL AIN[1], (Student Member, IEEE), SUNG JIN KIM[1], (Student Member, IEEE), DONGSOO LEE[2], (Student Member, IEEE), YOUNGGUN PU[1], (Member, IEEE), MINJAE LEE[3], KEUM CHEOL HWANG[1], YOUNGOO YANG[1], AND KANG-YOON LEE[1], (Senior Member, IEEE)

[1]Department of Electrical and Computer Engineering, Sungkyunkwan University, Natural Science Campus, Suwon-si 16419, South Korea
[2]Samsung Electronics, Suwon 443-743, South Korea
[3]School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology, Gwangju 61005, South Korea

Corresponding author: Kang-Yoon Lee (klee@skku.edu)

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ABSTRACT An energy efficient, low-power 10-bit asynchronous successive approximation register (SAR) analog-to-digital (ADC) converter with the sampling frequency of 8 MS/s is presented for IEEE 802.15.1 IoT sensor based applications. An improved common mode charge redistribution algorithm is proposed for binary weighted SAR ADC. The proposed method uses available common mode voltage (V_{CM}) level for SAR ADC conversion, and this method reduces the switching power by more than 12% without any additional DAC driver as compared to merged capacitor switching (MCS). Mathematical analysis of the proposed switching scheme results in the lower or equal power consumption for every digital code as compared to MCS. A two stage dynamic latched comparator with adaptive power control (APC) technique is used to optimize the overall efficiency. Furthermore, to minimize the digital part power consumption, a modified asynchronous SAR logic with digitally controlled delay cells is proposed. High efficiency with low power consumption makes it suitable for low power devices especially for IEEE 802.15.1 IoT sensor based applications. The proposed prototype is implemented using 1P6M 55 nm complementary metal-oxide-semiconductor (CMOS) technology. The measurement results that the proposed circuit achieves are 9.3 effective number of bits (ENOB) with signal-to-noise and distortion ratio (SNDR) of 58.05 dB at a sampling rate of 8 MS/s. The power consumption of SAR ADC is 45 μW when operated at 1 V power supply.

INDEX TERMS Adaptive power control (APC), asynchronous logic, Bluetooth low energy (BLE), capacitive DAC (CDAC), IEEE 802.15.1 IoT sensors, low power consumption, successive approximation register (SAR) ADC.

I. INTRODUCTION

Nowadays Internet of Things (IoT) are applicable for many applications such as sensor networks, wearable devices and health care [1]. For long battery life, wireless connectivity with low power is an essential requirement for the IoT applications. The IEEE 802.15.1 standard is the promising wireless connectivity [2]. Power efficiency and reduced area are the main features of Bluetooth Low Energy (BLE) transceivers, which make them more popular among the available choices. A low-noise amplifier amplifies the received high frequency signal, which is further demodulated to an intermediate frequency and through the band-pass filter. It is applied to the Analog-to-digital converters (ADCs) [3]. The block diagram of BLE Transceiver is shown in Fig. 1.

CMOS fabrication technologies have entered the submicron domain and transistor sizes are downscaling up

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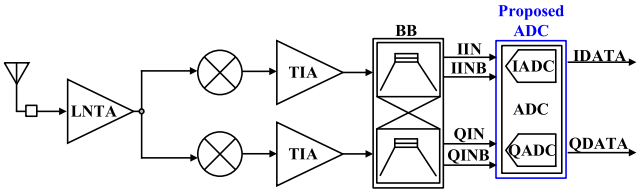

FIGURE 1. Block diagram of Bluetooth low energy transceiver.

to few nanometers. SAR ADCs are suitable for increasing scale-down technology and also can operate at a very low-power supply voltage. Excellent power efficiency and low analog complexity make the SAR ADC one of the best candidates for low energy applications [4]–[10].

The N-bit SAR structure requires N comparison cycles to complete the ADC conversion because of successive approximation conversion. Therefore, it is quite difficult to perform well in both resolution and throughput for SAR ADCs [11]–[13]. Low/medium resolution application, low to medium speed, low-power and area are the important characteristics of SAR ADCs [14], [15]. The SAR logic performs binary search algorithm through all possible bits to determine each bit successively. An asynchronous control signal is generated according to comparator state rather than the external clock. [16]. Thus, the conversion time (T_{CONV}) for asynchronous SAR ADC can be calculated as:

$$T_{CONV} = \frac{1}{F_S} - T_{sample} \tag{1}$$

where, T_{sample} is the sampling time and F_S is the sampling frequency.

A tri level switching scheme named as reverse V_{CM} based scheme which maintains good linearity without any driving and accuracy requirements on V_{CM} is represented in [6], and charge redistribution digital-to-analog converter (DAC) for the SAR ADC to reduce the area cost and power consumption and to promote the bandwidth is shown in [7]. For low supply voltage, asynchronous SAR assisted time-interleaved SAR ADC is considered in [10]. A dual-mode clock generator generates a low-jitter fixed-width sampling pulse for high-frequency operation while it generates a low-power-but-low-quality clock for low-frequency operation.

In asynchronous SAR ADC, back-to-back execution of each operation after the previous one is finished, makes it faster than the synchronous SAR ADC. This makes the asynchronous SAR ADC as an energy efficient and faster scheme as compared to synchronous SAR ADC. In order to cope-up with the need of high speed and energy efficient, many techniques have been applied [17]. The incomplete settling issues in DAC can be addressed by non-binary SAR ADCs. But to meet the matching requirement, layout cannot be designed properly, which can lead to the degradation in linearity and results in high order harmonics. Furthermore, for non-binary weighted SAR ADC, the digital error correction (DEC) logic is also too complicated [18]. Designing of redundant bit in binary weighted ADC is much easier than the non-binary weighted SAR ADC, but in every comparison cycle the compensation of incomplete settling is difficult for binary weighted SAR ADC [19]. An additional compensation capacitor is not required in binary-scaled recombination weighting method as proposed in [20]. But in high speed ADC case, power consumption cannot be overlooked because of DEC logic. Besides this, a call of an extra comparison cycle is required in the realization of [21] and [22].

This work presents an architecture in which several techniques have been applied which make its operation as an energy efficient and faster as well. The proposed switching architecture achieved a reduction in switching energy and improved linearity by determining whether the recent bit is similar as the first output comparison bit. The first comparison result will be sent to DAC, if the recent bit is same as the first comparison output bit, and if the recent bit is different, then the previous value of DAC will be reset to common mode voltage (V_{CM}). Asynchronous SAR Logic is implemented with dynamic logic in which sample time for each bit can be adjusted with trimming bits. A 0.5 fF custom designed unit capacitor is used to reduce the power consumption of analog part and modified rail-to-rail comparator with an adaptive power control (APC) control circuit, which results in low power consumption by reducing the active time for the comparator. This paper represents the optimization of power efficiency and area along with the speed of SAR ADC.

This paper is organized as follows. Section II discusses the main architecture for asynchronous SAR ADC for an I path and Q path and some of the Sub-blocks. Section III explains the ADC Core and its sub blocks, including design and implementation of improved common mode charge redistribution switching, the 0.5 fF custom designed unit capacitors, dynamic latched comparator with APC control and implementation of power-efficient asynchronous dynamic logic. Complete ADC measurement results are in Section IV and finally, conclusions are in Section V.

II. ASYNCHRONOUS SAR ADC ARCHITECTURE

In the design of BLE transceiver, the target resolution is 10 bits. To keep the low current consumption and faster operation, 10 bit resolution with reduced switching energy is applied to the ADC. The conversion rate is 8MS/s while the input frequency to the ADC can vary from the low frequency up to 2 MHz [2]. In a low power BLE transceiver, the low-noise amplifier (LNA) amplifies the noisy input signal as shown in Fig. 1. Then, through the baseband, the signal is delivered to ADC for modulating the lower frequencies. IIN, IINB, QIN and QINB are the differential input signals of I and Q path ADCs, respectively. The proposed 10-bit 8MS/s asynchronous SAR ADC is composed of DACs with binary-weighted capacitors (CDAC), high speed and low power dynamic latch comparator with APC technique and asynchronous SAR logic with DAC delay control as shown in Fig. 2. The binary architecture for CDAC in SAR ADC is more popular due to its ability to achieve comparatively better matching. The comparator with APC takes the voltages at the

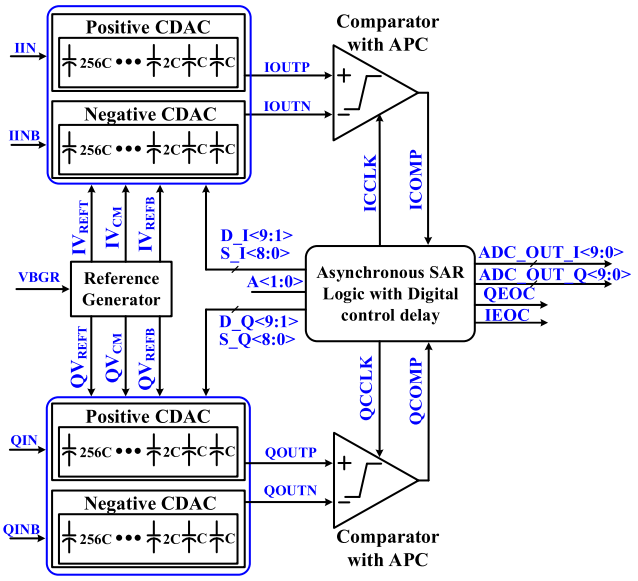

FIGURE 2. Architecture of the proposed SAR ADC.

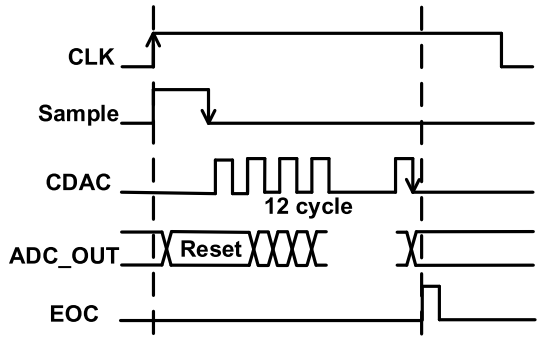

FIGURE 3. Timing diagram of the proposed SAR ADC.

bottom plates of the differential CDACs IOUTP and IOUTN as its inputs and determines output bits. Switching of DAC is controlled by the output bits of control logic from MSB to LSB. The differential CDACs are responsible for converting the output bit of control logic to analog values through switching capacitors at different voltages. One conversion is completed after N comparison cycles for N- bit SAR ADC.

The presented asynchronous SAR ADC is operating at 8 MS/s with the clock frequency of 8 MHz. The duty cycle of the clock signal is 75% and the whole conversion process is being done within the duty cycle of the clock. Digitally controllable delays have been added in asynchronous logic to control the conversion speed of each bit, which makes it optimized in the aspect of faster timing. Custom designed metal-oxide-metal (MOM) capacitors are used in CDAC to minimize the power consumption and the area of analog part. APC circuit has been used to reduce the overall power consumption of comparator. It controls the comparator's operation by turning it off when the outputs of the comparator are determined. For faster operation and reduction in overall size, 0.5 fF custom designed MOM unit capacitor is used in CDAC which also results in minimizing the overall power consumption of analog part of the ADC by reducing the switching current in CDAC.

Four CDACs and two comparators have been used for I/Q signals as shown in Fig. 2. Timing diagram of the proposed architecture is shown in Fig. 3. Reference voltage generator is common for I and Q path and provides voltages IV_{REFB}/ QV_{REFB} of 0.2 V, IV_{CM}/QV_{CM} of 0.5 V and IV_{REFT}/QV_{REFT} of 0.8 V. For I path SAR ADC receives the differential input signals IIN and IINB. The reference voltage generator generates V_{REFT}, V_{REFB}, and V_{CM} of values 0.8 V, 0.2 V and 0.5 V, respectively. A 10-bit CDAC provides the reference input signals IOUTP and IOUTN to the comparator. The Track-and-hold operation is done by the sampling switch and capacitors in the CDAC. Control signals D_I<9:1>, S_I<8:0>, D_Q<9:1> and S_Q<8:0> from asynchronous SAR logic with digital control delay block, controls the switching sequence of CDAC's and generates the comparator's clock signal ICCLK and QCCLK. Dynamic latched comparator generates control bits for asynchronous SAR logic after determining the signs of the voltage at the CDAC's output. On the completion of the successive approximation process, asynchronous SAR logic creates an End-of-Conversion (EOC) signal. In the proposed ADC architecture, we use the on-chip reference generator. To ensure the stability and low power, decoupling capacitors are used as on-chip and off-chip in the voltage reference circuit. On-chip decoupling results in better stability as compared to the off-chip decoupling. To minimize the number of pins, a fully integrated voltage reference is implemented. Besides, on-chip decoupling capacitors act as the AC driver for low power. The proposed on-chip reference voltage, which is similar to [9], with no extra pins. The switching noise at high frequency is suppressed by the on-chip decoupling capacitor effectively and it also helps in minimizing the settling time of the disturbed signals.

III. CIRCUIT IMPLEMENTATION

A. CAPACITIVE DAC

Many SAR ADC switching algorithms are presented for binary weighted CDAC architecture, but the voltage common mode based charge redistribution technique has been the most energy efficient nowadays. The CDAC is implemented with charge-redistribution topology [23]–[25]. The proposed scheme shows that the improved voltage common mode based charge redistribution algorithm in which static linearity and switching energy efficiency are improved by efficient selection of the time that individual binary capacitor is reset. Fig. 4 shows a 3-bit CDAC switching sequence. The improved switching technique is explained as follows: The top plates of all the capacitors are sampled at the common mode voltage (V_{CM}). At the same time, the bottom plates of the capacitors are initially sampled with the VIP and VIN for the positive and negative CDAC respectively. The total charge at the positive and negative input of the comparator is $Q_A = 4C(V_{CM}-V_{IP})$ and $Q_B = 4C(V_{CM}-V_{IN})$ and

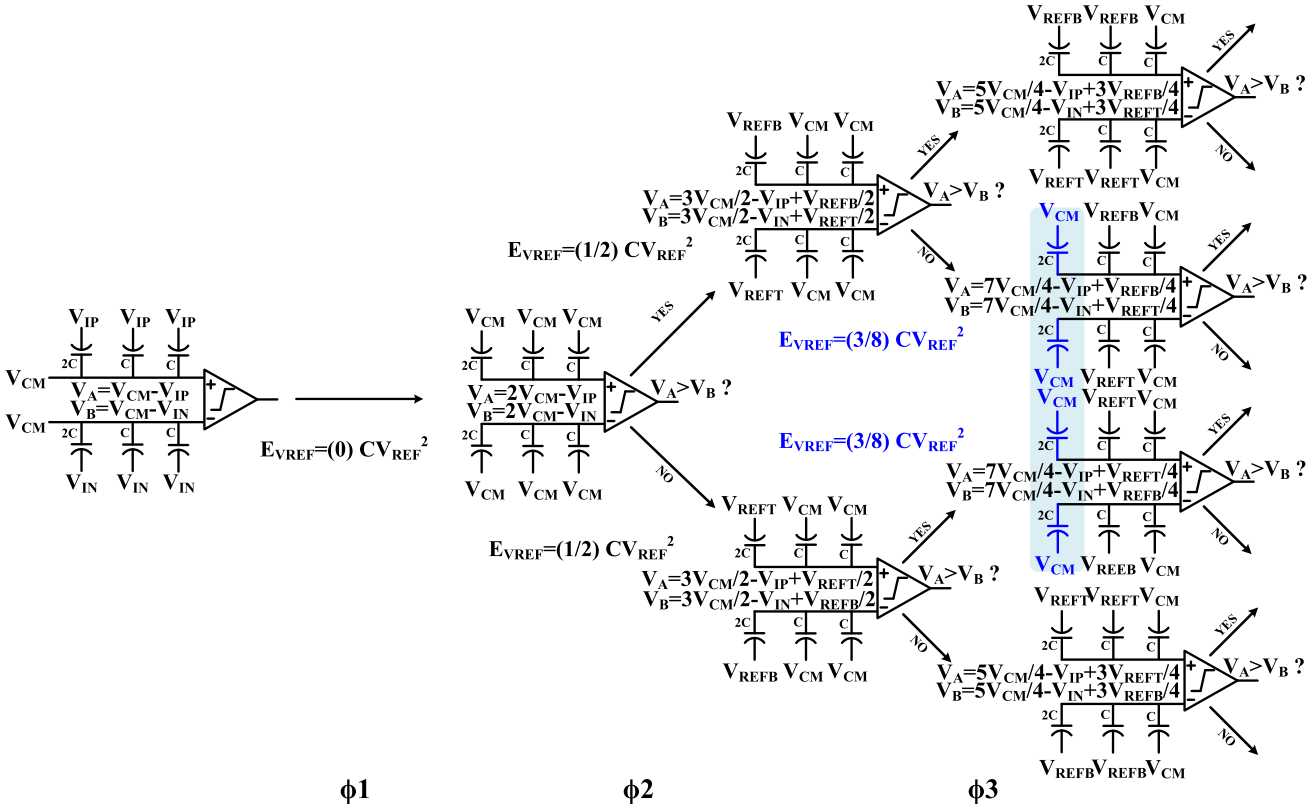

FIGURE 4. Proposed switching procedure for a 3-bit SAR ADC.

the energy requirement for each conversion is based on the previous code and the current code. Switching energy can be derived from the V_{REF}, where $V_{REF} = V_{REFT} - V_{REFB}$ and it can be determined by the calculation of positive and negative voltages of the MSB capacitor and multiplying by the switching capacitance. The energy at the phase $\phi 2$ EV_{REF} is shown as:

$$\phi 2 = EV_{REF} = \left[\left(\frac{1}{2} - \frac{C_{MSB}}{2C_T}\right) V_{REF} \times C_{MSB}\right] \times V_{REF} = \frac{CV_{REF}^2}{2} \quad (2)$$

where, C_T is the total capacitance, C_{MSB} is the MSB capacitor size and C is the LSB capacitor and the larger capacitors are composed of multiples of C.

The negative plates of all the capacitors are connected to the V_{CM}. The total charge at the comparator's positive input and at the comparator's negative input is $Q_A = 4C(V_A - V_{CM})$ and $Q_B = 4C(V_B - V_{CM})$, respectively. According to the law of conservation of charge, the total charge in both modes is the same, so the voltage levels at both sides is shown in Fig. 4.

In the next phase, if $V_A > V_B$, the comparator's output becomes high resulting in most significant bit (MSB) equal to '0' then the positive CDAC is charged at V_{REFB} and the negative CDAC is charged at V_{REFT}. The charge at the comparator's input is $Q_A = 2C(V_A - V_{REFB}) + 2C(V_A - V_{CM})$ and $Q_B = 2C(V_A - V_{REFT}) + 2C(V_A - V_{CM})$ respectively. If $V_A < V_B$, the comparator's output goes to low, resulting in MSB equals to '1' then the positive CDAC charged at V_{REFT} and negative CDAC charged at V_{REFB}. The charge at the comparator's input is $Q_A = 2C(V_A - V_{REFT}) + 2C(V_A - V_{CM})$ and $Q_B = 2C((V_A - V_{REFB}) + 2C(V_A - V_{CM})$.

Significantly less energy is consumed by the same direction switching in comparison to the opposite direction switching. To correct the previous voltage in opposite direction switching, required reference voltage should be generated, which is generated by overshoot. However, this is not the only option. Another solution is shown in Fig. 4 by resetting the previous capacitor to the V_{CM} and switching the recent capacitor to the opposite polarity. By this method, the capacitance connected with the reference voltage is minimized. Hence, the total supply reference capacitance is minimized before changing in the reference node voltage and additional charge is introduced from the supply. The energy at $\{1, 0\}$ conversion is shown as:

$$\phi 3 = EV_{REF} = \left[\left(\frac{1}{2} - \frac{C_{MSB-1}}{2C_T}\right) V_{REF} \times C_{MSB-1}\right] \times V_{REF} = \frac{3CV_{REF}^2}{8} \quad (3)$$

There is no additional energy required while previous capacitor is switched to the V_{CM} because it is switching in reset phase and all previous charges are differential and

cancelled on the capacitors across the shared V_{CM} node. Furthermore, in early stages, energy reduction will continue in the referenced capacitance due to the movement of virtual references in further stages. If the recent bit has opposite polarity from the previous bit, then the previous capacitor will be reset and a recent capacitor will be charged to the given positive and negative DAC to the opposite charge as proposed in this paper. To represent the code digitally, the reference voltage capacitance related to the current bit depends upon the previous bit and the next bit. The energy per code is shown as:

$$EV_{REF}(code) = \frac{V_{REF}^2}{2C_T}\left(\sum_{N=1}^{M-1} C_N \times \left[\sum_{S=2}^{N-1}\left(C_S\left(\overline{B_{P-1}\oplus B_{P+1}}\right)(-1)^{\left(\overline{B_C\oplus B_{P+1}}\right)}\right) + C_1\left(\overline{B_1\oplus B_2}\right)(-1)^{\left(\overline{B_N\oplus B_1}\right)} - C_N + C_T\right]\right) \quad (4)$$

where, N is the given stage, B_P is the previous stage bit and B_C is the current bit.

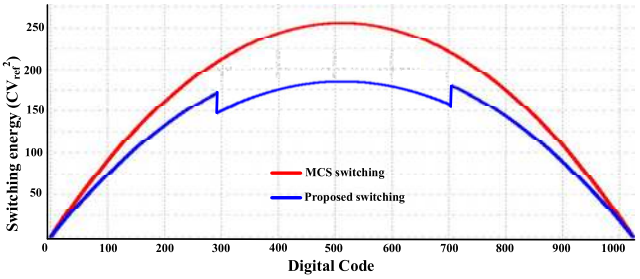

FIGURE 5. Simulation result of the switching energy of the employed switching method.

The behavioral simulation of per code energy is plotted in MATLAB as shown in Fig. 5. 10-bit SAR operation assigned to ($C*V_{REF}^2$) and reduction in energy can be observed for each code. The Unit capacitor is represented as C and supply voltage to the DAC is represented as Vref. For 10-bit case, monotonic switching energy [26] procedure and MCS consumes 255.5 CV_{REF}^2 and 170 CV_{REF}^2 while the proposed switching scheme consumes 149 CV_{REF}^2. The proposed common mode charge redistribution switching architecture results 12.5% reduction in average switching energy for uniform input probability density function (PDF) and 18.4% reduction for Gaussian PDF input. In MCS architecture, common mode redistribution technique reduces the switching energy from central codes by reducing the power of alternating codes. The proposed technique achieves 41.5% reduction in average switching energy as compared to [26]. To check the sensitivity due to capacitor mismatch, static performance of the proposed switching scheme based on behavioral simulation in MATLAB is shown in Fig. 6. The simulation is done without and with mismatch by considering 1 % unit capacitor mismatch [27], [28]. The simulation result for proposed CDAC is shown in Fig. 7.

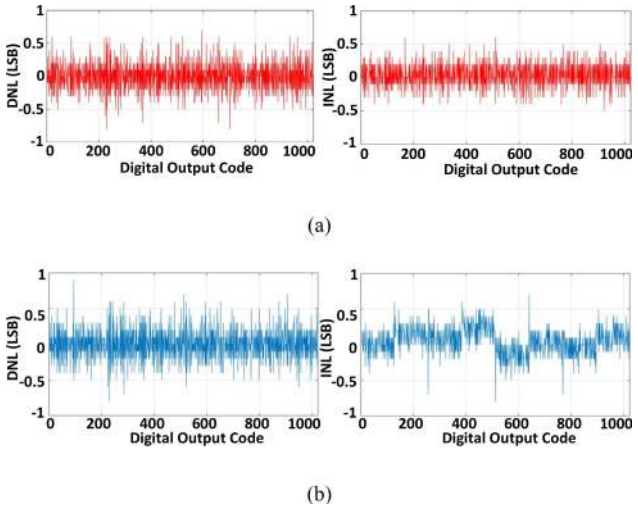

FIGURE 6. Behavioral model static performance of the proposed switching scheme (a) without mismatch (b) with 1% unit capacitor mismatch.

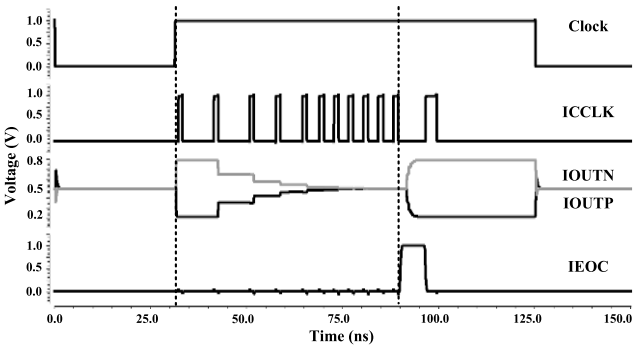

FIGURE 7. Simulation result of the CDAC switching.

In CDAC, the value of capacitor is doubled every time from LSB to MSB. The settling time of each interval for CDAC is based on $\tau = RC$, where R represents the sample switch resistance and capacitance in each bit is represented by C, which is controlled by adjusting the resistor's value to allow settling for a limited time. This can be done by adjusting the switch size resulting in different conversion time and switch size for each cycle. MOM capacitor layout is implemented by using metal 4 and metal 5 and verified by using electromagnetic extraction (EMX) simulation. Inner metals 4 and 5 are used with minimum spacing and width to minimize the unwanted parasitics between each terminal and ground as shown in Fig. 8. To minimize the mismatch, dummy capacitor array is added in the layout. CDAC layout is done with rectangular layout and dummy capacitor layout. Binary scaling is verified in top layout parasitics extraction with the capacitance of 0.514 fF and 130.3 fF for C and 256C, respectively.

IV. DYNAMIC LATCH COMPARATOR WITH APC

For fast operation and high resolution, a rail-to-rail comparator is used in ADC core of the proposed architecture,

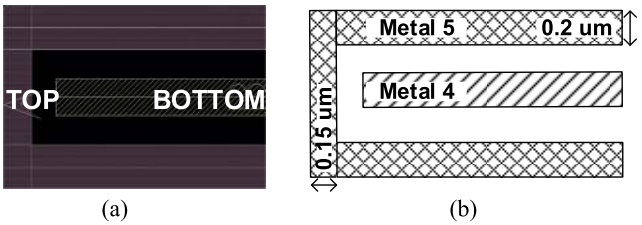

FIGURE 8. 0.5 fF MOM capacitor layout.

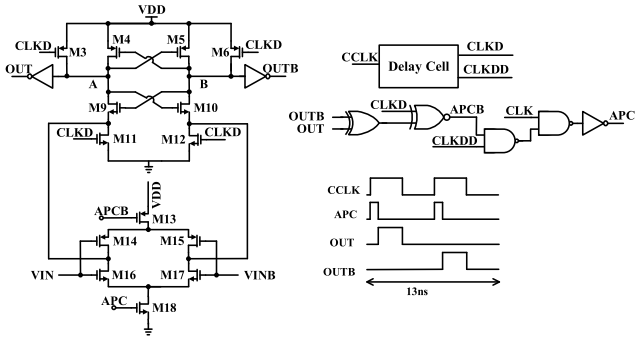

FIGURE 9. Schematic of a dynamic latch comparator with APC.

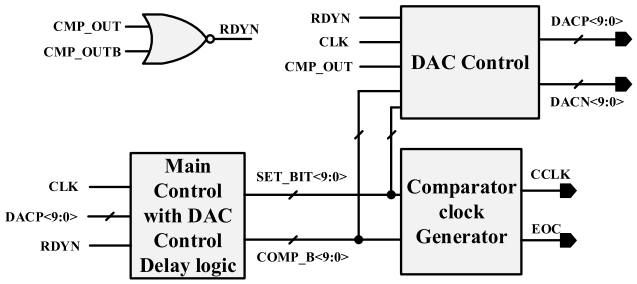

FIGURE 10. Simplified block diagram of asynchronous logic.

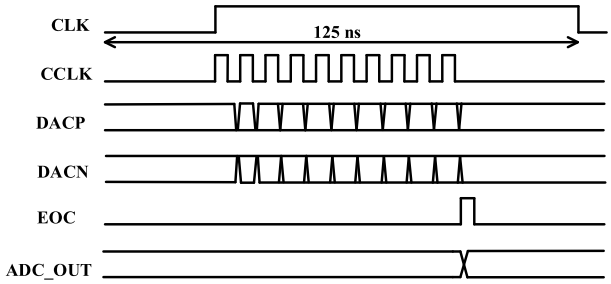

FIGURE 11. Timing Diagram of the proposed asynchronous logic.

which contains the dynamic latch and pre-amplifier as shown in Fig. 9. VIN and VINB are the differential input reference signals for the comparator, CCLK is the clock signal and OUT and OUTB are the output of the comparator. For rail-to-rail input the pre-amplifier has differential input pair as N-type and P-type. Due to static current after the comparison operation the power efficiency is poor in conventional dynamic latched comparator. In the proposed architecture, the pre-amplifiers static current can be blocked through the APC logic after pre-amplifying and output decision, hence power efficiency of ADC is improved.

As dynamic latch architecture can introduce large input referred offset, which is not suitable for medium and high resolution ADCs, we have reduced its effects by increasing the sizes of the input transistors in differential pair [29]–[32]. In addition to this, we have used an APC circuit which reduces the overall power consumption of the comparator. When CCLK is changed from low to high, APC signal changes to high and turns on the preamplifier. When the comparison is finished, OUT goes to high and OUTB goes to low and output of XOR_A goes to high. Now both input terminals of XOR_B are high, APC signal changes to low and DC supply of the preamplifier is turned-off.

V. ASYNCHRONOUS SAR LOGIC

In the proposed architecture, the implementation of digital logic is to minimize the complexity from current dynamic logic. Combinational logics are implemented with transistors. Asynchronous logic is comprised of main control, DAC control and a comparator clock generation block. Fig. 10 shows the simplified block diagram of the logic for the SAR ADC. Fig. 11 shows the timing diagram of the proposed asynchronous logic. DAC control, and a comparator clock generator are implemented after main control and delays for DAC control. The comparator clock generator needs to generate a high-level at the input of the comparator clock when comparator-state is shown in one of the cycle of main control. Thus, the comparator clock generator is a logic operation for the all cycle's states, and the complementary logic functionality is used to implement it:

$$CCLK = \sum_{cycle(i=0)}^{10} \overline{C_1}, \overline{C_{2,i}} \tag{5}$$

Leakage current is the most prominent in consuming power at low sampling frequencies and leakage current is directly dependent on the implemented logic state of the state-machine. In this design, when the CLK is 0, then the SAR logic is in a standby state and then the leakage current is minimized.

To minimize the power consumption in digital part, asynchronous SAR logic is used. With asynchronous SAR logic, instead of a high reference clock, a sampling rate of 8 MHz can be implemented with only one clock resulting in reduced current consumption. It generates internal control signals and eliminates the need of global synchronization at each bit cycle as shown in Fig. 12. Furthermore, a modified asynchronous SAR control logic is proposed to optimize the delay between comparator's operation and DAC switching. In case of a general asynchronous controller, there is a specific delay for each cycle when the comparison is made, but in the proposed modified logic control there is a scalable delay for different comparison from LSB to MSB. Delay cell, which can be externally controlled by A<1:0> is shown in Fig. 13. To reduce the complexity and current consumption,

TABLE 1. Performance summary and comparison.

Parameter	JSSC' 16 [10]	JSSC' 11 [23]	VLSI' 10 [33]	ISSCC' 10 [34]	TCAS' 15 [35]	TCAS' 19 [36]	This work
Technology	65 nm	90 nm	180 nm	90 nm	130 nm	180 nm	55 nm
Resolution (bit)	12	8	10	8	10	10	10
Supply (V)	0.6	1	1	1	1	1.8	1
Sampling Rate (MS/s)	10	10.24	10	10.24	1.1	5	8
Power (W)	83 µ	26.3 µ	98 µ	69 µ	15.6 µ	2.35 m	45 µ
ENOB (bit)	10.4	7.77	9.83	7.74	8.8	9.13	9.46
DNL (LSB)	0.24	-0.7/+0.3	-0.3/+0.2	-0.5/+0.3	-0.8/+0.6	-	-0.9/+0.8
INL (LSB)	0.45	-0.8/+0.1	-0.3/+0.2	-0.3/+0.2	-1.4/+1.6	-	-1/+0.84
FOM (fJ/step)	6.2	12	63	30	31.8	845	8

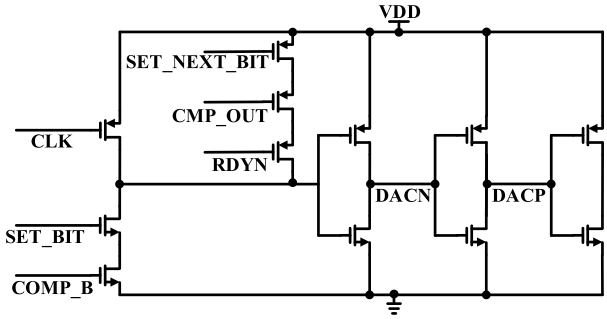

FIGURE 12. Schematic of a DAC control.

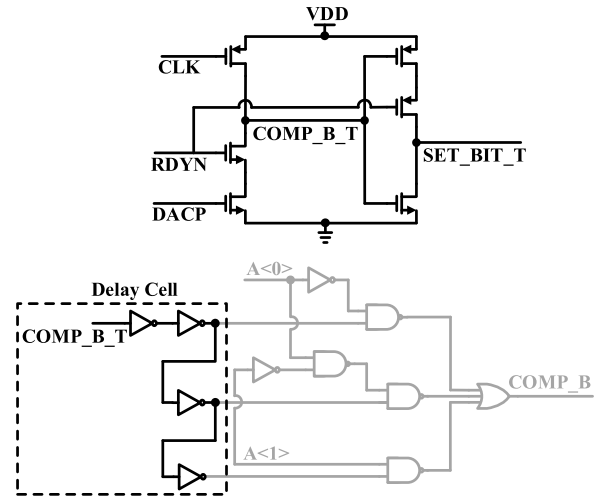

FIGURE 13. Schematic of the main control with DAC control delay logic.

dynamic logic is used for implementation. The same function can be done with fewer transistors than the complementary logic [25].

VI. MEASUREMENT RESULTS

The proposed prototype of SAR ADC is implemented and tested with 55 nm CMOS process. The die photograph of the whole structure is shown in Fig. 14 and the measurement setup for the ADC test board is shown in Fig. 15. The area

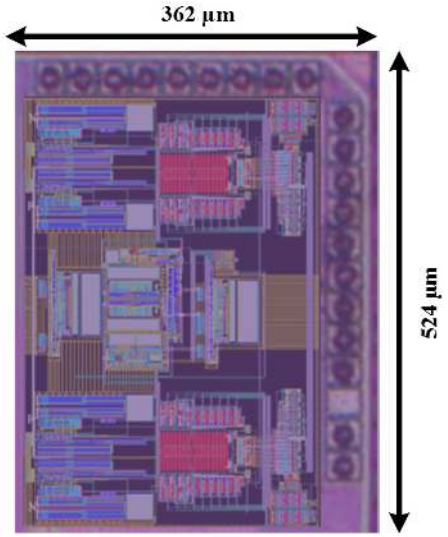

FIGURE 14. Die photograph of the proposed ADC.

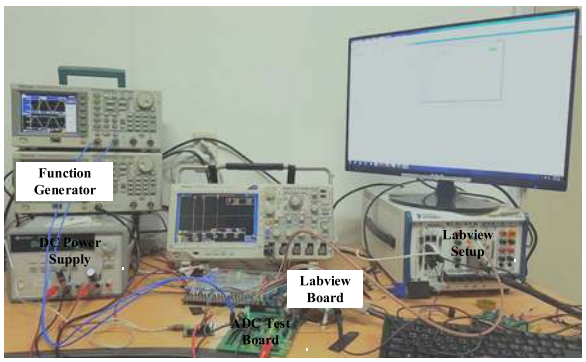

FIGURE 15. Measurement Setup for the proposed ADC.

of the proposed ADC is 362 x 524 μm^2 and it operates at 1V power supply at 8MS/s sampling speed.

The FFT spectrum of the proposed ADC operated in differential operation is presented in Fig. 16. It achieves an ENOB of 9.35 bits, SNDR of 58.053 dB and SFDR of 65.992 dB at

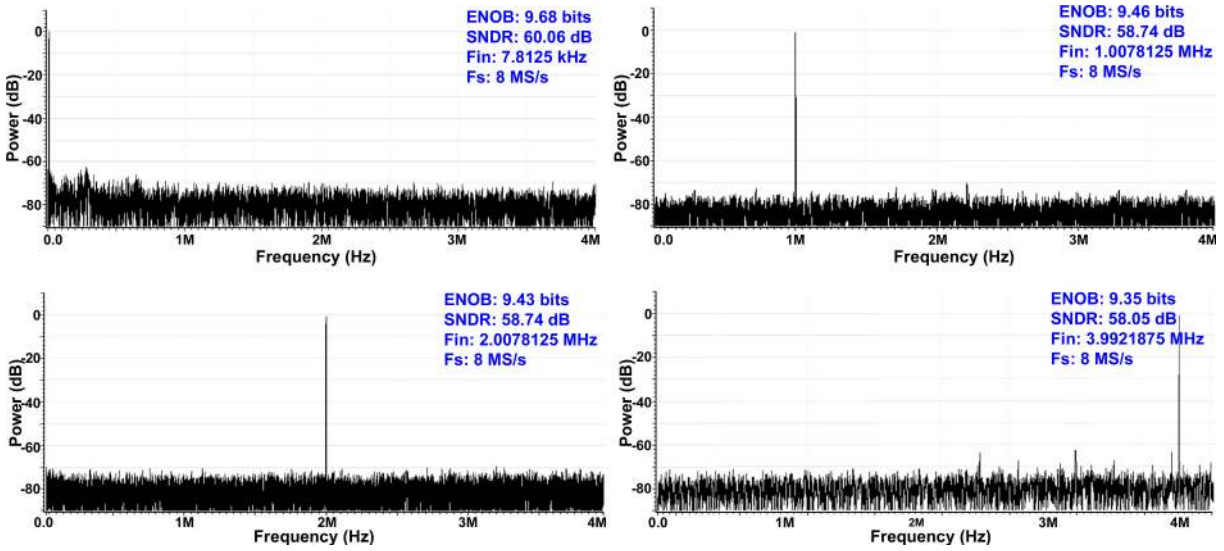

FIGURE 16. Measured dynamic performance at different frequencies @ nyquist input.

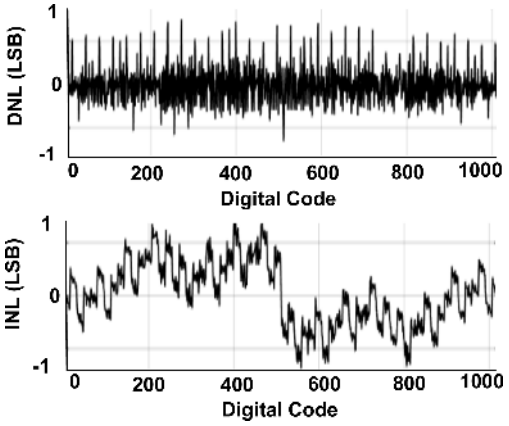

FIGURE 17. Measured INL and DNL results.

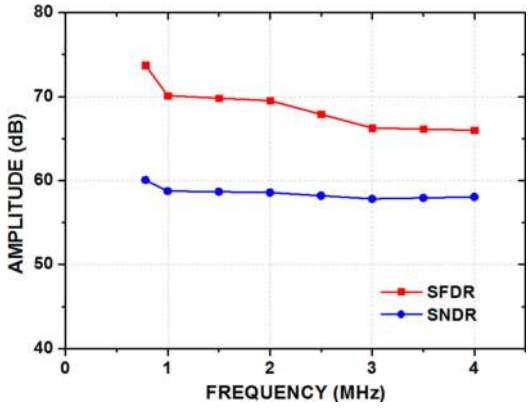

FIGURE 19. SFDR and SNDR versus input frequency at 8MS/s conversion rate.

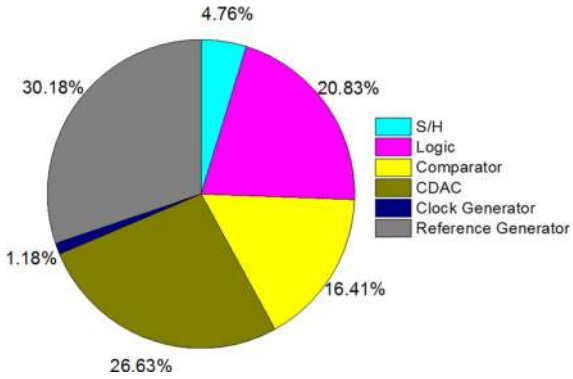

FIGURE 18. Power breakdown of ADC.

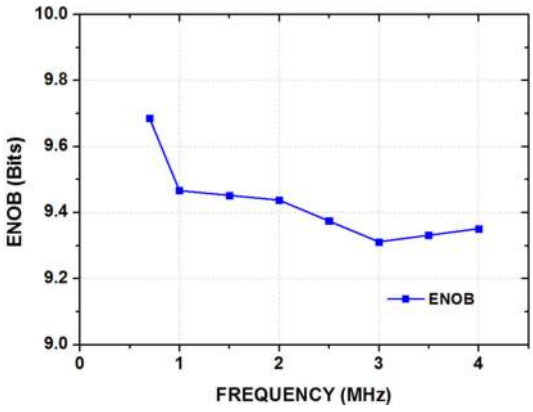

FIGURE 20. ENOB versus input frequency at 8MS/s conversion rate.

the nyquist input signal frequency at a sampling rate of 8 MS/s and a full-scale input range of 600 mVp-p.

The measured DNL and INL of the proposed ADC are shown in Fig. 17, which represents peak DNL error and the INL in the proposed ADC are −0.91 to 0.89 and −1 to 0.84, respectively. The power breakdown of ADC is represented in Fig. 18. Fig. 19 shows the SNDR and SFDR levels trend

and Fig. 20 depicts the ENOB trend of the proposed ADC with different input frequencies at 8MS/s sampling rate.

Table 1 shows the measured performance summary and comparison with other ADC structures. To compare the presented 10-bit 8MS/s ADC with resolution, different sampling rates and figure-of-merit (FOM) of other ADCs works are essential. FOM is calculated as given [34]:

$$FOM = \frac{POWER}{\min\{F_S, 2 \times ERBW\}2^{ENOB}} \tag{6}$$

where, Power and F_S represent the power consumption of ADC and the sampling frequency, respectively and ERBW is the effective resolution bandwidth.

The current ADC core shows a FOM of 8 fJ/step, while for a whole structure it is 75.3 fJ/step. The FOM of whole structure includes the reference generator and two ADC cores for I and Q paths. Table 1 shows the comparison with other state-of-the-art SAR ADC [10], [23], [33]–[36] and summarizes the performance of proposed asynchronous SAR ADC.

VII. CONCLUSION

This paper presents a 10-bit low power asynchronous SAR ADC for IEEE 802.15.1 IoT sensor based applications. The proposed prototype of ADC is implemented in 55-nm CMOS process. To minimize the power consumption in analog part, very small size custom designed 0.5 fF MOM capacitors are used in CDAC. The proposed switching technique reduces the switching power consumption by 12 % as compared to MCS. The employed switching strategy improves or equalizes the energy efficiency requirements for each code by utilizing the common mode reference in DAC. It guarantees the consequently improved linearity and common-mode voltage level of the comparator unchanged. A modified two-stage dynamic latch comparator is used for the fast operation and high resolution. APC circuit is used along with the comparator to control its operation resulting in enhancing overall energy efficiency. Compact control logic and high-speed dynamic latched are implemented, to enhance energy efficiency and the operation of proposed SAR ADC. Furthermore, modified asynchronous SAR logic is implemented with adjustable delays for different comparison from LSB to MSB. The proposed prototype achieved a FoM of 8 fJ/conversion-step. The proposed structure occupied an area of 362 μm $\times$ 524 μm. The measurement results show that it achieved an ENOB of 9.3 bits and SNDR of 58.05 dB at a sampling rate of 8 MS/s with 1 V power supply.

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DEEKSHA VERMA (Student Member, IEEE) received the B.S. degree from CSJM University, Kanpur, India, and the M.S. degree in information and communication engineering from Gautam Buddha Technical University, Lucknow, India. She is currently pursuing the Ph.D. degree with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. Her research interests include design of high-performance data converters including SAR and power IC including DC-DC converters.

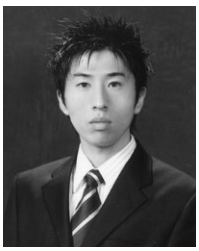
KHURAM SHEHZAD (Student Member, IEEE) received the B.S. degree in electrical engineering with specialization in telecommunication from Government College University, Faisalabad, Pakistan. He is currently pursuing the combined M.S. and Ph.D. degree in electrical and computer engineering with the College of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. His research interests include design of high performance data converters, including SAR and SD ADC, and CMOS RF transceiver.

DANIAL KHAN (Student Member, IEEE) received the B.S. degree in electrical and electronic engineering from the University of Engineering and Technology, Peshawar, Peshawar, Pakistan. He is currently pursuing the combined M.S. and Ph.D. degree with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. His research interests include wireless power transfer and power IC design.

QURAT UL AIN (Student Member, IEEE) received the B.S. degree in electronic engineering from International Islamic University, Islamabad, Pakistan. She is currently pursuing the combined M.S. and Ph.D. degree with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea. Her research interests include power IC design, analog, digital, and mixed circuit design.

SUNGJIN KIM (Student Member, IEEE) received his B.S. degree from the Department of Electronic Engineering at Inje University, Kimhea, Korea, in 2014. He is currently working toward the Combined Ph.D. & M.S degree in School of Information and Communication Engineering, Sungkyunkwan University, South Korea. His research interest include CMOS RF transceiver and wireless power transfer systems.

DONGSOO LEE (Student Member, IEEE) received the B.S. degree in electronic engineering from Konkuk University, Seoul, South Korea, in 2012, and the M.S. and Ph.D. degrees in electronic engineering from Sungkyunkwan University, Suwon, South Korea, in 2014 and 2018, respectively. He joined Samsung Electronics, Suwon, in 2018, where he has been involved in the circuit design of Phase Locked Loop, Frequency Doubler, and RF attenuator. His research interests are focused on CMOS RF transceiver and phase locked loop, silicon oscillator, and sensor interfaces design.



YOUNGGUN PU (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the Department of Electronic Engineering, Konkuk University, Seoul, South Korea, in 2006, 2008, and 2012, respectively. His research interest is focused on CMOS fully integrated frequency synthesizers and oscillators and on transceivers for low-power mobile communication.

MINJAE LEE received the B.Sc. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1998 and 2000, respectively, and the Ph.D. degree in electrical engineering from the University of California, Los Angeles, in 2008. In 2000, he was a Consultant with GCT semiconductor, Inc., and Silicon Image Inc., designing analog circuits for wireless communication and digital signal processing blocks for Gigabit Ethernet. He joined Silicon Image Inc., Sunnyvale, CA, USA, in 2001, developing Serial ATA products. In August 2008, he joined Agilent Technologies in Santa Clara, CA, USA, where he was involved with the development of next generation high-speed ADCs and DACs. Since 2012, he has been with the School of Information and Communications, Gwangju Institute of Science and Technology, Gwangju, South Korea, where he is currently an Assistant Professor. He was a recipient of the 2007 Best Student Paper Award at the VLSI Circuits Symposium in Kyoto, Japan. He received the GIST Distinguished Lecture Award, in 2015.

KEUM CHEOL HWANG received the B.S. degree in electronics engineering from Pusan National University, Busan, South Korea, in 2001, and the M.S. and Ph.D. degrees in electrical and electronic engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2003 and 2006, respectively. From 2006 to 2008, he was a Senior Research Engineer at the Samsung Thales, Yongin, South Korea, where he was involved with the development of various antennas including multiband fractal antennas for communication systems and Cassegrain reflector antenna and slotted waveguide arrays for tracking radars. He was an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, South Korea, from 2008 to 2014. In 2015, he joined the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include advanced electromagnetic scattering and radiation theory and applications, design of multiband/broadband antennas and radar antennas, and optimization algorithms for electro-magnetic applications. Prof. Hwang is a Life Member of KIEES, and a member of IEICE.

YOUNGOO YANG was born in Hamyang, South Korea, in 1969. He received the Ph.D. degree in electrical and electronic engineering from the Pohang University of Science and Technology (Postech), Pohang, South Korea, in 2002. From 2002 to 2005, he was with Skyworks Solutions Inc., Newbury Park, CA, USA, where he designed power amplifiers for various cellular handsets. Since March 2005, he has been with the School of Information and Communication Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor. His research interests include power amplifier design, RF transmitters, RFIC design, integrated circuit design for RFID/USN systems, and modeling of high power amplifiers or devices.

KANG-YOON LEE (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Seoul National University, Seoul, South Korea, in 1996, 1998, and 2003, respectively.

From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, USA, where he was the Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was an Associate Professor with the Department of Electronics Engineering, Konkuk University. Since 2012, he has been with College of Information and Communication Engineering, Sungkyunkwan University, where he is currently a Professor. His research interests include implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system design.