A Design Optimisation Tool for Maximising the Power Density of 3-Phase DC-AC Converters Using Silicon Carbide (SiC) Devices

DOI:
10.1109/TPEL.2017.2705805

Document Version
Accepted author manuscript

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

A Design Optimisation Tool for Maximising the Power Density of 3-Phase DC-AC Converters Using Silicon Carbide (SiC) Devices

Ian Laird, *Member, IEEE,* Xibo Yuan, *Senior member, IEEE,* James Scoltock, *Member, IEEE* and Andrew J. Forsyth, *Senior member, IEEE*

***Abstract*—The emergence of wide-bandgap devices, e.g. silicon carbide (SiC), has the potential to enable very high-density power converter design with high-switching frequency operation capability. A comprehensive design tool with a holistic design approach is critical to maximise the overall system power density, e.g by identifying the optimal switching frequency. This paper presents a system level design tool that optimises the power density (volume or mass) of a 3-phase, 2-level DC-AC converter. The design tool optimises the selection of the devices, heatsink and passive components (including the design of the line, EMI and DC-link filters) to maximise the power density. The structure of the optimisation algorithm has been organised to reduce the number of potential design combinations by over 99%, and thus produces fast simulation times. The design tool predicts that when SiC devices are used instead of Si ones, the power density is increased by 159.4%. A 5 kW, 600 V DC-link, 3-phase, 2-level DC-AC converter was experimentally evaluated in order to confirm the accuracy of the design tool.**

***Index Terms*—Silicon Carbide (SiC), Design Optimisation, Power density, Switching frequency, DC-AC converters**

I. Introduction

THE CONTINUING technological development in the areas of electric and hybrid electric vehicles (EVs and HEVs), more electric aircraft (MEA) and portable consumer electronics has lead to a greater desire for power converter designs that are not only robust and efficient, but also achieve the highest possible power density [1], [2]. For example, HEVs typically require converters rated at 10 to 20 kW for highway cruising and 60 to over 100 kW for accelerating. Without a high power density system, these demands can force vehicle designers to eliminate certain amenities, such as a full size spare tyre, in order to accommodate all the hybrid components [2]. Similarly for aerospace applications, light and compact converters enable the replacement of the mechanical, hydraulic and pneumatic systems with electrical systems for generation, actuation, distribution and hybrid propulsion systems, the so called MEA.

One of the major factors in determining what power density can be achieved is the component selection. This includes the selection of:

- the switching devices and/or modules (MOSFET, BJT, IGBT);
- the cooling method (heatsink, fan, cold plate); and
- the passive components (line filter, EMI filter, DC-link capacitor, boost inductor)

Improving any of these components will produce higher power densities, however it is the recent advances in wide bandgap (WBG) technology that has created the best opportunities for increasing the power density. WBG devices, such as silicon carbide (SiC), possess properties that are superior to that of silicon (Si). Properties of SiC include:

- a higher critical electrical field which produces higher breakdown voltages from a smaller die thickness than Si and hence lowers the conduction resistance. This makes SiC devices superior to Si in the 1.2-1.7 kV range [3].
- higher thermal conductivity which allows more heat to be dissipated from a device subject to a smaller temperature differential.
- higher operating temperatures of up to 400°C as compared to the maximum 150°C limit that applies to Si, however package limitations prevent this limit from being reached.
- a higher current density of approximately 2 to 3 times that of Si [4].
- the ability to create unipolar power devices (MOSFETs, JFETs, etc.) at breakdown voltages $\geq$ 1.2 kV resulting in superior dynamic performance and lower switching energy losses than Si IGBTs. [5] showed that an all-SiC switch / free-wheeling diode combination provided a 70% reduction in switching losses compared to an all-Si combination.

As a result of the lower conduction and switching losses, along with higher thermal conductivity and operating temperatures, SiC devices can use smaller heatsinks to improve power density. Additionally, the potential for higher frequency operation reduces the size of the various inductors and capacitors needed to limit the ripple currents and voltages within the circuit. These attributes have been taken advantage of to produce converters of high power densities such as those

This work was supported by the UK EPSRC National Centre for Power Electronics under Grant EP/K035096/1 and EP/K035304/1.

I. Laird and X. Yuan are with the Electrical Energy Management Group (EEMG), Department of Electrical and Electronic Engineering, The University of Bristol, Bristol BS8 1UB, UK (e-mail: ian.laird@bristol.ac.uk; xibo.yuan@bristol.ac.uk).

J. Scoltock and A. J. Forsyth are with the School of Electrical and Electronic Engineering, The University of Manchester, Sackville Street, Manchester M13 9PL, UK (e-mail: james.scoltock@manchester.ac.uk; andrew.forsyth@manchester.ac.uk).

Corresponding author: Xibo Yuan; Postal address: Department of Electrical and Electronic Engineering, Merchant Venturers Building, Woodland Road, Bristol, BS8 1UB, UK; Telephone number: +44 01179545186; Fax: +44 01179545206; e-mail: xibo.yuan@bristol.ac.uk

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

shown in [6]–[8].

However, what is not clear is exactly how much SiC devices improve the power density. For the example of a 3-phase, 2-level DC-AC converter, whilst SiC devices can reduce the size of the line filter and DC-link capacitor by increasing the switching frequency, it may not produce a design that is smaller overall due to, firstly the heatsink size increasing with the switching frequency, and secondly the complex relationship between the component values of the electromagnetic interference (EMI) filter and the switching frequency [9]. Since SiC MOSFETs, in particular, open up the potential switching frequency range for a multi-kW DC-AC converter to several hundred kHz, it becomes paramount to be able to determine what exactly is the optimal switching frequency from the system power density point of view. Also, since SiC devices are more expensive than their Si counterparts, the overall power density of a SiC converter must increase by a sufficient amount in order to justify their usage over Si. Given that this trade-off should be made for every new design, an engineer would greatly benefit from a design optimisation tool that can quickly evaluate the effect that various types of semiconductor devices have on the overall power density of the converter. As the tool needs to optimise the design at the system level, a holistic design approach that considers all the component specifications and constraints in unison will be essential.

In order to create a design tool such as this, all the interdependencies between the various components need to be properly understood so that decisions that are made as part of the design process in regard to one component will not adversely affect other parts of the circuit. To this effect, research has already been carried out into determining the design equations that govern the potential power density of a converter. [10] performed calculations to estimate the power densities of Si and SiC DC-DC converters. It predicted that a 7kW DC-DC (100V/2kV) converter using Si devices and operating at a 50 kHz switching frequency and a temperature of 150°C would have an efficiency of 85%. By comparison the SiC version was predicted that by operating at 500 kHz and 300°C, it could achieve an efficiency of 89% and improve the power density by 50% over that of the Si version. Similarly [11] predicted that by 2025, converters fully utilising SiC devices will be able to reach power ratings of 1 MW that will be 1/50 of their former size. [12] analysed many of the key components that determine the power density of a converter, including the thermal management, magnetic devices, EMI filters and DC-link capacitors. While in-depth discussions were given, no converter was constructed for experimental validation. [13] further expanded on this work by developing an automatic optimisation algorithm to maximise the power densities of both a phase-shift and a series-parallel resonant DC-DC converter that were designed for a telecom power supply application. The work is experimentally verified however the approach to the problem involves optimising the geometry of a single custom-designed integrated heatsink and inductor/transformer rather than a range of off-the-shelf components. Similarly the capacitor volume prediction is made by extrapolating the capacitance-volumetric density of a single reference component, chosen for the specific design, rather than searching through a database of components which possesses a wide range of capacitance densities. In [14] a systematic evaluation methodology was used to optimise and compare several different AC-AC converter topologies utilising SiC devices, however the simulation tool was not validated experimentally. The key design parameters of the optimisation included the switching frequency, modulation scheme and passive values in order to access their impact on the converter's losses, harmonics, EMI, control and protection. [15] outlines the design optimisation of a single-phase power factor correction (PFC) converter with 2 interleaved boost cells. The converter is rated at 300W and covers the optimisation of the boost inductor, output capacitor, semiconductor selection and the differential mode (DM) and common mode (CM) filters. The optimised design is carried on a small database of components and the performance of the converter is experimentally verified, however while it uses SiC devices for the diodes, it uses Si devices for the switches. Similarly [16] outlines the optimisation process for the passives and heatsink of an interleaved boost converter which uses SiC devices for the diodes but Si CoolMOS devices for the switches. In [17] an optimisation process for a water-cooled 50-kW 3-phase DC-AC converter was discussed without experimental verification.

In practice a converter design is not just limited by the theoretical power density limits but also by the range of components that a design engineer has at their disposal. Although previous research efforts have focused on the governing design equations, as stated above, there has not been much consideration given to developing an automated design tool that can produce a high power density converter by selecting a set of components from a range of common electronic supplier component databases. More critically, the theoretical optimisation and prediction may not agree with the real component characteristics. This paper has highlighted which components differed the most from manufacturer datasheet information and needed to be paid the most attention to in a practical design. Additionally, this paper focuses on the design optimisation of SiC MOSFET based converters. The SiC MOSFET is likely to be the preferred choice compared to the SiC BJT, JFET, etc. because of its normally-off state and simpler gate drive requirements. This paper has carried out extensive characterisation of SiC MOSFET devices in order to provide accurate models for the design tool. It has been demonstrated that the SiC MOSFET converter can operate up to 100 kHz with an efficiency of 97.5%. Finally, this paper outlines a system level design tool that optimises the power density (volume or mass) of a 3-phase, 2-level DC-AC converter. The design tool selects from a database the combination of device, heatsink and passive components that will produce the highest power density. Included in the automated process is the design of the line, EMI and DC-link filters. The structure of the optimisation algorithm has been organised to reduce the number of potential design combinations by over 99%, and thus produces fast simulation times. In addition, the design tool is used to compare the power densities of 3-phase, 2-level DC-AC converters using either SiC or Si power devices. With the design tool, a power density of 3.585 kW/L can be achieved with a SiC MOSFET converter by searching the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

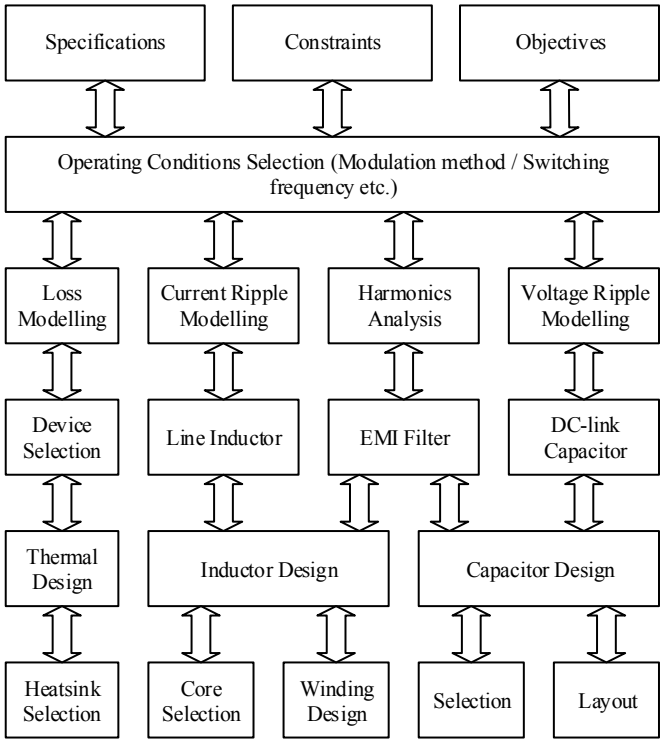


Fig. 1. Overview of the operational structure of the design optimisation tool

optimal switching frequency as compared to 1.426 kW/L for a Si IGBT converter.

The paper is organised as follows. Section II overviews the design tool, discussing its various component models through way of a design example. Section III describes the operation of the optimisation algorithm and discusses how the algorithm's structure can be altered to improve its computational efficiency. Section IV outlines the experimental work carried out on a 5 kW, 600 V DC-link SiC MOSFET based 3-phase inverter, in order to assess the accuracy of both the manufacturer data used in the design tool and the results of the design tool for the 2-level converter using SiC devices. Finally conclusions are drawn in section V.

II. Design Optimisation Tool Overview

The design optimisation tool is composed of a set of inter-dependent component models, as shown in Fig. 1, each of which are responsible for selecting and optimising a specific component of the converter. The component models can be categorised into one of three main areas; device loss modelling, heatsink design and passive components design. This section discusses each of these areas by outlining the fundamental equations and selection criteria that govern the models contained within them. To aid the discussion a design example, based on the specifications and constraints given in Table I, will be used to demonstrate the operation and outputs of each of the component models. The objective of the example will be to minimise the overall volume, and by effect the weight, of the converter.

TABLE I
Design Example Specifications and Constraints

Specification	Value
Rated Power (P_o)	5 kW
DC-link voltage (V_{dc})	600 V
Fundamental frequency (f_0)	400 Hz
Modulation index (M)	0.9
Power factor (PF)	0.99
Maximum junction temperature (T_j)	125 °C
Ambient temperature (T_a)	40 °C
Maximum output current ripple (ΔI_o)	10% of $\hat{I}_o$
Maximum DC-link voltage ripple (ΔV_{dc})	0.5% of V_{dc}
Minimum converter efficiency (η)	98%
EMI limit standard	DO-160E

A. Devices: Loss Modelling and Selection

The devices in the 3-phase, 2-level DC-AC converter contribute both conduction and switching losses. In [18] the conduction losses are split into those created when current flows through the device's channel and when it flows through its anti-parallel or body diode. The optimisation carried out in this work will focus exclusively on SiC MOSFETs and therefore the conduction losses in the channel and body diode, when the switching dead-time periods are ignored, are respectively given by:

$$P_Q = \left(\frac{1}{8} + \frac{M}{3\pi}\cos\theta\right) R_{ds(on)} \hat{I}_d^{\,2} \tag{1}$$

$$P_D = \left(\frac{1}{8} - \frac{M}{3\pi}\cos\theta\right) R_{D(on)} \hat{I}_d^{\,2} \tag{2}$$

where $\hat{I}_d$ = Peak MOSFET drain current
M = Modulation index
θ = Converter/output current phase angle
$R_{ds(on)}$ = MOSFET channel on resistance
$R_{D(on)}$ = Diode forward-biased resistance

For MOSFETs synchronous conduction is normally used to reduce the conduction loss. This involves the channel conducting instead of the body diode when the current reverses through the MOSFET. In this case $R_{D(on)}$ in equation (2) is replaced by $R_{ds(on)}$. The total conduction loss is then given by:

$$\begin{aligned} P_{cond} &= P_Q + P_D \\ &= \frac{1}{4} R_{ds(on)} \hat{I}_d^{\,2} \end{aligned} \tag{3}$$

The device switching losses are broken down into turn-on, turn-off, reverse-recovery and output capacitor losses. According to [19] the turn-on and turn-off losses are calculated as follows:

$$P_x = f_s \frac{V_{dc}}{V_{CC}} \left(\frac{A_{0(x)}}{2} + \frac{B_{0(x)}}{\pi}\hat{I}_d + \frac{C_{0(x)}}{4}\hat{I}_d^{\,2}\right) \tag{4}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

where f_s = Switching/carrier frequency
V_{CC} = Test voltage of device
$\left.\begin{matrix} A_{0(x)} \\ B_{0(x)} \\ C_{0(x)} \end{matrix}\right\}$ = Device specific constants for x switching losses

The constants $A_{0(x)}$, $B_{0(x)}$ and $C_{0(x)}$ can be taken from a device's datasheet switching energy, drain current relationship. Equation (4) can also be used to calculate the total reverse recovery losses. During the turn-off transition of a device's body diode, the reverse recovery effect will produce losses in both the diode and the complementary device that is simultaneously turning on. The total losses in both the diode and device can be obtained from equation (4) by setting $A_{0(rr)}$ and $C_{0(rr)}$ to zero and then setting $B_{0(rr)}$ to:

$$B_{0(rr)} = \frac{Q_{rr} V_{CC}}{I_{CC}} \tag{5}$$

where Q_{rr} = Reverse recovery charge
I_{CC} = Test current of device

Equation (4) then becomes:

$$P_{rr} = \frac{f_s V_{dc} Q_{rr}}{\pi} \frac{\hat{I}_d}{I_{CC}} \tag{6}$$

The output capacitor of the MOSFET must discharge its stored energy every switching cycle and thus has a switching loss associated with it. This loss can be calculated by using the relationship between the device's output capacitor stored energy (E_{oss}) and its drain to source voltage (V_{DS}) that is given graphically in the datasheet. The information can be approximated by a quadratic and thus results in the following formula:

$$P_{oss} = f_s \frac{V_{dc}}{V_{CC}} \left(A_{oss} {V_{dc}}^2 + B_{oss} V_{dc} \right) \tag{7}$$

where $\left.\begin{matrix} A_{oss} \\ B_{oss} \end{matrix}\right\}$ = Device specific constants for the E_{oss} - V_{DS} relationship

Summing all the various conduction and switching losses will give the total loss for each device, which in turn can be used to determine the predicted efficiency of the converter for each device. This is illustrated in Fig. 2 where the combined conduction and switching losses of various devices from the Cree C2M SiC MOSFET series have been used to calculate the predicted converter efficiency over a range of switching frequencies for the design example specified in Table I. In Fig. 2 the effect on efficiency due exclusively to conduction loss of the devices is given by the values at $f_s = 0$ Hz, while the switching energy loss of each device correlates to the gradient of the curves where the larger the switching energy the steeper the gradient will be. From Fig. 2 it is clear that devices that have the lowest conduction losses also have the highest switching energy loss. This trade-off of different losses

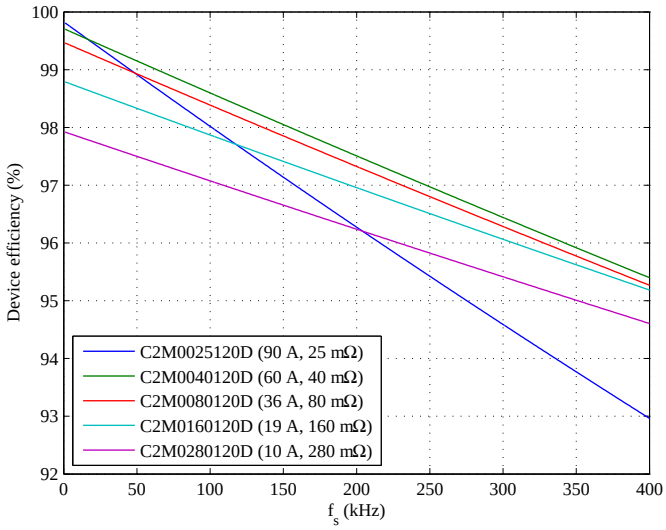


Fig. 2. Converter efficiency as a function of switching frequency when the total conduction and switching losses of various different Cree C2M series MOSFETs are considered

is a natural result of the size of the chip area of the device. As the chip area increases the on resistance ($R_{ds(on)}$) will decrease and hence reduce the conduction losses. However increasing the area will also increase the output capacitance (C_{ds}) which results in larger switching losses. Each device has a different chip area and thus the ratio of conduction to switching losses is different for each device. Thus there are clearly defined switching frequency ranges where a specific device will have the smallest total loss. In practice, device selection is based first and foremost on whether the voltage and current ratings of the device are greater than the voltages and currents it will be subject to in the converter. However for the case were multiple devices meet the voltage and current rating requirements, these switching frequency ranges, based on the device losses, form the device selection criteria used by the optimisation tool. Additionally at this stage of the process the design tool is able to determine which switching frequencies produce designs that meet the minimum efficiency requirement since the power losses are dominated by the device switching losses.

Ultimately this method led the design tool to select the C2M0040120D device since it covers the range of frequencies that are most likely to be used by the optimisation tool in its final design. Despite the C2M0040120D possessing a nominal current rating (60 A) well above the device's RMS current (calculated at approximately 8.8 A), the device was still predicted to have the lowest combined conduction and switching losses. Furthermore, the higher device rating is opportune for a couple of reasons. Firstly, the 60 A current limit is based on an operational temperature of 25 °C, however as the converter is designed to operate at 125 °C, temperature de-rating of the current limit must be taken into account. According to the C2M0040120D datasheet, at 125 °C the current limit will be approximately 30 A. Secondly, 8.8 A is the device's RMS value, however in reality it will be subjected to peak currents higher than this (calculated at 12.5A not

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

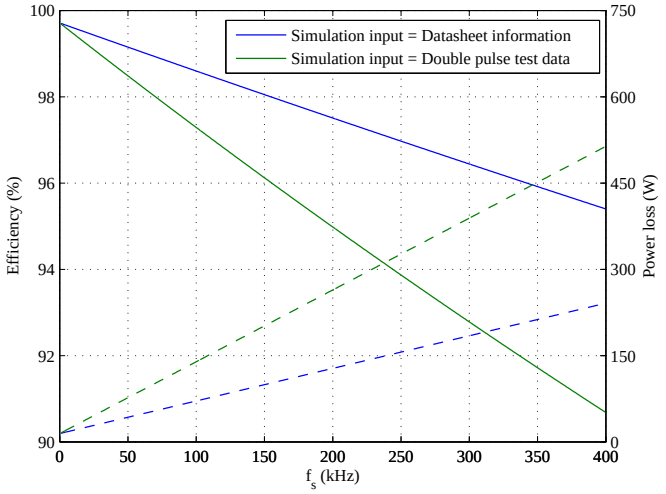


Fig. 3. The total simulated conduction and switching losses (dashed lines) and the predicted efficiency (solid lines) in the 3-phase, 2-level DC/AC converter predicted by the design tool as a function of switching frequency the Cree C2M0040120D SiC MOSFET when the input to the design tool is based on switching energy measurements from the Cree datasheet [20] and when it was obtained via double pulse test experiments in section IV-A

including switching transition spikes). Therefore it is desirable to select a device for which the current rating is high enough to provide an adequate safety margin. Note that practically, as is discussed at length in section IV-A, the switching losses specified in the manufacturers datasheet do not match that found from double pulse test measurements due to a range of external conditions not factored into the manufacturer's datasheet information. Therefore for the remainder of the design example the switching energy data, obtained from experimental measurements performed on C2M0040120D devices, was used to calculate the power losses and converter efficiencies (shown in Fig. 3) which were used in turn for determining the remaining circuit parameters and components. It should be noted that by starting with the experimental data the design tool functions no differently and all the power losses shown above are still calculated in exactly the same way, as all that is being changed is the input data to the design tool.

B. Heatsink Design

The magnitude of the power losses in the devices has a direct effect on the design of the heatsink. The key purpose of the heatsink for the design being considered here, is that it ensures that the junction temperature of each switching device does not exceed its maximum safe operating value. While some of the passive components also benefit from heatsinking, they will not be considered here and the focus will be exclusively on designing for the switching devices.

The heatsink design begins by determining the maximum surface temperature of the heatsink as dictated by the maximum device junction temperature. Assuming that all the devices have approximately the same thermal characteristics, the heatsink surface temperature is given by:

$$T_{hs} = T_j - \Theta_{jc} P_{loss} \tag{8}$$

where Θ_{jc} = Junction to case thermal resistance
P_{loss} = Power loss of a single device

From here the required thermal resistance of the heatsink can be determined as follows:

$$\Theta_{hs,a} = \frac{T_{hs} - T_a}{n P_{loss}} \tag{9}$$

where n = Number of devices used in converter

There are three main approaches to modelling a heatsink; analytical models based on thermodynamic equations and principles, utilising information in heatsink datasheets provided by the manufacturer, and experimentally characterising the heatsink in the laboratory. Analytical models, whilst quite useful for very specific geometries, cannot be readily applied across a broad range of heatsink geometries, as each fin geometry (rectangular, trapezoidal, pin, etc.) will be governed by a different set of design equations. Finite element methods (FEMs), whilst able to evaluate any heatsink to a reasonably high level of accuracy, are not suitable at the initial design stage which the design tool is aimed at. The relatively computationally heavy operation of FEMs comes as a disadvantage at this stage as hundreds of different heatsink geometries need to be evaluated. Furthermore the accuracy of FEMs tend to be negated at this stage as the design is still relying on a number of physical assumptions that prevent FEMs from arriving at the more realistic solutions they are capable of. Given these limitations and the complexity of the analytical methods, it was decided that these methods would not be used for the design optimisation tool.

Using information from the manufacturer datasheet proved to be a much more suitable method. From a design standpoint the thermal resistance of the heatsink is determined mainly by its fin geometry (or cross-sectional shape), extruded fin channel length and, for the case of cooling by natural convection, by the temperature difference between the heatsink surface and the ambient air ($\Delta T = T_{hs} - T_a$). Heatsink manufacturers provide a nominal thermal resistance of each fin geometry (Θ_{nom}) for a specific length (L_{nom}) and temperature difference (ΔT_{nom}), along with graphs that show how Θ_{nom} varies with changing length and/or temperature difference. These graphs can be approximated by fitting them to either an exponential or polynomial curve. The curve fitting constants (A, B, C) that result from these curves of best fit can be used to create scaling factors for the length (S_L) and temperature difference ($S_{\Delta T}$) of the heatsink. These scaling factors specify how much Θ_{nom} needs to be altered if a heatsink length or temperature difference other than the nominal values specified in the datasheet are required by the design. For the proposed design tool the scaling factors were calculated from the following equations:

$$S_L = A_L \left(\frac{L}{L_{nom}} \right)^{B_L} \tag{10}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

$$S_{\Delta T} = A_{\Delta T}\left(\frac{\Delta T}{\Delta T_{nom}}\right)^2 + B_{\Delta T}\left(\frac{\Delta T}{\Delta T_{nom}}\right) + C_{\Delta T} \quad (11)$$

where L = Heatsink extrusion length
L_{nom} = Nominal extrusion length
ΔT_{nom} = Nominal temperature difference
$A_{L/\Delta T}$, $B_{L/\Delta T}$, $C_{L/\Delta T}$ = Curve fitting constants

Using these scaling factors the actual thermal resistance for any combination of length and temperature difference is given by the following equation:

$$\Theta_{sa} = S_L S_{\Delta T} \Theta_{nom} \quad (12)$$

where Θ_{nom} = Nominal thermal resistance

Given that ΔT is already fixed, equations (10) to (12) can be used to determine the required length of the heatsink which in turn can be used to determine the heatsink mass and volume envelope.

Additionally, the heatsink design is also subject to various limiting constraints such as the maximum and minimum extrusion lengths. Manufacturers provide extrusions that are cut to a stock length which a designer may cut down to a shorter length. Longer extrusions can be acquired by making a custom order, however since the optimisation tool presented here focuses on utilising readily available components, the maximum extrusion length will be restricted to the stock length provided by the manufacturer. The minimum extrusion length is constrained by the minimum length required to fit the footprints of all the devices onto the heatsink. If we consider that n devices of the dimensions $L_m \times W_m$ need to fit atop the heatsink then these devices can be arranged in $2N$ ways where N is the number of factors of n including 1 and itself. The factor of 2 is a result of the fact that as long as $L_m \neq W_m$ then the device can be orientated either with its length or width aligned with the front edge of the heatsink. Fig. 4 shows all the possible arrangements, and how it affects the overall footprint length and width, for the case of $n = 4$. The layout arrangement that will be selected by the optimisation tool will by the one that has the shortest overall footprint length (L_{FP}) while also ensuring that the overall footprint width is less than the heatsink width ($W_{FP} < W_{HS}$).

Returning to the design example, Fig. 5 shows the heatsink extrusion lengths and volume envelopes for four different heatsink fin geometries from Aavid Thermalloy [21]. The power losses were calculated for an inverter utilising C2M0040120D devices as in accord with the results shown in Fig. 3. The solid lines display the calculated heatsink length and volume with the minimum and maximum length constraints included, while the dotted lines show the length and volume that could be achieved if there were no length constraints. The minimum length constraints produce the horizontal portions of the curves that occur at the lowest frequencies in Fig. 5. They show that below a certain switching frequency the minimum length, and subsequently the minimum volume, has been reached and no shorter lengths can be achieved at lower frequencies. The maximum length constraints produce the vertical portions of the curves in Fig. 5. In this case as soon as the switching frequency increases to a value where it produces the maximum length of a particular extrusion (such as 150 mm for the 0K267), all switching frequencies greater than this value will set the length to infinity (or a suitably high value) thus creating the vertical portions of the curve. This ensures that the design tool will not be able to select that particular extrusion at these higher switching frequencies. Focusing on the 0K267 heatsink in Fig. 5, despite it being the longest in length, its compact profile produces the smallest volume envelope. However, given that its maximum length is only 150 mm it is limited to switching frequencies below 52 kHz, after which 000EK* becomes the best option.

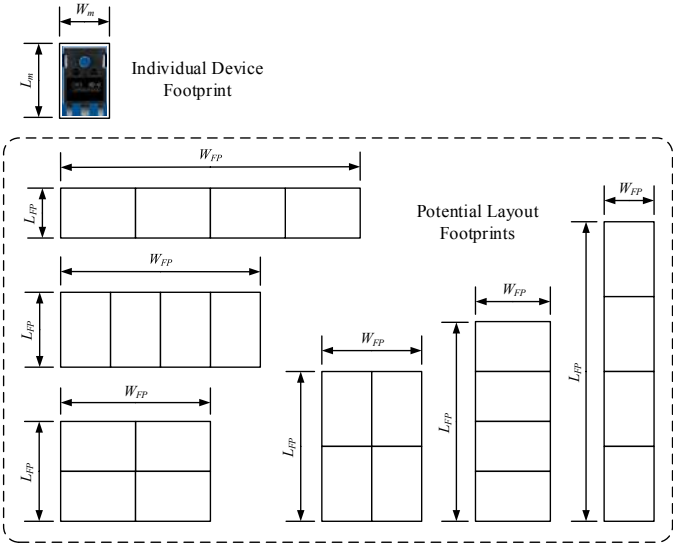


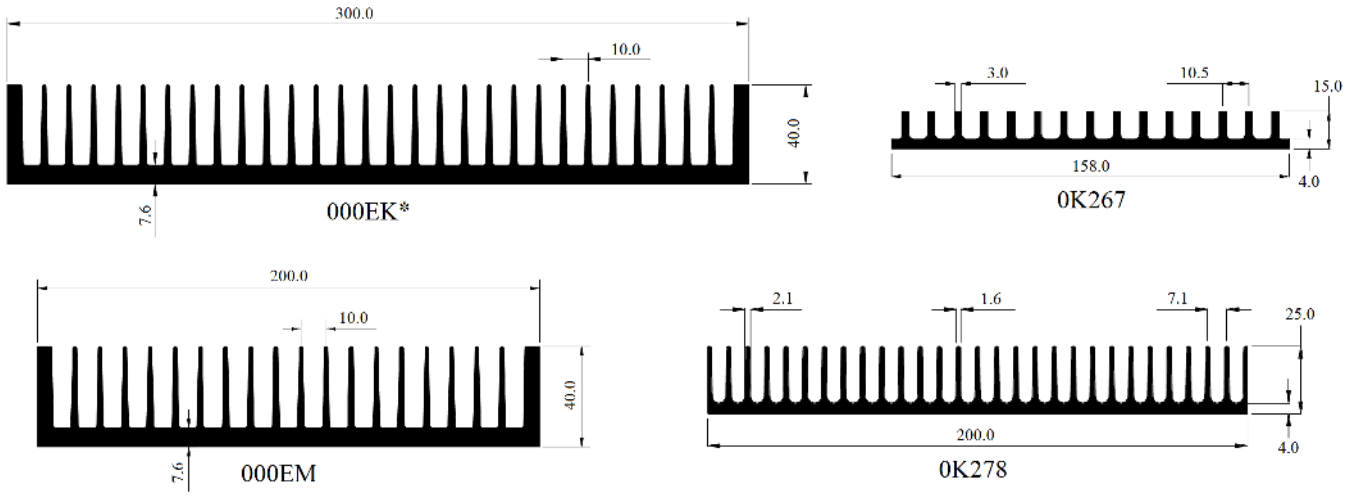
Fig. 4. Device footprint layouts, and their corresponding dimensions, for 4 devices

Finally it should be noted that while the datasheet based method is useful for the initial design stage, just like for the analytical methods, it is limited in its accuracy due to it lacking particular pieces of realistic information. As a result the design had to be supplemented with an experimental characterisation which will be discussed in section IV-B.

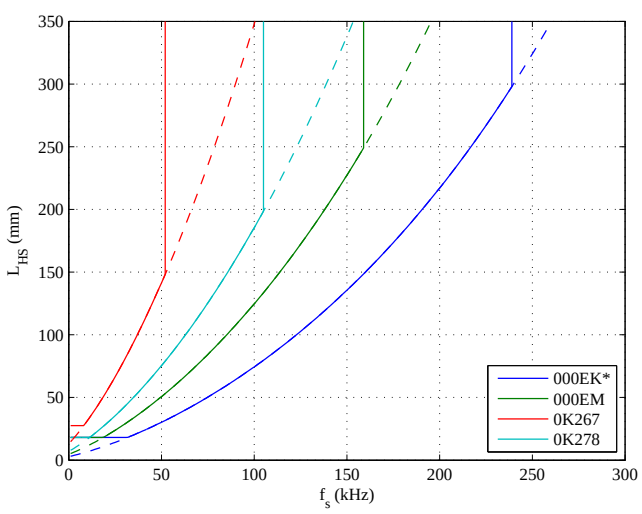
C. Passive Components Design

The passive components that the converter is comprised of include a DC link capacitor at the input, and a line and EMI filter at the output. The purpose of the DC link filter is to limit the input voltage ripple of the converter while the line filter is used to limit the output current ripple. The purpose of the EMI filter is to limit the amount of both the conducted differential mode (DM) and common mode (CM) noise of the converter. Similar to the heatsink design, the optimisation tool

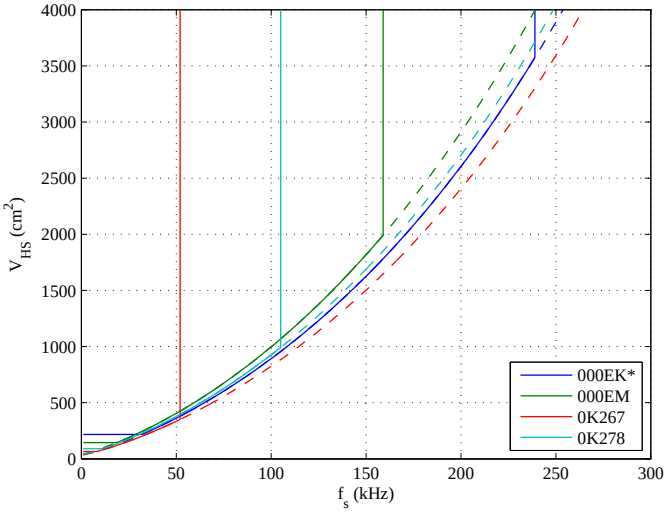
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics



(a)



(b)



(c)

Fig. 5. Examples of heatsink fin geometries analysed by the optimisation tool: (a) Extrusion cross-section dimensions, (b) Minimum required extrusion length and (c) Minimum volume envelope. Figures (b) and (c) are created assuming C2M0040120D devices have been selected. Dotted lines indicate the length if no maximum or minimum limits are applied to the extrusion length

assesses a range of switching frequencies to determine which combination of components and switching frequency produces the design with the smallest total volume.

When selecting the DC-link capacitor, two main objectives must be taken into consideration. Firstly the capacitance must be large enough to meet the voltage ripple requirement of the inverter. Secondly, the capacitor must be able to sustain the ripple current that the circuit will subject it to otherwise it may overheat and exceed its temperature rating. Appropriate capacitor types for the DC-link filter include aluminium electrolytic capacitors and metallised polypropylene film capacitors. Electrolytic capacitors exhibit high capacitance per unit volume but possess a relatively high equivalent series resistance (ESR) and thus are limited by the ripple current requirements. Metallised polypropylene film capacitors exhibit low ESR and low capacitance per unit volume and thus are limited by the voltage ripple requirement [22]. As a result the proposed design tool implements different capacitor sizing methods depending on which type of capacitor and thus which major ripple limitation needs to be considered.

In order to correctly size an electrolytic capacitor so that it adheres to the ripple current requirement, one must first calculate the RMS value of the current flowing through the capacitor. This is done according to the following equation [23]:

$$I_{C(rms)} = I_{rms}\sqrt{2M\left(\frac{\sqrt{3}}{4\pi} + \cos^2\theta\left(\frac{\sqrt{3}}{\pi} - \frac{9}{16}M\right)\right)} \tag{13}$$

where I_{rms} = RMS output phase current

As $I_{C(rms)}$ is fundamentally an AC current it can be compared with the ripple current ratings (I_{rip}) given in the electrolytic datasheets. As ripple currents are typically defined for an operational frequency of 120 Hz, an appropriate ripple

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

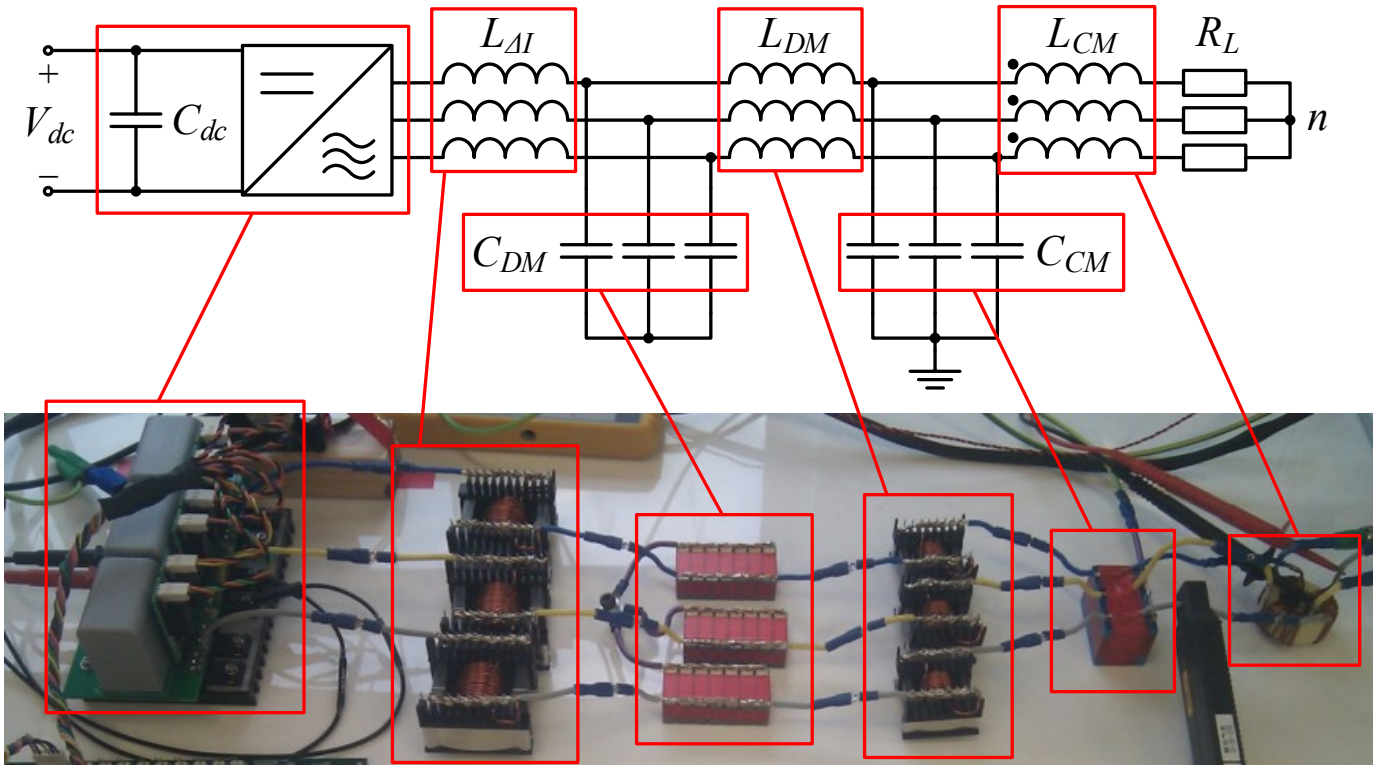


Fig. 6. Experimental setup of filter components of the 2-level, 3-phase DC/AC converter

current multiplier must be selected from the datasheet to ensure that the ripple current rating is scaled for use with the kHz frequency range that the design tool will operate within. With this information the design tool can select a capacitor (or capacitor combination) that has a higher ripple current rating then the capacitor current i.e. $I_{rip} > I_{C(rms)}$.

For a metallised polypropylene film capacitor whose design is based primarily on the voltage ripple requirement (ΔV), its capacitance, which will be the main dictator of its physical size, can be approximately calculated according to the following equation [24]:

$$C_{dc} = \frac{MI_{rms}}{16\Delta V f_s}\sqrt{\left(6 - \frac{96\sqrt{3}}{5\pi}M + \tfrac{9}{2}M^2\right)\cos^2\theta + \frac{8\sqrt{3}}{5\pi}M} \tag{14}$$

At the output of each phase is an LC network that combines to form the line and EMI filters. The filter consists of three main stages, as shown in Fig. 6, which is representative for grid-tie and inverter applications (other filter types can also be considered). The first stage is the line filter which consists of a single inductor on each phase ($L_{\Delta I}$). The second is the DM filter which consists of capacitors (C_{DM}) and additional inductors (L_{DM}) that when combined with $L_{\Delta I}$ creates an LCL network that forms the full DM filter. The final stage is the CM filter which consists of capacitors (C_{CM}) and a 3-phase CM choke (L_{CM}) that when combined with $L_{\Delta I}$ creates an LCL network that forms the full CM filter. The optimisation tool designs each of these stages in turn, beginning with the line filter and adding on the DM and CM filters afterwards.

The size of the line filter's inductance is determined by the design constraint governing the maximum allowable ripple current. This results in a single inductance value for each possible switching frequency. The relationship between the maximum ripple current and line inductance (for low to mid-range switching frequencies) is approximated by the following equation [25]:

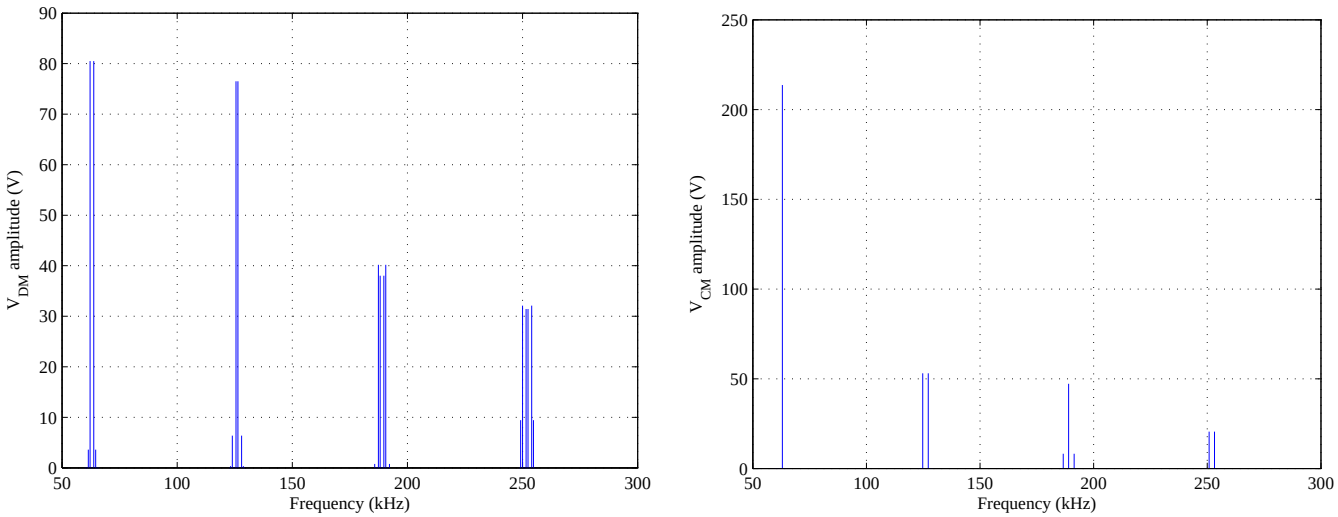
$$\Delta I = \frac{V_{dc}MT_s}{4\sqrt{3}L_{\Delta I}} \tag{15}$$

where T_s = Switching/carrier period

Both the DM and CM components of the EMI filter are designed so that they conform to the L, M and H categories of the DO-160E standard [26]. In order to achieve this, the DM and CM harmonics are calculated for the frequencies specified by the standard. If it is assumed that naturally sampled, sine-triangle modulation is used to control the converter, then according to [27] the major harmonics occur at frequencies of $f_{(m,n)} = mf_s + nf_0$, where m and n are integer values. These major harmonics can be decomposed into their DM and CM voltage components by using equations (16a) and (16b) [28]. Example results for these equations are shown in Fig. 7 which displays the DM and CM voltage harmonics for the case where the switching frequency is 63 kHz and all other parameters are as given in Table I.

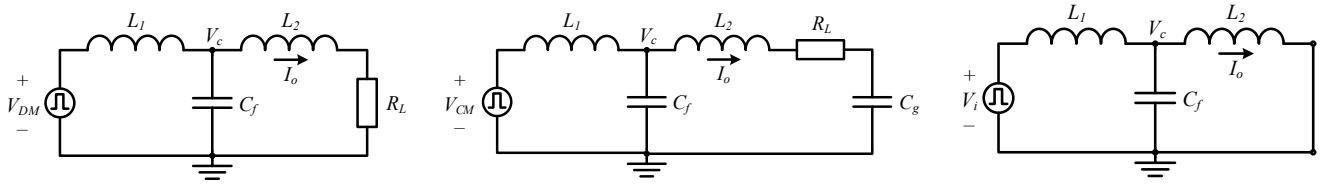
$$\left|V_{DM(m,n)}\right| = \left|\frac{4V_{dc}}{\sqrt{3}\pi}X_{(m,n)}\sin\left(n\frac{\pi}{3}\right)\right| \tag{16a}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics



(a) (b)

Fig. 7. Frequency spectra of the (a) DM voltage harmonics and (b) CM voltage harmonics for $f_s = 63$ kHz, $f_0 = 400$ Hz, $V_{dc} = 600$ V and $M = 0.9$



(a) (b) (c)

Fig. 8. Single-phase LCL filter models for the (a) DM EMI filter, (b) CM EMI filter and (c) DM and CM filter with a short-circuit load

$$\left|V_{CM(m,n)}\right| = \left|\frac{2V_{dc}}{3\pi} X_{(m,n)} \left(1 + 2\cos\left(n\frac{2\pi}{3}\right)\right)\right| \quad (16b)$$

$$\text{where} \quad X_{(m,n)} = \frac{1}{m} J_n\left(m\frac{\pi}{2}M\right) \sin\left((m+n)\frac{\pi}{2}\right)$$

In order to adhere to the design's specifications, the optimisation tool needs to ensure that the load current harmonics of each phase are below the limit specified by the DO-160E standard (I_{lim}). As mentioned above, the DM and CM filters were modelled as LCL filters each connected to an appropriate load. For the DM filter this is just a resistance (R_L) whereas for the CM filter it was a resistance plus a parasitic capacitance to ground (C_g) as shown in Fig. 8a and 8b respectively. Typically in either case the impedance of the filter inductors will be much higher than the load resistance (i.e. $\omega L > R_L$), and thus the load can be treated as a short circuit ($R_L = 0$). This assumption is beneficial during the design process as it corresponds to the worst case scenario when the load current is at its maximum. With this in mind it is therefore useful to replace C_g with a short-circuit, in the case of the CM filter, to ensure that the worst case scenario is designed for. Therefore both the DM and CM models simplify to that shown in Fig. 8c and the resulting LCL filter will produce the following transfer function:

$$\frac{V_i\left(j\omega_{(m,n)}\right)}{I_o\left(j\omega_{(m,n)}\right)} = j\omega_{(m,n)}\left(L_1 + L_2 - {\omega_{(m,n)}}^2 L_1 L_2 C_f\right) \quad (17)$$

From (17) it can be seen that the angular resonant frequency of an LCL filter is given by $\omega_{res} = \sqrt{\frac{L_1+L_2}{L_1 L_2 C_f}}$. Substituting this into (17) produces:

$$\left|\frac{V_i\left(j\omega_{(m,n)}\right)}{I_o\left(j\omega_{(m,n)}\right)}\right| = \omega_{(m,n)}\left(L_1 + L_2\right)\frac{\left|{\omega_{(m,n)}}^2 - {\omega_{res}}^2\right|}{{\omega_{res}}^2} \quad (18)$$

Equation (18) shows that the filter attenuation at a particular frequency is dependent on the total filter inductance ($L_1 + L_2$) and the resonant frequency. The optimisation tool specifies that L_1 be the line inductance, as calculated from (15). Basing the value of L_1 on the ripple current requirement may result in a slightly larger filter volume than if L_1 was optimised simultaneously with L_2 and C_f, however doing so doesn't have a detrimental affect on the overall power density, since the EMI requirements are typically much stricter than the current ripple requirements of an application. For example if the current ripple is allowed to be larger than 10% (as is the case in this design example), then the size of the line inductor would decrease. However, the size of all the EMI filter components would need to increase in order to meet the EMI requirements and thus the overall volume would not be significantly reduced. Furthermore, basing L_1 on only ripple current greatly improves the computation time of the design tool as it only has to simultaneously search through two component databases (L_2 and C_f) rather than three, and

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

thus was considered to be the better design methodology for the optimisation tool.

Next the design tool specifies a range of inductances that L_2 is allowed to take. For each potential value of L_2 the optimisation tool calculates the resonant frequency of the filter, that will be required to achieve the desired attenuation, according to the following equation:

$$\omega_{res} = \omega_{(m,n)} \sqrt{\frac{\omega_{(m,n)} (L_1 + L_2) \left| I_{o(m,n)} \right|}{\omega_{(m,n)} (L_1 + L_2) \left| I_{o(m,n)} \right| + \left| V_{i(m,n)} \right|}} \tag{19}$$

From here the range of values of L_2 and its corresponding range of resonant frequencies are translated into a range of values for the capacitance C_f. This completes a range of inductance-capacitance ($L - C$) pairs that will comprise the DM and CM parts of the EMI filter. For the DM section of the filter, the optimisation tool substitutes the following values into equation (19): $V_i = V_{DM}$, $I_o = I_{lim}$, $L_1 = L_{\Delta I}$, $L_2 = L_{DM}$, $C_f = C_{DM}$. For the CM section it substitutes the following: $V_i = V_{CM}$, $I_o = I_{lim}$, $L_1 = \frac{1}{3} L_{\Delta I}$, $L_2 = L_{CM}$, $C_f = C_{CM}$.

At this point in the optimisation process, each and every switching frequency will yield a single L or C value for the line inductor and DC-link capacitor, and a range of $L - C$ pairs for the DM and CM portions of the EMI filter. For the next stage of the optimisation process, the tool will convert all the L and C values into real physical parts by designing and selecting each component from a suitable subset of parts. The line and DM inductors are constructed from gapped ferrite cores where the optimisation tool determines the core size, gap length, winding diameter and number of turns. The diameter of the windings are selected based on the desired current density of the wire (J_{rms}). The core selection was based on the area-product method outlined in [29] which states that the core size must satisfy the following inequality:

$$A_w A_{core} > \frac{L \hat{I} I_{rms}}{K_u J_{rms} \hat{B}} \tag{20}$$

where A_w = Winding window area
A_{core} = Core area
$\hat{I}$ = Peak inductor current
I_{rms} = RMS inductor current
K_u = Window utilisation factor
$\hat{B}$ = Maximum allowable flux density

Once the core has been selected the number of turns and the gap length are calculated according to the following:

$$n = \frac{L \hat{I}}{\hat{B} A_{core}} \tag{21}$$

$$l_g = \frac{\mu n^2 A_{core}}{L} \tag{22}$$

where μ = Core permeability

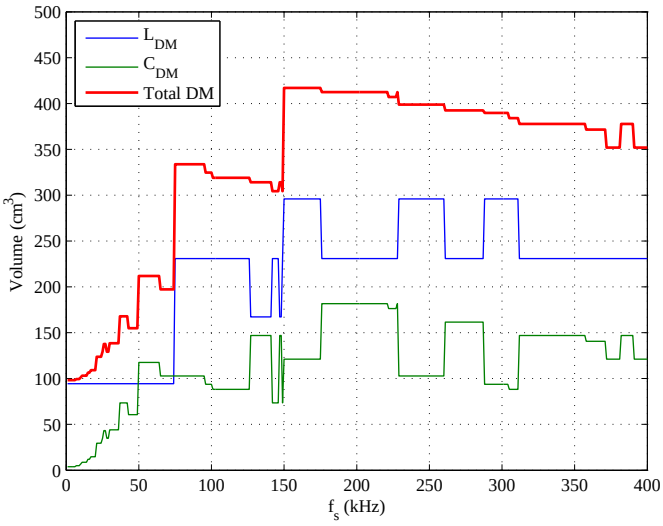


Fig. 9. Optimised volume of the differential mode (DM) filter components (excluding the line inductor) as a function of switching frequency

The optimisation tool constructs the CM inductor from a toroidal coil. The winding diameter is, once more, set by the desired current density. Once selected, the winding diameter is used to determine the maximum number of turns, and hence the maximum inductance, that each specific core in the component database is capable of producing. The EMI filter is completed by the optimisation tool selecting film suppression capacitors for C_{DM} and C_{CM}. For safety reasons class X1 capacitors were used in the DM filter while class Y2 were used in the CM one. The selection process involves the optimisation tool assessing each capacitor in the component database by determining the number that would need to be paralleled to meet the capacitance requirement and then selecting that which has the lowest overall volume. The DC link capacitor is selected via the same method however it is selected from a database of film and/or electrolytic capacitors suitable for DC filtering.

Now that all the L and C values have been turned into real physical components, the optimisation tool is able to select the $L - C$ pair that produces the smallest volume at each switching frequency for both the DM and CM portions of the EMI filter. The volumes of the DM EMI filter components for the design example are shown in Fig. 9. The step changes present on the result curves indicates that the optimisation tool has changed from one component choice to another in order to minimise the overall volume. Examining the total volume of the DM filter section shows that as the switching frequency increases, there are step increases in the volume at frequencies of 150 kHz and its factors (i.e. 75, 50, 37.5, 30, etc.). This is because the limit defined by the DO-160E EMI standard applies only to harmonics above 150kHz. Therefore any switching frequency that is a factor of the 150 kHz will produce harmonics that fall just within the standard's limits whereas a slightly lower switching frequency will produce harmonics that fall just outside it. A similar effect is observed for the CM filter optimisation.

Shown in Fig. 10 are the volumes of all the passive

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

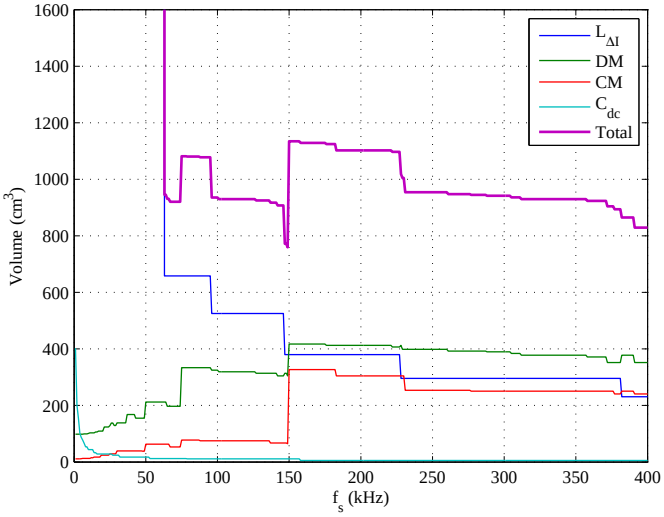


Fig. 10. Optimised total volume of the all the passive components as a function of switching frequency. Note that "DM" refers to the combined volume of L_{DM} and C_{DM}, and "CM" refers to the combined volume of L_{CM} and C_{CM}

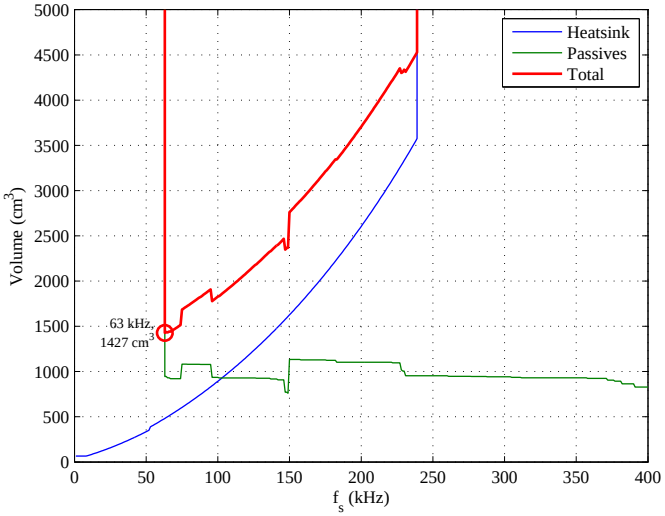


Fig. 11. Optimised total converter volume (i.e combined heatsink and passive components volume) as a function of the switching frequency with a marker indictating the absolute minimum volume and the optimal frequency at which it occurs

components and their combined overall volume as a function of the switching frequency. The DM and CM filter volumes follow the patterns described above. Since only a finite number of components can be selected from the database, not every intermediate volume value can be obtained and thus the results plot as a step-based discrete function. This is most clearly seen with the volume of the line inductor where each step on the curve represents a distinct inductor core and bobbin. If every intermediate inductor volume could be achieved then the volume curve would be approximately inversely proportional to the switching frequency. However, since there are a finite number of cores and bobbins, optimising over a range of switching frequencies results in volume steps that follow this trend but don't match it exactly. For example the step starting at 63 kHz and finishing at 95 kHz represents the ETD59/31/22 core and bobbin where the number of turns decreases as the frequency increases. At 63 kHz the number of turns completely fills the winding window however this will not change the overall volume envelope as the windings will all be contained within the space defined by the bobbin. Therefore if the switching frequency was to be made lower than 63 kHz then a larger core would be required. Since the ETD59 core was the largest one in the database, the design tool sets the volume to virtual infinity for all switching frequencies below 63 kHz so to indicate that no core will meet the design specifications at these frequencies. At 96 kHz the design tool is able to identity a smaller core and bobbin, that when its winding window is completely filled, produces the required amount of inductance. Thus the design tool selects this smaller volume core for all further switching frequencies until the process repeats and an even smaller core can achieve the required inductance.

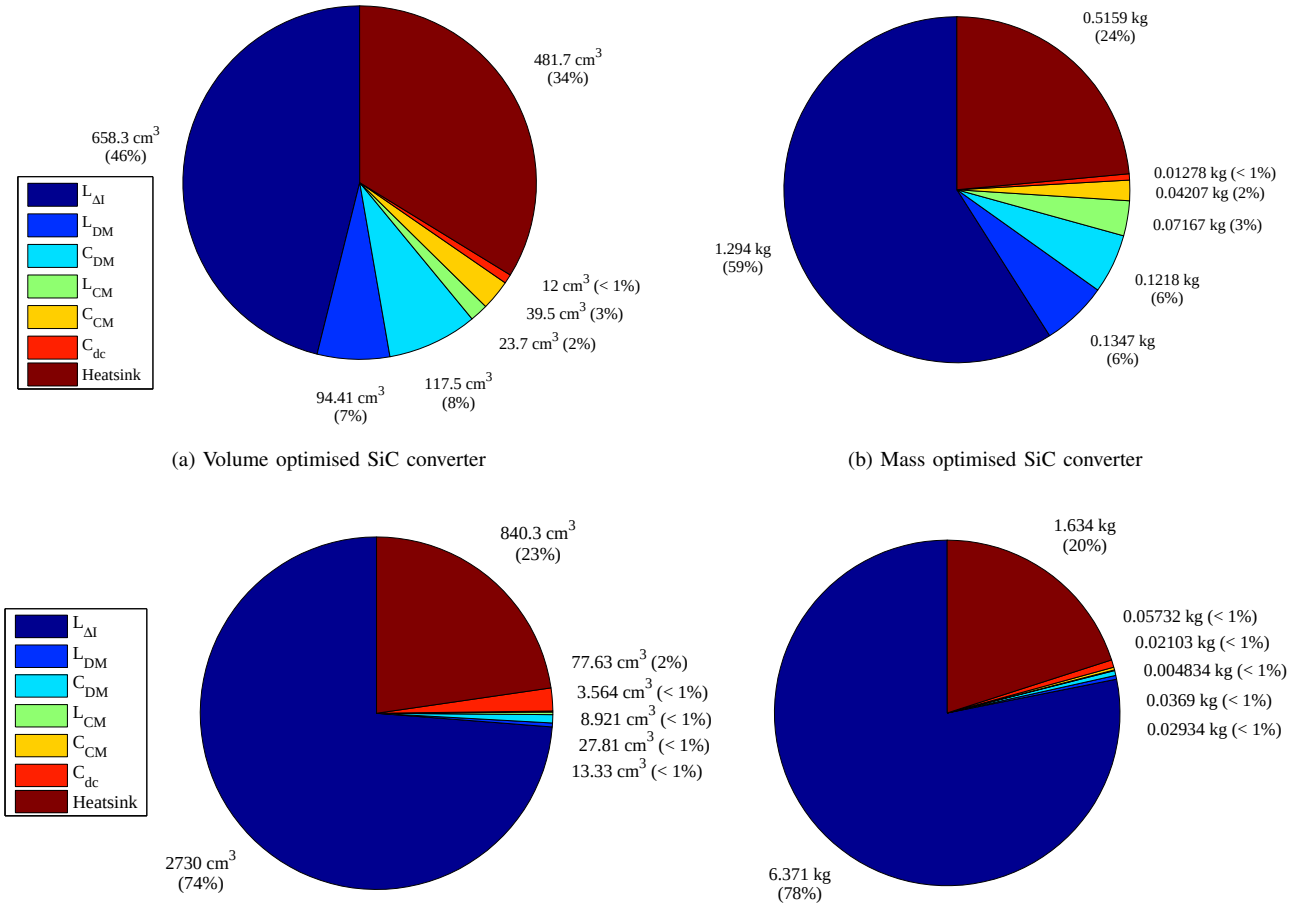
D. Overall Converter Results

To finish the design process the optimisation tool calculates the total converter volume by adding the heatsink and passive component volumes at each potential switching frequency, as is shown for the design example in Fig. 11. It can be seen that as the switching frequency increases the heatsink volume increases while the volume of the passive components tends to decreases, however in this case the rate of increase of the heatsink is much greater than any decrease in the passives. With this final piece of information the optimisation tool is able select the converter design that produces the smallest total volume, which for the design example is 1427.19 cm^3 produced at a switching frequency of 63 kHz. The full component details of the optimal design for this example are given in Table II while a breakdown of the contribution of each component to the total converter volume is shown in Fig. 12a. For the sake of comparison, the optimisation tool was used to design a converter with the same specifications except this time it was to use Si IGBT devices. The design produced by the tool is also shown in Table II, side by side with the SiC MOSFET design, and a volume breakdown of the converter is shown in Fig. 12c. As can be seen the switching frequency is reduced to 6 kHz leading to a significant increase in the volume of the passive components, especially the line inductor. The end result is that the power density of the SiC MOSFET design is 159.4% higher than the Si IGBT one. It should also be noted that the efficiency of the Si IGBT design is only 96% as no components in the database could be combined to achieve the desired 98% efficiency and thus a compromise had to be made so that a valid design could be presented.

III. Optimisation Algorithm Implementation

A simplified operational flow diagram of the optimisation tool is shown in Fig. 13. The process begins by the user defining the specifications (e.g. output voltage, power rating), constraints (e.g. minimum converter efficiency, maximum component temperatures) and objectives (e.g. minimise the volume). The algorithm then combines all the suitable items in the component databases with all the potential converter

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics



(a) Volume optimised SiC converter

(b) Mass optimised SiC converter

(c) Volume optimised Si converter

(d) Mass optimised Si converter

Fig. 12. Contribution of each component in a SiC MOSFET or Si IGBT based converter that has been optimised for either volume or mass

operating conditions (e.g. the range of allowable switching frequencies) to create every possible design within the solution space. Each design is checked to see if it satisfies the constraints and, if successful, will have its objective value calculated, referred to as the design's cost (e.g. the design's total volume or mass). If the calculated cost of the current design is less than the cost of all the other designs that have been examined thus far, then the optimisation algorithm will store the current design as the best design and all the remaining designs will be compared against it until a design with an even lower cost is found. Upon completion the algorithm will have iterated through all the possible designs and selected the one that has the lowest cost as the optimal design. This method is effective in finding the optimal design however it is very inefficient as it must check through every possible design in the solution space in order to do so.

The reason that the method described above is inefficient is because it is effectively a nested loop structure where each level of the structure is occupied by a single design variable set. An example of this structure for 4 design variable sets is shown in Fig. 14a. In this case the total number of designs that will need assessing is equal to $N_a \times N_b \times N_c \times N_d$. It can be seen that as the number of design variables increases, the number of designs grows exponentially. In order to reduce the number of designs, and hence improve the computational efficiency, the algorithm has been structured so that it exploits the interdependency relationships of the design variables. This method identifies whether or not one variable is directly dependent on another variable or if they are indirectly connected through a chain of variables. Identifying variables by this manner results in a structure where dependent variables branch off from each other. The variables that has the most dependent variables branching from it forms the underlying outer loop of the design tool algorithm while the other variables form the various nested loop levels. The overall effect is that the number of nested loop levels is reduced. An example of this is given in Fig. 14b where the same 4 design variables shown in Fig. 14a have been reused. In this case variable B branches from variable A while variables C and D branch from A rather than B as was the case in Fig. 14a. Therefore the total number of designs is now given by $N_a\left(N_b + N_c N_d\right)$.

This type of branching structure shown in Fig. 14b was applied to the design optimisation tool by examining its operational structure shown in Fig. 1. The structure links the various design specifications, constraints and objectives feed into the tool by the user, to the various component models and selection procedures controlled by the tool's algorithm. At the highest level the optimisation tool makes selections

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

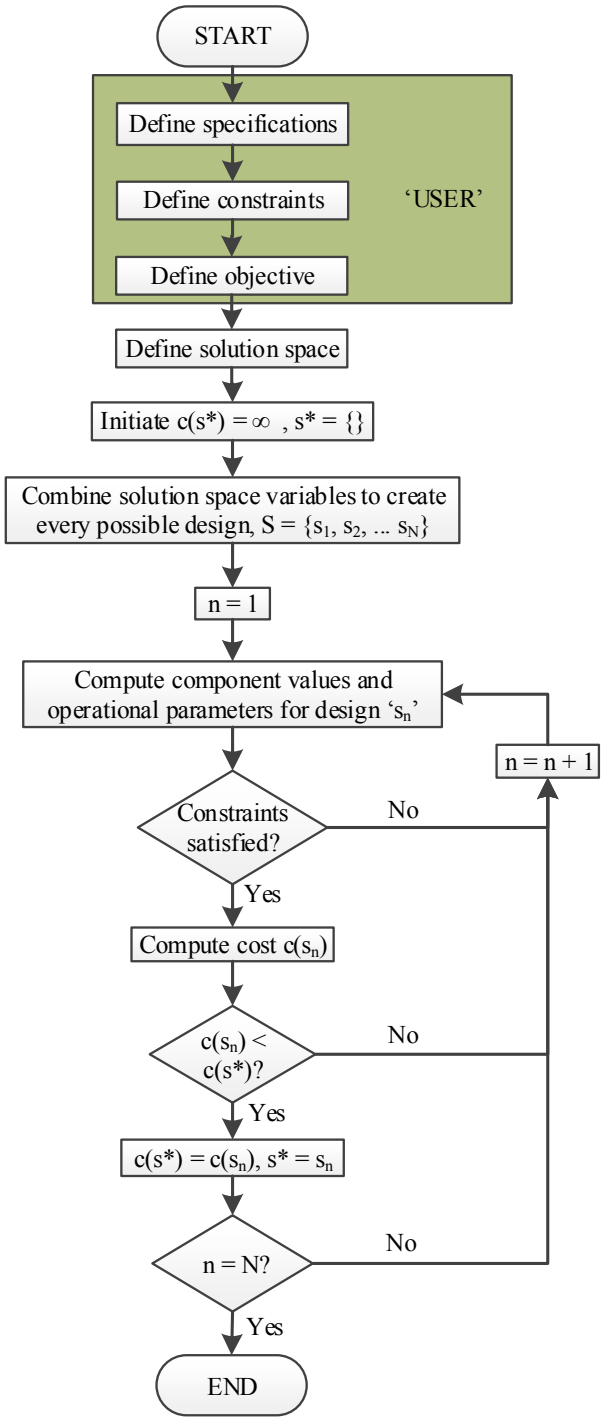


Fig. 13. Operational flow diagram of the optimisation tool [30]

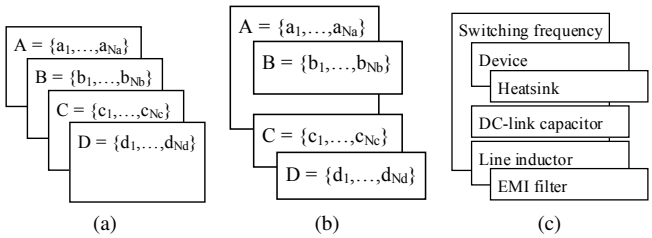


Fig. 14. Design variable arrangement structures; (a) Nested loop structure, (b) Branching variable structure, (c) 3-phase DC/AC inverter design tool structure

TABLE II
DESIGN EXAMPLE OPTIMISED COMPONENT DETAILS

Design parameter	SiC MOSFET	Si IGBT
Volume	1427.19 cm^3	3701.96 cm^3
Switching frequency	63 kHz	6 kHz
Device	C2M0040120D	FGW15N120VD
Heatsink	000EK*	000EK*
• Length	40.15 mm	70.03 mm
$L_{\Delta I}$	964.7 μH	10.417 mH
• Core	ETD59/31/22	E100/60/28
• # turns	71	375
• Gap length	2.4 mm	12.5 mm
• Wire size	1.8 mm	1.8 mm
L_{DM}	50 μH	5 μH
• Core	ETD29/16/10	E19/8/5
• # turns	18	6
• Gap length	0.6 mm	0.2 mm
• Wire size	1.8 mm	1.8 mm
C_{DM}	1.76 μF	0.33 μF
• Type	474R32201A12	BFC23381X334
• # in parallel	8	1
L_{CM}	646.38 μH	188.19 μH
• Core	TX36/23/15-3E5	R25.3/14.8/10-T37
• # turns	9	6
• Wire size	1.8 mm	1.8 mm
C_{CM}	0.44 μF	0.015 μF
• Type	B32024A3224M	B32022A3153M
• # in parallel	2	1
C_{dc}	3 μF	30 μF
• Type	MKP1848530094K2	C4AEOBW5300A3MJ
• # in parallel	1	1

in regards to the operating conditions of converter such as the switching frequency, which is then passed down into the component models in order to design and select all the various components such as the switching devices, the heatsink and the passive components. The selected components are then passed back up the structure to be measured against the specifications, constraints and objectives and help inform the tool's decision as to what the optimal operating conditions should be. From Fig. 1 it can be seen that the devices and heatsink selection form one branch off of the operating conditions and switching frequency, while the passive component selection procedures form a separate branch. Therefore these sections of the algorithm can make use of the branching variable structure in the way shown in Fig. 14c where the switching frequency forms the outer loop of the algorithm from which the other variables branch off from.

For the design example discussed in section II the component database and circuit parameters that the tool was able to select and form potential designs from is given in Table III. Without restructuring, the algorithm is required to assess approximately 2.2×10^{12} designs. By comparison, using the independent variable separated structure illustrated in Fig. 14b, the number of designs is reduced to 224,822 which is a reduction of over 99.9%.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

TABLE III
DESIGN EXAMPLE COMPONENT DATABASE AND CIRCUIT PARAMETERS

Design parameter	Values
Device type	Cree C2M MOSFETs (5 in total)
Switching frequency	10, 11, , 400 kHz
Line and DM inductor core type	Ferroxcube gapped double ETD cores (7 in total)
CM inductor core type	TDK/EPCOS & Ferroxcube toroids (44 in total)
DM capacitor type	Kemet & Vishay X1 class film (21 in total)
CM capacitor type	Kemet, TDK & Vishay Y2 class film (68 in total)
DC link capacitor type	AVX, Kemet & Vishay DC film (36 in total)
Heatsink types	Aavid thermalloy (14 in total)

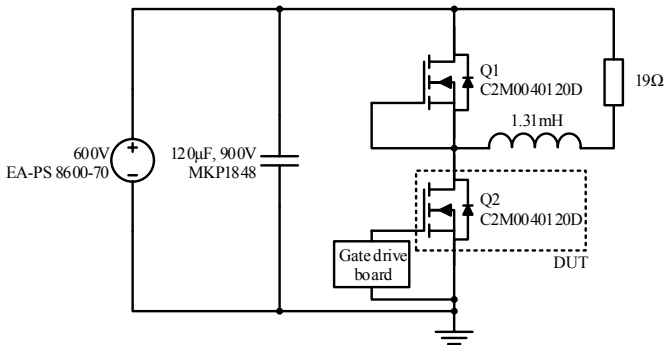


Fig. 15. Schematic of the double pulse test setup

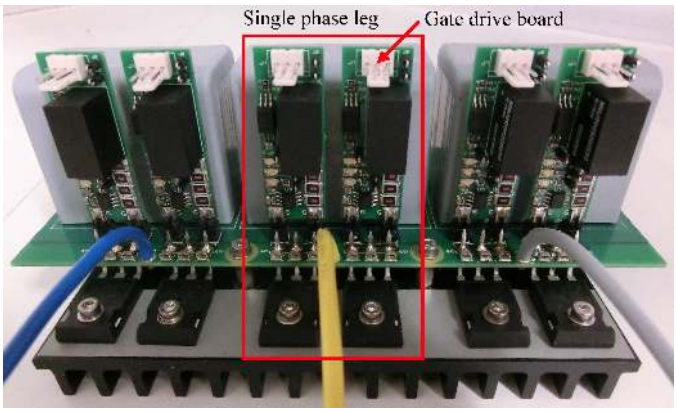


Fig. 16. Power board, devices and gate drivers of a 3-phase, 2-level DC-AC converter created by the design optimisation tool. A single phase leg was used for double pulse test measurements

IV. DESIGN OPTIMISATION TOOL EXPERIMENTAL VERIFICATION

In order to fully assess the design optimisation tool, it is necessary to first determine whether or not the component data used by the tool matches that of an actual experimental converter. This section first focuses on the two areas where the greatest discrepancy between component manufacturer data and actual converter measurements usually occur; device switching losses and heatsink thermal resistance. It then investigates the performance of a converter built according to the results of the design example given in Table II. Through experiments carried out on the converter, the device loss model and the output filter design model of the optimisation tool are evaluated.

A. Device Switching Loss Measurement

The switching energy loss of a converter is affected by not only the inherent switching energy of the device itself, but also by the surrounding circuitry in which the device is placed. The switching energy (E_{on}, E_{off}) specified in a manufacturer's datasheet is based on a clamped inductive switching test that inserts the device under test (DUT) into an evaluation board. The board itself consists of a single phase leg where the DUT is usually paired with a Schottky diode since a Schottky has low switching losses and no reverse recovery. External components such as gate drive circuits and load inductances are added externally so that various different operating conditions can be tested. Consequently, the switching energy results produced are specific to component values, board layout and the operating conditions used.

The uniqueness of the manufacturer's results becomes problematic when trying to apply them to a converter design for several reasons. Firstly the components used in the actual 3-phase converter will be different and thus change the switching dynamics of the system. The phase leg typically consists of two SiC MOSFETs placed in both the upper and lower positions, one of which is the DUT, as the current in the phase leg must be bi-directional and thus changes the switching waveforms that the DUT is subject to. The gate drive circuitry will also be different to that used in the manufacturer's setup in order to meet the speed, power and stability requirements of the actual converter. As a result the gate drive produces signals that might transition faster or slower, or even be shaped differently altogether to the signals that produced the manufacturer's results. Secondly, the PCB layout of the actual converter will be different to the manufacturer's setup and hence will be subject to different parasitic components that will change the shape of the turn-on and turn-off transitions. This is of particular importance for SiC devices since small changes in the layout can have significant effects on the switching energy requirement of the devices, much more so than is the case for Si devices.

For these reasons, double pulse tests (DPTs) were carried out on the converter created by the optimisation design tool, to determine the real switching losses of the chosen SiC devices. A simplified schematic of the double pulse setup is shown in Fig. 15 along with the various component values used in the double pulse test. Fig. 16 shows the converter's power board containing the 3 phase legs with their upper and lower devices, of which a single phase leg was used for the DPTs. Fig. 17 shows the turn-on and turn-off transitions captured during the DPTs for load currents of 10 A, 25 A and 40 A where the gate resistance used was 24Ω. The current overshoot present on all the turn-on transitions (Fig. 17a, 17b and 17c) is produced in part by the high dv/dt experienced by the output capacitance of the devices and in part by the reverse recovery effect of the complementary device's body diode. The turn on

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

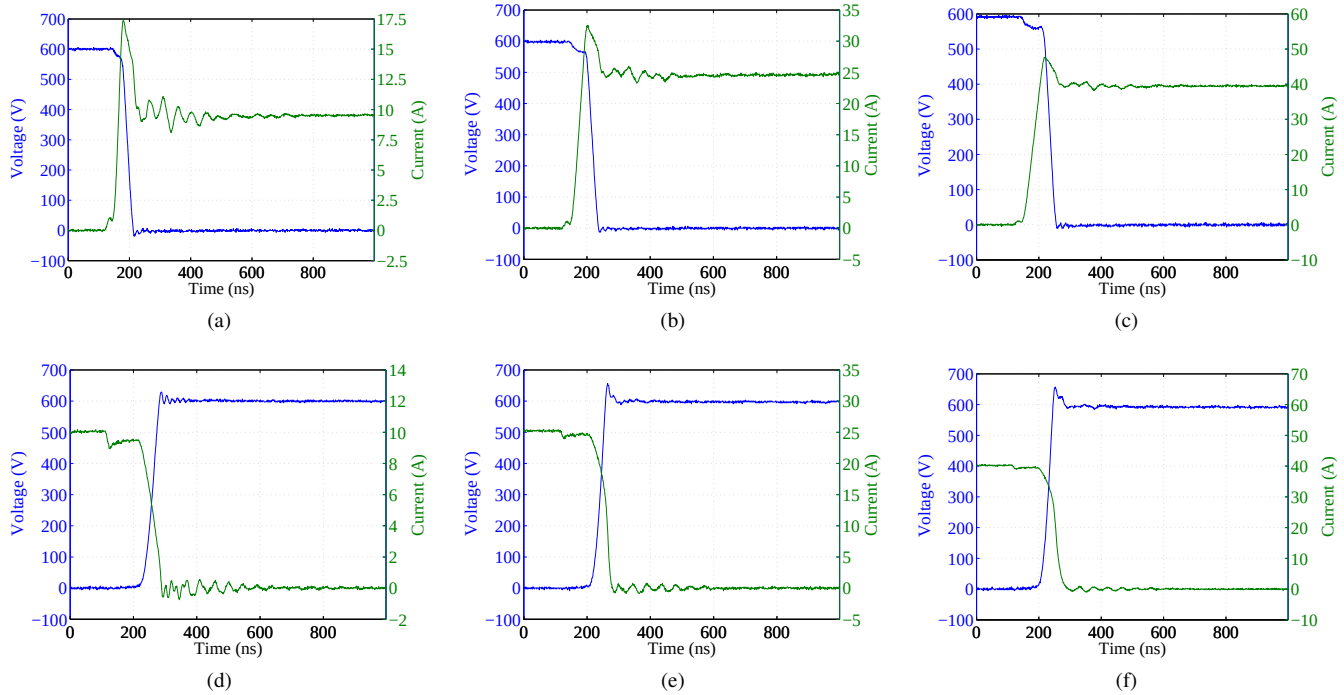


Fig. 17. Turn on switching transitions for load currents of (a) 10 A, (b) 25 A, (c) 40 A, and turn off switching transitions for load currents of (d) 10 A, (e) 25 A, (f) 40 A produced by double pulse tests. The gate resistance for all the transitions was 24Ω

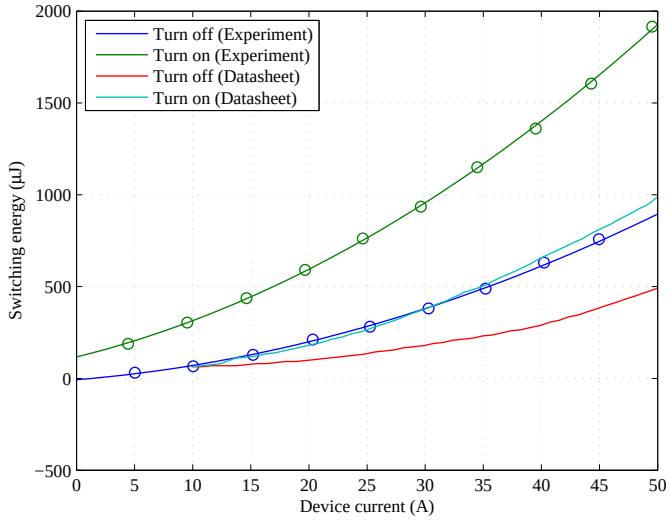


Fig. 18. Turn on and turn off switching energy as a function of the device current for Cree's C2M0040120D MOSFET obtained from the DPT and from Cree's official datasheet

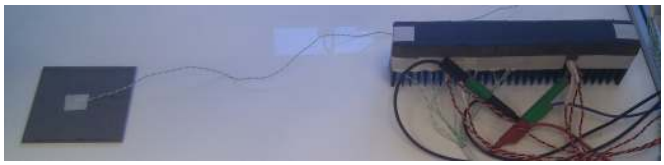
transitions also show a small drop in the device voltage during the device's initial current rise. This is produced primarily by the parasitic inductance in the main power loop, created by the PCB layout, interacting with the high di/dt of the transition. As can be seen the voltage drop is only approximately 5% of the DC-link voltage and hence could be neglected in the loss calculation of the design tool. During the turn-off transitions shown in Fig. 17d, 17e and 17f overshoot and ringing are observed on the device voltage waveforms. This too is caused by parasitic inductance of the power loop, however once again it produces a negligible switching energy that can also be ignored by the design tool (calculated at approximately 0.5% of the total turn-off energy). This can partly be attributed to the board layout, which was designed to minimise the length of the tracks that form the loop of Q1, Q2 and C_{dc} in Fig. 15, and to the choice of gate resistance that limited the magnitude of the di/dt experienced at the transition. Fig. 18 shows the turn-on and turn-off switching energy as a function of the drain current that were measured from all the DPTs conducted with a gate resistance of 24Ω. In order to compare these measurements, Cree's switching energy measurements given in the C2M0040120D datasheet [20] is also included in Fig. 18. The results clearly show the discrepancy that is created by the variations in the components and layout between the two measurement circuits as the experimentally measured turn-on switching energies are approximately 2 to 4 times higher than those from the datasheet, while the measured turn-off energies are approximately 2 times higher than the datasheet. Therefore in order to maximise the accuracy of the design optimisation tool, the switching energy data produced by the double pulse tests was used in place of Cree's datasheet information.

B. Heatsink Thermal Resistance Measurements

Like for the switching losses, the measured thermal resistance of a heatsink extrusion is highly dependent on the operating conditions of the measurement test. According to the heatsink manufacturers datasheet [21] used by the design tool, the thermal resistances were measured using 150 mm long extrusions in the vertical orientation, a sink-to-ambient temperature difference of 75°C and a uniform load on the heatsink base. While the datasheet provides information showing how

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

(a)



(b)

Fig. 19. Setup for thermal resistance measurements: (a) Device and wiring connections (b) Insulated heatsink and ambient temperature thermocouple plate

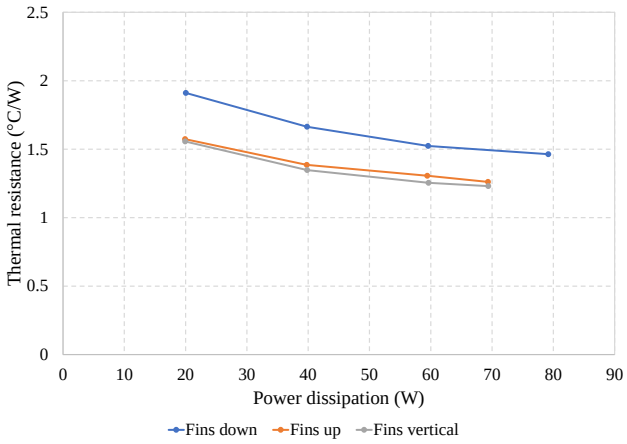


Fig. 20. Thermal resistance as a function of power dissipation for various heatsink fin orientations

the thermal resistance can be adjusted for different extrusion lengths and temperature differences, it does not provide any information on how to adjust for changes in orientation or for uneven thermal loads. In the case of commercial converters, the heatsink may have to be orientated in a particular way in order to fit with the dimensions of the enclosure. Furthermore, the devices and modules attached to the heatsink will not produce a uniform thermal load, especially in the case where multiple discrete devices are used as this leads to hotspots throughout the heatsink.

Thermal resistance measurements were carried out for a 40 mm long Aavid thermalloy 000EK type extrusion, as shown in Fig. 5a. The C2M0040120D devices were attached to the heatsink in the same manner that they would be for the optimised converter (see Fig. 16). In order to accurately control the power dissipated from the devices, the setup depicted in Fig. 19a was used. In this setup the drain-source terminals of the devices were connected in a single series chain with the gate terminals left unconnected. During the test a voltage was applied across the series chain with the positive potential being applied at the source end of the chain and the negative at the drain end so that heat was generated by current flowing through the internal body diodes of the devices. As a means of checking whether or not the body diodes of each device were contributing equally to the total power, twisted wire pairs were soldered across the source-drain terminals of each device in order to measure their voltage throughout the test. The current entering the experimental setup was measured by an LEM HX 05-P/SP2 current transducer. For each test, thermocouples were attached at various different locations on the heatsink with fiberglass tape. High performance polyamide 6 (nylon 6) foam was placed on the top side of the heatsink in order to limit the amount of heat that escapes from the system through the front of the device cases. In order to measure the ambient temperature a thermocouple was attached to an aluminium plate and placed away from the experimental setup as shown in Fig. 19b. The aluminium plate acted as a low-pass filter, preventing sudden changes in the ambient temperature from appearing in the measurements. The temperature, voltage and current measurements were recorded by an Agilent 34972A data acquisition and multiplexer unit.

To determine the effect of the fin orientation, thermal resistance measurements were recorded for three different heatsink orientations; the fins pointing directly down, the fins pointing directly up, and the fins pointing at a 90° angle to allow vertical airflow along the channels between the fins. For these tests just the two central devices were used so it could be assumed that the heat source was effectively a single point located in the centre of the heatsink between the two devices, and thus make the thermal resistance calculations of the heatsink simpler. The calculated thermal resistances from the assumed heat source point to the ambient air for the three orientations at various different power levels are shown in Fig. 20. In all cases the thermal resistance decreases with increasing power dissipation due the thermal energy being more able to spread throughout the heatsink and better utilise the entire geometry. Regardless of the changes with power dissipation, it is clear that the vertical airflow orientation (average $\Theta_{HS} = 1.347$°C/W) produces a lower thermal resistance than both the fins down ($\Theta_{HS} = 1.641$°C/W) and fins up ($\Theta_{HS} = 1.382$°C/W) orientations. For various design and measurement reasons, the heatsink of the optimised converter was orientated with its fins pointing down, thus resulting in a higher thermal resistance than the one predicted by the design optimisation tool.

If a uniform thermal load was applied to entire top surface of the heatsink, the temperature would be constant regardless of the position along its width. The thermal energy would travel through the baseplate to the fins, in a direction perpendicular to the top surface, at every position on that surface. Therefore the thermal resistance at every position would be equal as the path from the heat source to the ambient air would be identical. The uneven temperature distribution of the heatsink, resulting from hotspots generated by the devices, was measured by attaching thermocouples in the locations shown in Fig. 21a, the results of which, for various power dissipation levels, are shown in Fig. 21b. The thermal energy spreads out to create a thermal equilibrium however the fins located further away from the devices will require the heat to travel along

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

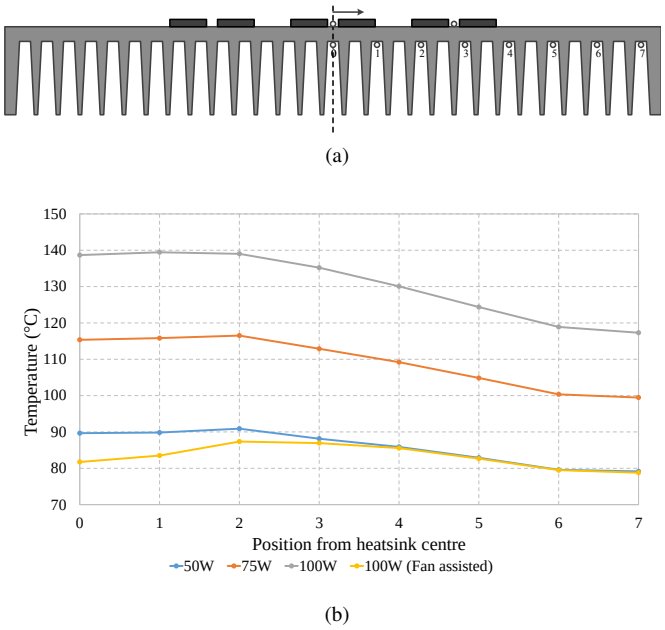


Fig. 21. Heatsink temperature profile: (a) Thermocouple locations, (b) Results for various power levels including fan assisted results

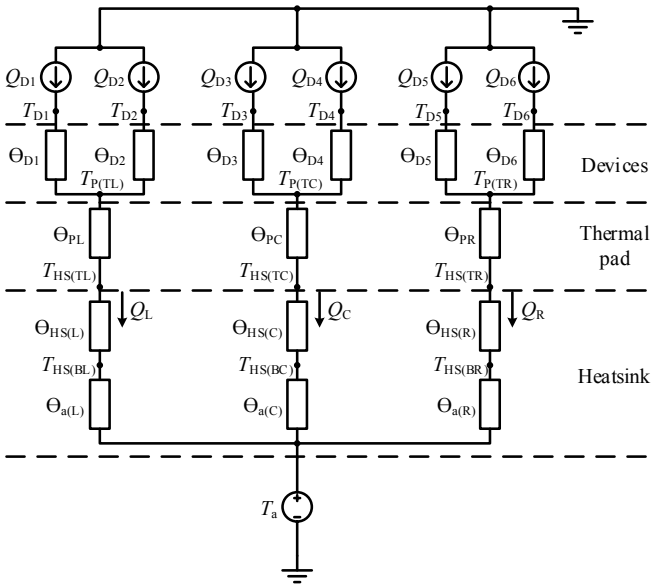


Fig. 22. Thermal model of devices and heatsink under typical operating conditions

paths of higher thermal resistance, thus causing the uneven temperature distribution. In essence the edges of the heatsink are under-utilised and therefore, in comparison to a uniform thermal load, the overall thermal resistance from the device junctions to ambient air is increased. Fig. 21b shows that for a power dissipation of 100 W (equivalent to the power dissipation occurring during the converter's rated full load) the temperature at the centre of the heatsink is in excess of the maximum operating temperature. Thus in order to obtain a thermal resistance equivalent to that determined by the model described in the design optimisation tool, a fan was placed at the centre of the heatsink, the results of which are also shown in Fig. 21b.

To determine the actual thermal resistance of the heatsink during operation (given the effects of the fins down orientation, the uneven thermal load and the assistance of the fan) the devices, the thermal pad (between the devices and the heatsink), and the heatsink itself were approximated by the thermal model shown in Fig. 22. The model assumes that the heatsink can be separated into three parts, one for each phase leg, where the heat generated by the devices on each phase leg passes through the heatsink into the ambient air without spreading out into the other two parts. Thus the thermal resistance of each branch can be calculated by measuring the ambient temperature (T_a), the temperature at the surface of the heatsink between the upper and lower devices of each phase leg ($T_{HS(Tx)}$) and the power dissipated in the devices ($\dot{Q}_{Dx}$). In reality heat from the two side phase legs spread into the centre phase legs while heat for the centre leg will also spread to side legs, altering the thermal resistance of each part of the model. However this assumption can still be useful if the temperatures on the top surface of the heatsink are almost equal (i.e. $T_{HS(TL)} = T_{HS(TC)} = T_{HS(TR)}$) as this allows the three heatsink branches in the model ($\Theta_{HS(x)} + \Theta_{a(x)}$) to be paralleled together which nearly eliminates the effect of the heat spreading between the parts. Using these assumptions and the temperature and power measurements obtained from the experiment, the thermal resistances of the devices, thermal pad and heatsink were calculated and the results are shown in Table IV.

TABLE IV
THERMAL MEASUREMENT RESULTS

Parameter	Value
Ambient temperature	25.60 °C
Device case temperature	107.3 °C
Pad temperature	89.59 °C
Heatsink temperature	82.62 °C
Device thermal resistance	1.084 °C/W
Pad thermal resistance	0.0680 °C/W
• per device	0.4081 °C/W
Heatsink thermal resistance	0.7016 °C/W
• per device	4.210 °C/W

In conclusion, the discrepancies between the heatsink datasheet information and the experimental measurements are due to differences in the heatsink's orientation and the uneven thermal load created by the multiple discrete devices. Experimental results showed that the heatsink orientation used by the optimisation design (fins down) resulted in an average thermal resistance 22% larger than the orientation used according to the datasheet (fins vertical). Additionally the thermocouple measurements revealed that the thermal hotspots created by the discrete devices produced a heatsink temperature profile at 100 W where the minimum and maximum temperatures differed by 22.1°C when the average temperature of the profile was 130.4°C. Both the orientation and uneven thermal load resulted in an increase in the thermal resistance of the heatsink such that a fan was required to reduce it to the level

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

assumed by the design tool. Future versions of the design tool will consider these experimental results so that more precise thermal designs can be achieved.

C. Device Loss Model Test and Validation

The device switching energy and the thermal resistances calculated in the previous sections were used to test the validity of the device loss model used in the design optimisation tool. This was done through a thermal superposition test where the converter was operated at the rated load for multiple different switching frequencies. The case temperature of all six devices were measured using thermocouples and covered over with polyamide 6 foam to minimise the heat transfer from the cases directly to the ambient air. The converter was run until it reached thermal equilibrium before the device temperatures were recorded and averaged over a set period of time. A thermal image of the setup with the insulation foam removed so that the devices are visible is shown in Fig. 23. Using the thermal resistances that were measured during the heatsink characterisation, the power loss of the devices were estimated for each switching frequency. The device switching energy that was measured during the double pulse tests was used by the design optimisation tool to simulate the device losses. Both the simulation and thermal superposition results are shown in Fig. 24 where they are plotted as the switching loss efficiency as a function of the switching frequency. The switching loss efficiency calculated from the experimental thermal superposition method at 40, 60 and 75 kHz was 98.8%, 98.3% and 97.8% respectively, where the difference between the simulation and thermal superposition results were 0.17%, 0.18% and 0.04% respectively. Using this close agreement between the simulation and experimental results, it can also be seen in Fig. 24 that at 100 kHz, the SiC converter will have an estimated efficiency of 97.5%. In conclusion the very close agreement between the simulation and experimental results, especially given the expected precision of the thermocouple temperature measurements, shows that the device loss model of the optimisation tool produces accurate results so long as the measured switching energy of the devices is used.

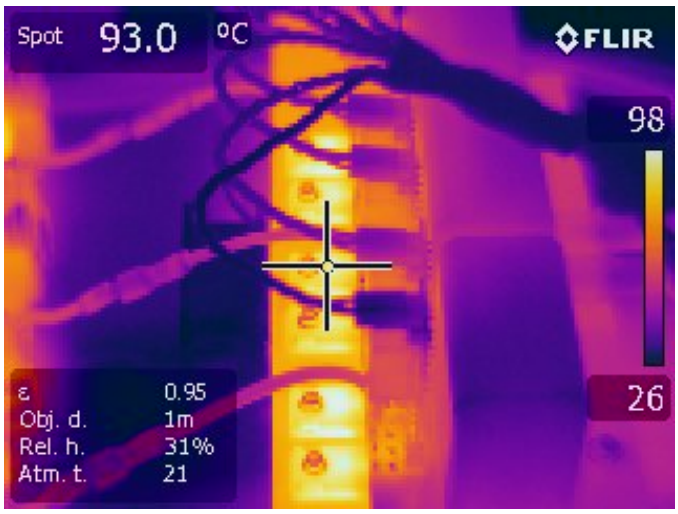


Fig. 23. Thermal image of the switching devices under fan assisted normal operation

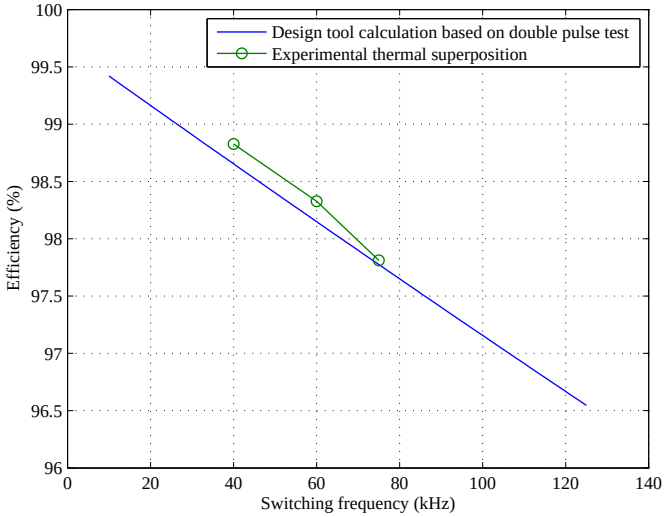


Fig. 24. Converter switching device efficiency as calculated by the design optimisation tool compared to the experimentally measured thermal superposition results

D. Line and EMI Filter Design Test and Validation

The models governing the line and EMI filters of the converter were tested through various electrical tests. The converter was subjected to the operating conditions given in Table I and each phase was loaded with 25Ω to ensure that the power draw of the converter didn't exceed the rated output of 5 kW. The converter was operated at 60 kHz rather than the optimised value of 63 kHz due to limitations in the control hardware. The input and output voltages, currents and power produced by this test are shown in Table V. As can be seen the targeted efficiency of 98% has almost been achieved. In order to demonstrate the converter operating as close as possible to the rated power, another test was conducted where all the operating conditions were kept the same except for the modulation index which was increased to 0.94. The results for this test are displayed in Table VI which shows an increase in the output power of 326.9 W while the power losses increase by only 3.1 W and the efficiency rises to 97.75%. The output phase to neutral voltage waveform of one phase and the output phase current waveforms of all three phases that were produced from this test are shown in Fig. 25.

The EMI filter design model was assessed by performing a frequency spectrum analysis on the output phase waveforms of the converter. To minimise any electrical noise not produced by the switching action of the devices, and so obtain a noise floor low enough to allow proper assessment of the DO-160E EMI standard, the converter was operated until it reached thermal equilibrium, at which point the waveform sampling method described in [31] was used. The sampled waveforms were averaged and decomposed into their DM and CM components for frequency spectrum analysis, the results of which are shown in Fig. 26a and 26b respectively. As can be seen the harmonics of interest that fall close to and within the range of the DO-160E standard (as marked by circles in

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

TABLE V
EXPERIMENTAL CONVERTER RESULTS ($V_{dc} = 600$ V, $M = 0.9$, $R_L = 25\Omega$, $f_0 = 400$ Hz AND $f_s = 60$ kHz)

Parameter	Value
DC-link voltage (V_{dc})	599.31 V
Output phase voltage (V_o)	187.05 V (rms)
Input current (I_i)	6.932 A
Output current (I_o)	7.225 A (rms)
Input power (P_i)	4.152 kW
Output power (P_o)	4.0543 kW
Power loss (P_{loss})	97.7 W
Efficiency (η)	97.65%

TABLE VI
EXPERIMENTAL CONVERTER RESULTS ($V_{dc} = 600$ V, $M = 0.94$, $R_L = 25\Omega$, $f_0 = 400$ Hz AND $f_s = 60$ kHz)

Parameter	Value
DC-link voltage (V_{dc})	599.32 V
Output phase voltage (V_o)	194.65 V (rms)
Input current (I_i)	7.482 A
Output current (I_o)	7.503 A (rms)
Input power (P_i)	4.482 kW
Output power (P_o)	4.3812 kW
Power loss (P_{loss})	100.8 W
Efficiency (η)	97.75%

Fig. 26a and 26b) are all well below the limit for both DM and CM components. The CM results are significantly lower than the limit and this is partially because the optimisation tool designed for the worst-case scenario where the load is a short-circuit. Therefore the frequency results are better than expected as increasing the resistance value of the load further reduces the harmonics. Though dead-time compensation was implemented in the PWM, there are still noticeable low order harmonics, e.g. multiples of fundamental frequencies (400 Hz) in the spectrum, which are primarily due to the regular-sampled PWM and various non-idealities of the converter such as unsymmetrical pulses, device voltage drop, switching

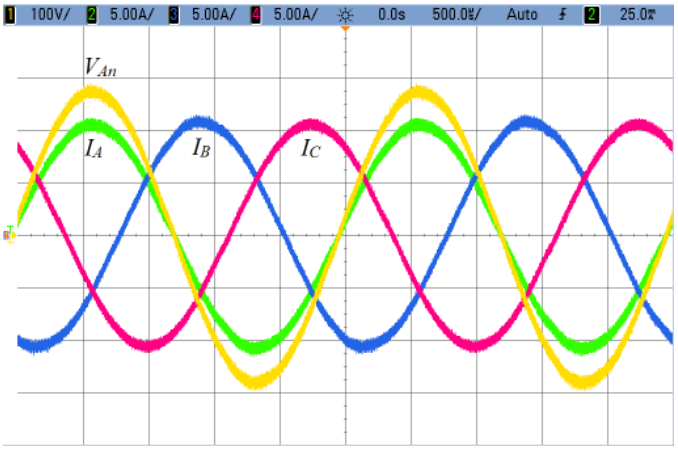
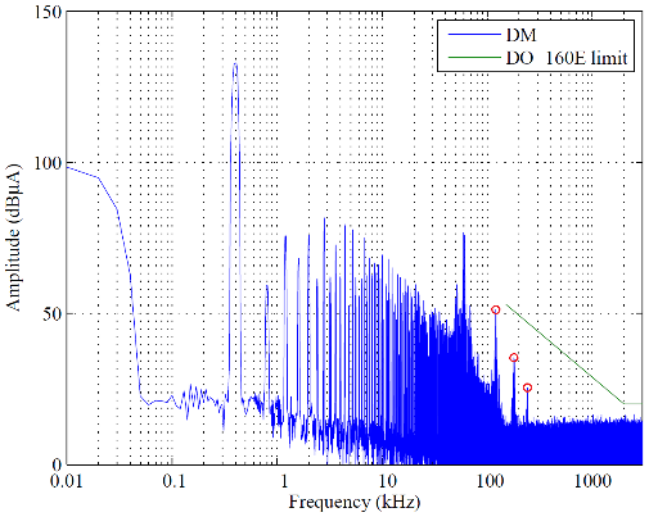
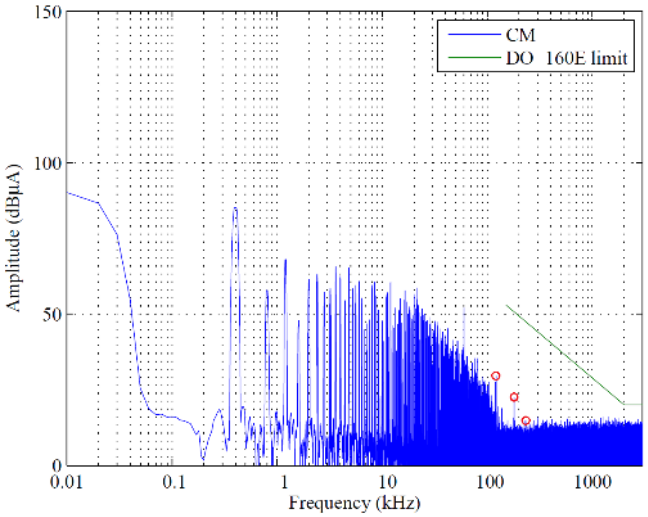


Fig. 25. Experimental output waveforms of the optimised converter operating at $V_{dc} = 600$ V, $M = 0.94$, $R_L = 25\Omega$, $f_0 = 400$ Hz and $f_s = 60$ kHz. Traces include Phase A output voltage (V_{An}), Phase A output current (I_A), Phase B output current (I_B), Phase C output current (I_C)



(a)



(b)

Fig. 26. Experimental converter output current (a) differential mode (DM) and (b) common mode (CM) component frequency spectrum for $V_{dc} = 600$ V, $M = 0.9$, $R_L = 25\Omega$, $f_0 = 400$ Hz and $f_s = 60$ kHz

transition (turn-on, turn-off) time, etc. In conclusion the results for both the DM spectrum and CM spectrum suggest that the model over-sizes the EMI filter components and that there is room for further volume reduction. This is because the design optimisation tool designs the DM and CM filters separately assuming the DM and CM components exclusively aid their respective filters. However in reality L_{DM} contributes to the CM filter and C_{CM} contributes to the DM filter, thus improving the attenuation of both.

V. CONCLUSION

In conclusion this paper has presented a design optimisation tool that can optimise the volume or mass of a 3-phase 2-level DC-AC converter that uses SiC switching devices. The component models governing the design tool (including the device, heatsink and passive components) were discussed in light of a design example which was subsequently built into an experimental converter that was used to assess the

performance of these models. Using SiC MOSFETs the design tool produced a converter with a power density of 3.503 kW/L which is 159.4% higher than one based on Si IGBTs. The algorithm structure of the converter has been discussed along with methods that can be used to improve its computational efficiency. The algorithm improved computational speed by reducing the number of potential designs by over 99.9%. Discussions based on measurements that were made of the SiC device switching energy loss and of the heatsink thermal resistance, explained the external conditions that result in discrepancies between manufacturer and experimental data. Furthermore examination of the experimental converter revealed that the device models accurately predict the power losses, and the output EMI filter was shown to meet the design specifications. The experimental converter achieved a measured efficiency of 97.75% at a switching frequency of 60 kHz.

However as was discussed, the design optimisation tool does have some limitations. The main one is its dependence on datasheet information that can potentially be inaccurate and/or incomplete such as was the case with the switching energy data and the heatsink thermal resistance. However it should be noted that this limitation can be overcome by performing pre-experimental characterisation, as was done in section IV-A and IV-B. Another limitation is the absence of PCB parasitics in the model and their effect on the switching performance. Despite the fact that they were observed to be almost negligible in the experimental results of the converter presented here, these parasitics could however cause problems for other circuits where the PCB layout has not been carefully designed. The absence of a detailed thermal model that factors in the orientation and the position of the devices on the heatsink limited the accuracy of the tool. However since this information is not given in manufacturer datasheets, experimental measurements, as were carried out here, are the only valid means of accounting for these attributes. Lastly the worst case scenario design methodology used on the EMI filter lead to a slightly oversized design that lowered the overall power density.

Future work will focus on better understanding the switching energy losses created by the gate drive circuit and the PCB layout. Work will also be carried out into understanding the effect of localised heat sources and thermal spreading in order to improve the heatsink design models. Finally, this work determined the total converter volume from the sum of the individual volume envelopes of the components. In reality the geometric layout of the components will determine the true volume of the converter. Future work will investigate how the design tool can optimise this part of the design.

REFERENCES

[1] R. Jayabalan, B. Fahimi, A. Koenig, and S. Pekarek, "Applications of power electronics-based systems in vehicular technology: state-of-the-art and future trends," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 3, Jun. 2004, pp. 1887–1894.

[2] J. Miller, "Power electronics in hybrid electric vehicle applications," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, vol. 1, Feb. 2003, pp. 23–29.

[3] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[4] H. Choi, "Overview of silicon carbide power devices," Fairchild Semiconductor.

[5] N. Oswald, P. Anthony, N. McNeill, and B. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2393–2407, May 2014.

[6] B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. McNutt, A. Lostetter, J. S. Lee, and K. Shiozaki, "A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2606–2617, May 2014.

[7] G. Calderon-Lopez, A. Forsyth, D. Gordon, and J. McIntosh, "Evaluation of SiC BJTs for high-power DC-DC converters," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2474–2481, May 2014.

[8] J. Rabkowski, D. Peftitsis, and H.-P. Nee, "Parallel-operation of discrete SiC BJTs in a 6-kW/250-kHz DC/DC boost converter," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2482–2491, May 2014.

[9] R. Lai, F. Wang, Y. Pei, R. Burgos, and B. Dushan, "Minimizing passive components in high-frequency high-density AC active voltage source converters," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, Jun. 2007, pp. 672–677.

[10] K. Shenai, "Silicon carbide power converters for next generation aerospace electronics applications," in *National Aerospace and Electronics Conference, 2000. NAECON 2000. Proceedings of the IEEE 2000*, 2000, pp. 516–523.

[11] I. Takahashi, "SiC power converter technology in future," in *Electric Machines and Drives Conference, 2003. IEMDC'03. IEEE International*, vol. 3, Jun. 2003, pp. 1903–1908.

[12] J. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli, and S. Round, "PWM converter power density barriers," in *Power Conversion Conference - Nagoya, 2007. PCC '07*, Apr. 2007, pp. 9–29.

[13] J. Biela, U. Badstuebner, and J. Kolar, "Impact of power density maximization on efficiency of DC-DC converter systems," *Power Electronics, IEEE Transactions on*, vol. 24, no. 1, pp. 288–300, Jan. 2009.

[14] R. Lai, F. Wang, R. Burgos, Y. Pei, D. Boroyevich, B. Wang, T. Lipo, V. Immanuel, and K. Karimi, "A systematic topology evaluation methodology for high-density three-phase PWM AC-AC converters," *Power Electronics, IEEE Transactions on*, vol. 23, no. 6, pp. 2665–2680, Nov. 2008.

[15] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. Kolar, "Comprehensive design and optimization of a high-power-density single-phase boost PFC," *Industrial Electronics, IEEE Transactions on*, vol. 56, no. 7, pp. 2574–2587, Jul. 2009.

[16] C.-m. Ho, H. Breuninger, S. Pettersson, G. Escobar, L. Serpa, and A. Coccia, "Practical design and implementation procedure of an interleaved boost converter using SiC diodes for PV applications," *Power Electronics, IEEE Transactions on*, vol. 27, no. 6, pp. 2835–2845, Jun. 2012.

[17] A. Nawawi, C. F. Tong, Y. Liu, A. Sakanova, S. Yin, Y. Liu, K. Men, K. Y. See, K. Tseng, R. Simanjorang, C. Gajanayake, and A. Gupta, "Design of high power density converter for aircraft applications," in *Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS), 2015 International Conference on*, Mar. 2015, pp. 1–6.

[18] F. Casanellas, "Losses in pwm inverters using IGBTs," *Electric Power Applications, IEE Proceedings -*, vol. 141, no. 5, pp. 235–239, Sep. 1994.

[19] S. Dieckerhoff, S. Bernet, and D. Krug, "Power loss-oriented evaluation of high voltage IGBTs and multilevel converters in transformerless traction applications," *Power Electronics, IEEE Transactions on*, vol. 20, no. 6, pp. 1328–1336, Nov. 2005.

[20] C. Inc., "C2M0040120D datasheet," Cree Inc., 4600 Silicon Drive, Durham, NC 27703. [Online]. Available: http://http://cree.com/Power/Products/MOSFETs/TO247/C2M0040120D

[21] *2002 Extrusion Selection Guide Power Profiles for the European Market*, Aavid Thermalloy, 80 Commercial Street, Concord, New Hampshire, USA, 2002.

[22] B. Karanayil, V. Agelidis, and J. Pou, "Performance evaluation of three-phase grid-connected photovoltaic inverters using electrolytic or polypropylene film capacitors," *Sustainable Energy, IEEE Transactions on*, vol. 5, no. 4, pp. 1297–1306, Oct. 2014.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2705805, IEEE Transactions on Power Electronics

[23] J. Kolar, T. Wolbank, and M. Schrodl, "Analytical calculation of the RMS current stress on the DC link capacitor of voltage DC link PWM converter systems," in *Electrical Machines and Drives, 1999. Ninth International Conference on (Conf. Publ. No. 468)*, 1999, pp. 81–89.

[24] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 7, pp. 2950–2964, Sep. 2012.

[25] J. Loncarski, *Peak-to-Peak Output Current Ripple Analysis in Multiphase and Multilevel Inverters*. Springer, 2014.

[26] *Environmental Conditions and Test Procedures for Airborne Equipment*, RTCA Inc. Std. DO-160E, 2004.

[27] G. D. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. IEEE Press & Wiley-Interscience, 2003.

[28] A. Kempski, "EMI noise splitting into common and differential modes in PWM inverter drive system," in *IEEE Compatibility in Power Electronics, 2005.*, Jun. 2005, pp. 200–203.

[29] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, 3rd ed. John Wiley & Sons, inc., 2003.

[30] I. Laird, J. Scoltock, A.J.Forsyth, and X. Yuan, "A unified framework for computationally efficient power converter design optimisation," in *Power Electronics, Machines and Drives, 2016, PEMD'16, IET Conference on*, Apr. 2016, pp. 1–6.

[31] N. Oswald, B. H. Stark, N. McNeill, and D. Holliday, "High-bandwidth, high-fidelity in-circuit measurement of power electronic switching waveforms for EMI generation analysis," in *2011 IEEE Energy Conversion Congress and Exposition*, Sep. 2011, pp. 3886–3893.

Ian Laird (S'09-M'11) received both the B.Eng. degree (Hons. I) in mechatronic engineering in 2008 and the PhD degree in electrical engineering (power electronics) in 2013 from the University of Sydney, NSW, Australia. From 2008 to 2009 he worked at the CSIRO material science and engineering division in Lindfield, NSW, Australia in the thermoelectric energy group. Since 2014 he has been a research associate with the Electrical Energy Management Group (EEMG) at the University of Bristol as part of its work with the EPSRC Centre for Power Electronics. His research interests include thermoelectrics, converter topologies, wide band-gap devices and design optimisation.

Xibo Yuan (S'09-M'11-SM'15) received the B.S. degree from China University of Mining and Technology, Xuzhou, China, and the Ph.D. degree from Tsinghua University, Beijing, China, in 2005 and 2010, respectively, both in electrical engineering.

He is currently a Reader in the Electrical Energy Management Group, Department of Electrical and Electronic Engineering, University of Bristol, Bristol, U.K. He also holds a Royal Academy of Engineering/Safran Senior Research Fellowship. He was a Visiting Scholar at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, and the Institute of Energy Technology, Aalborg University, Denmark. He was a Postdoctoral Research Associate in the Electrical Machines and Drives Research Group, Department of Electronic and Electrical Engineering, University of Sheffield, Sheffield, U.K.

His research interests include power electronics and motor drives, wind power generation, multilevel converters, application of wide-bandgap devices, and more electric aircraft technologies.

James Scoltock (S'09-M'15) received the B.E. (Hons) and Ph.D. degrees, both in electrical and electronic engineering, from The University of Auckland, New Zealand, in 2009 and 2015, respectively. He is currently a Research Assocaite with the School of Electrical and Electronic Engineering, The University of Manchester, United Kingdom. His research interests include power electronics, electrical drives, and model predictive control.

Andrew J. Forsyth (M'98-SM'06) received the B.Sc.(Eng) degree in electrical engineering from Imperial College, London, U.K., in 1981 and the Ph.D. degree in power electronics from the University of Cambridge, Cambridge, U.K., in 1987.

He was a Design Engineer with GEC Electrical Projects Ltd from 1981 to 1983, a Lecturer at the University of Bath from 1986-1990, and a Lecturer / Senior Lecturer at Birmingham University from 1991 to 2004. Since 2004 he has been Professor of Power Electronics at the University of Manchester, Manchester U.K. His research interests include high-frequency converters and magnetic components, wide-band-gap device applications, more-electric aircraft and electric vehicle systems.