A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy

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***Abstract*—In this brief, a systematic design procedure for a second-order all-digital phase-locked loop (PLL) is proposed. The design procedure is based on the analogy between a type-II second-order analog PLL and an all-digital PLL. The all-digital PLL design inherits the frequency response and stability characteristics of the analog prototype PLL.**

***Index Terms*—All-digital phase-locked loop (PLL), bilinear transform, digital loop filter, digitally controlled oscillator.**

I. Introduction

RECENT advances in integrated circuit (IC) technology make fabrication processes very suitable for digital designs. Small-area and low-voltage designs are mandated by market requirements. Another advantage of a digital design is its scalability and easy redesign with process changes or shrinks. Since analog blocks are present in a number of digital and mixed-signal ICs, their redesign is an important factor in the release of a new product. However, the performance requirements of analog blocks necessitates a complete redesign in a new process, thereby increasing the design cycle time. Reducing the amount of analog circuitry can improve the redesign of these mixed-signal ICs.

Recently, several digital and all-digital phase-locked loops (PLLs) for different applications (including multigigahertz ones) have been reported [1]–[4]. They demonstrate the ability of a digital implementation to achieve the performance of analog PLLs and even outperform them. There are several other advantages of a digital implementation of PLLs. These include eliminating the noise-susceptible analog control for a voltage-controlled oscillator (VCO) and the inherent noise immunity of digital circuits.

Analog PLLs (Fig. 1) have been investigated for the past several decades. As a result, different types and orders of analog PLLs have been analyzed and procedures for their design have been developed. Second-order analog PLLs have been analyzed by Hein and Scott [5] and Gardner [6]. Several other references [7]–[9] provide an analysis and design procedure for third-order charge-pump PLLs (CPPLLs). But there is only limited research dedicated to the analysis of all-digital PLLs (ADPLLs). Phase-domain ADPLLs have been analyzed in [2] and [10]. In [11], the root locus technique has been applied to analyze the effect of the digital loop filter parameters on the bandwidth and stability of an ADPLL. However, none of these publications presents a procedure for designing an all-digital PLL given required bandwidth and phase margin specifications.

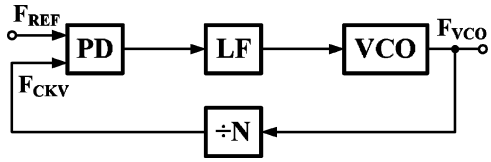

Fig. 1. Analog PLL.

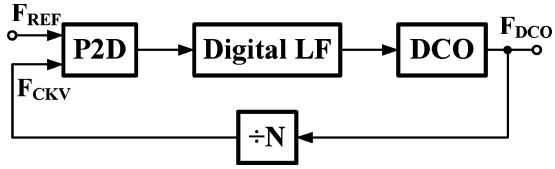

Fig. 2. All-digital PLL.

This brief is focused on a design approach for type-II second-order all-digital PLLs and forms the basis for a systematic design procedure starting from the ADPLL specifications. In general, the proposed approach can be extended for the design of all-digital PLLs with different types and orders.

The brief is organized as follows. Section II gives an overview of typical all-digital PLLs. The discussion on the importance of the time-to-digital converter (TDC) resolution is given in Section III. In Section IV, a design flow for the ADPLL is described. A design example of a second-order all-digital PLL is presented in Section V. Finally, conclusions are provided in Section VI.

II. Overview of All-Digital PLLs

A simplified block diagram of the all-digital PLL for a microprocessor or serial link application is shown in Fig. 2. It consists of a phase-to-digital converter (P2D), a digital loop filter (LF), a digitally controlled oscillator (DCO), and a feedback divider. The P2D senses the phase difference between the reference clock F_{REF} and the DCO divided clock F_{CKV} and converts it to a digital format. This information is filtered by the first-order digital LF and then is used to control the DCO. In the

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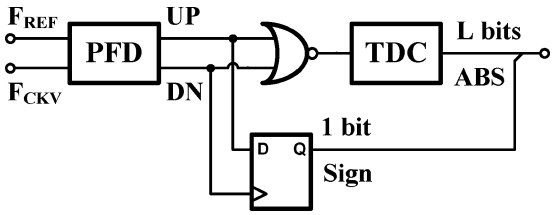

Fig. 3. Typical implementation of a P2D converter.

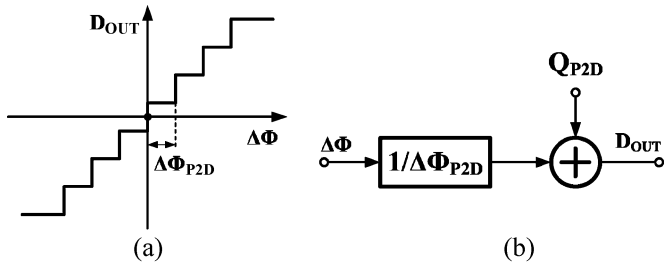

Fig. 4. (a) Transfer characteristic of P2D. (b) Linear model of P2D.

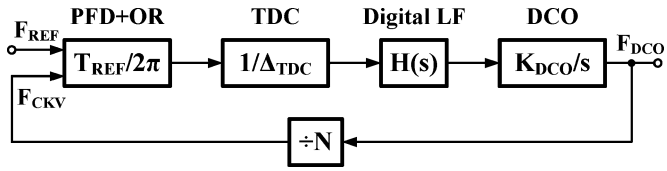

Fig. 5. s-domain approximation of the ADPLL.

case of a ring-oscillator-based DCO, frequency tuning can be performed by digitally turning on and off bias current sources. When an *LC*-based DCO is employed, frequency tuning is done by switching on and off the tank capacitors. The P2D can be implemented in many different ways. One way, shown in Fig. 3, features a conventional phase/frequency detector (PFD) followed by a time-to-digital converter. It is beneficial to use a PFD instead of just a phase detector in order to expand the frequency lock range. The PFD produces up (UP) and down (DN) pulses. They are overlapped by an OR gate to create a pulse, the width of which is proportional to the absolute value of the phase error. The width of this pulse is digitized by a TDC with a resolution $\Delta_{\rm TDC}$ and an L-bit output ABS is produced. The D-flip-flop samples the UP pulse on the rising edge of the DN pulse. In this manner, the sign of the phase/frequency error can be determined.

The ADPLL of Fig. 2 has a structure and operation very similar to a second-order CPPLL. The principal difference is that the phase error information is processed in different domains. In the all-digital PLL, the UP and DN pulses are overlapped, and the result is digitized and processed by a digital filter. For the CPPLL, a charge pump (CP) is used to generate a charge which is proportional to the time difference between the UP and DN pulses. The resulting charge is pumped into the analog filter, the output voltage of which controls the VCO. This similarity allows one to extend the design procedure for a second-order CPPLL to a second-order ADPLL.

III. TDC Resolution

The operation of an ADPLL fully depends on the TDC resolution, since it defines the resolution of the phase detector. Assuming that the period of the reference signal $T_{\rm REF}$ remains unchanged over time, the time resolution of the TDC can be converted in to a phase resolution of the phase-to-digital converter as

$$\Delta\Phi_{\rm P2D} = \frac{2\pi\Delta_{\rm TDC}}{T_{\rm REF}}. \tag{1}$$

Fig. 4(a) shows a representative characteristic of the P2D, where the input phase difference is noted as $\Delta\Phi$. The relation between $\Delta\Phi$ and the phase resolution of the P2D determines the applicability of a linear analysis for the ADPLL. If the input phase error $\Delta\Phi$ is smaller than the resolution of the P2D converter, the behavior of the P2D is no different from a bang-bang phase detector. A linear analysis is not applicable in this case, and thus the bandwidth in a strict sense is not defined. The interested reader is referred to [12] for further discussion on this topic.

On the other hand, if the input phase error $\Delta\Phi$ is much larger than the resolution of the P2D converter, the input phase error is digitized in a linear manner. The P2D can be modeled as a gain of $1/\Delta\Phi_{\rm P2D}$ plus quantization noise as in Fig. 4(b). Having a linear phase detector allows us to use linear techniques for the analysis of ADPLLs. The noise contribution of a TDC is given in [13].

IV. Design Flow for an ADPLL

It is beneficial to have a clear procedure for calculating the ADPLL parameters. Given a set of specifications, which usually include the phase margin (PM), the unity gain bandwidth $(\omega_{\rm UGBW})$, and the reference frequency $(F_{\rm REF})$, a designer should choose the loop filter parameters. This task can be accomplished by comparing s-domain models for digital and charge-pump PLLs. A conventional CPPLL has three poles and a zero. The third pole is introduced in order to attenuate the ripple which appears due to the nature of the CPPLL. In all-digital PLLs, this problem does not exist, and a second-order PLL is sufficient.

A. s-domain Model for a Second-Order ADPLL

An s-domain approximation for the second-order ADPLL is shown in Fig. 5. The phase-frequency detector together with the OR gate converts the input phase error into an output pulse of width Δt. The transfer function of the PFD can be approximated as

$$\mathrm{PFD}(s) = \frac{T_{\rm REF}}{2\pi}. \tag{2}$$

The pulsewidth Δt is digitized by a time-to-digital converter with a resolution of $\Delta_{\rm TDC}$. Usually, the resolution of the TDC is limited to one inverter delay and is considered to be fixed in our design approach. The transfer function of this operation can be approximated as

$$\mathrm{TDC}(s) = \frac{1}{\Delta_{\rm TDC}}. \tag{3}$$

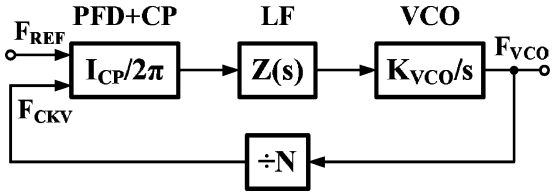

Fig. 6. s-domain model for a second-order CPPLL.

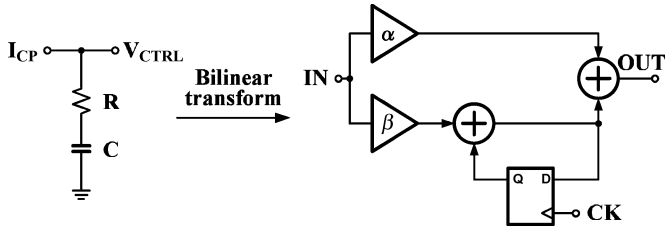

Fig. 7. Transform from an analog to a digital loop filter.

Combining (2) and (3), the joint PFD and TDC transfer function (P2D) can be obtained as

$$\mathrm{P2D}(s) = \frac{T_{\mathrm{REF}}}{2\pi\Delta_{\mathrm{TDC}}}. \tag{4}$$

The phase error in the digital domain is filtered by a first-order digital loop filter and then fed to the DCO with a transfer function given by

$$\mathrm{DCO}(s) = \frac{K_{\mathrm{DCO}}}{s}. \tag{5}$$

When comparing this model to the s-domain model for a second-order CPPLL (Fig. 6), it can be seen that they are the same if

$$\begin{aligned} I_{\mathrm{CP}} &= \frac{T_{\mathrm{REF}}}{\Delta_{\mathrm{TDC}}} \\ K_{\mathrm{VCO}} &= K_{\mathrm{DCO}} \\ Z(s) &= H(s). \end{aligned} \tag{6}$$

Thus, in order to design an ADPLL given a set of specifications, first a CPPLL can be designed. Then, the specific parameters of the ADPLL can be calculated based on the relationships given in (6).

B. Design of a Second-Order CPPLL

Let us consider I_{CP} and K_{VCO} as predetermined constants. For the ADPLL, I_{CP} is equivalent to the ratio of a reference clock period T_{REF} to the resolution of the TDC (Δ_{TDC}), and K_{VCO} is equivalent to K_{DCO}. A loop filter for the second-order CPPLL consists of a capacitor and a resistor connected in series. The capacitor value C and the resistor value R are the only unknowns.

The open loop gain of the CPPLL in Fig. 6 is given by

$$\mathrm{LG}(s) = \frac{I_{\mathrm{CP}}}{2\pi}\frac{K_{\mathrm{VCO}}}{s}\frac{1}{N}\frac{s+\omega_z}{s}R \tag{7}$$

where ω_z is the zero frequency

$$\omega_z = \frac{1}{RC}. \tag{8}$$

The phase margin for this system is given by

$$\mathrm{PM} = \arctan\left(\frac{\omega_{\mathrm{UGBW}}}{\omega_z}\right). \tag{9}$$

From (9), the required zero frequency ω_z can be found as

$$\omega_z = \frac{\omega_{\mathrm{UGBW}}}{\tan(\mathrm{PM})}. \tag{10}$$

Based on $|\mathrm{LG}(j\omega_{\mathrm{UGBW}})| = 1$, the resistance value R can be found in a unique way as

$$R = \frac{2\pi N}{I_{\mathrm{CP}}K_{\mathrm{VCO}}}\frac{\omega_z^2}{\sqrt{\omega_z^2+\omega_{\mathrm{UGBW}}^2}}. \tag{11}$$

Then, from (8) and (10), the capacitance value C is found to be

$$C = \frac{\tan(\mathrm{PM})}{R\omega_{\mathrm{UGBW}}}. \tag{12}$$

C. Calculation of the Digital Loop Filter Coefficients

A digital equivalent of an analog loop filter consists of a proportional path with a gain α and an integral path with a gain β. The parameters of a digital loop filter α and β can be obtained from the parameters of an analog loop filter R and C by using the bilinear transform (Fig. 7). The bilinear transform (13) is commonly used to design digital filters based on their analog prototypes [14]

$$s = \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}} \tag{13}$$

where T_s is the sampling time of a discrete-time system, which is the inverse of the reference frequency in our case.

Our goal is to preserve the frequency response and stability of the system; thus, the bilinear transform is an obvious choice. The only disadvantage of the bilinear transform is frequency warping. This affects the frequency response at frequencies close to the Nyquist rate. Since the bandwidth of the PLL is at least ten times smaller than the update rate, frequency warping will have a negligible effect.

The z-domain transfer function of the digital loop filter is given by

$$H(z) = \alpha + \beta\frac{1}{1-z^{-1}} = \frac{(\alpha+\beta)-\alpha z^{-1}}{1-z^{-1}} \tag{14}$$

where α represents the proportional part and β represents the integral part of the loop filter gain.

The s-domain transfer function of the analog loop filter, given by (15), can be converted to the z-domain via the bilinear transform as follows:

$$Z(s) = \frac{V(s)}{I(s)} = R + \frac{1}{sC} \tag{15}$$

$$Z(s) \overset{s\to z}{=} \frac{\left(\frac{T_s}{2C}+R\right)+z^{-1}\left(\frac{T_s}{2C}-R\right)}{1-z^{-1}}. \tag{16}$$

Comparing (14) and (16), α and β can be found as

$$\alpha = R - \frac{T_s}{2C}$$
$$\beta = \frac{T_s}{C} \tag{17}$$

where α and β are the only unknown parameters that need to be determined for the ADPLL design at this stage.

D. Relationship Between α and β

As a consequence of the analysis presented above, a simple relationship between the proportional gain α and the integral gain β can be established. From (17), the ratio of α to β is found to be

$$\frac{\alpha}{\beta} = \frac{RC}{T_s} - \frac{1}{2}. \tag{18}$$

Then, R and C from (11) and (12), respectively, are substituted into (18) to yield

$$\frac{\alpha}{\beta} = \frac{1}{T_s}\frac{\tan(\mathrm{PM})}{\omega_{\mathrm{UGBW}}} - \frac{1}{2}. \tag{19}$$

Given that $T_s = 1/F_{\mathrm{REF}}$ and $\omega_{\mathrm{UGBW}} = 2\pi F_{\mathrm{UGBW}}$, (19) can be expressed as

$$\frac{\alpha}{\beta} = \frac{F_{\mathrm{REF}}}{F_{\mathrm{UGBW}}}\frac{\tan(PM)}{2\pi} - \frac{1}{2}. \tag{20}$$

It can be seen from (20) that, for the given ADPLL reference frequency F_{REF} and the unity gain bandwidth F_{UGBW}, the α-to-β ratio defines the phase margin and thus the stability of a system.

V. Design Example

To validate the proposed approach, an all-digital PLL with the following specifications has been designed:

- phase margin $PM = 45°$;
- unity gain bandwidth $F_{\mathrm{UGBW}} = 1$ MHz;
- reference frequency $F_{\mathrm{REF}} = 80$ MHz;
- feedback divider $N = 16$;
- DCO gain $K_{\mathrm{DCO}} = 1$ MHz/LSB;
- TDC resolution $\Delta_{\mathrm{TDC}} = 20$ ps.

The phase margin has been intentionally chosen to be 45° in order to have ringing in the PLL's step response. This allows for better visual comparison of the step responses obtained by different methods. If a conventional inverter chain-based TDC is used, fine resolution ($\Delta_{\mathrm{TDC}} = 20$ ps) is possible only in a deep-submicrometer CMOS process. There are other types of TDC as in [15] and [16] which can overcome this limitation.

The calculation starts with (10) from which, using the specifications for the unity gain bandwidth and phase margin, the required zero frequency is found to be $\omega_z = 6.28 \cdot 10^6$ rad/s. Given the DCO gain K_{DCO}, the resolution of the TDC, Δ_{TDC}, and the period of the reference clock $T_s = 1/F_{\mathrm{REF}}$, I_{CP} and K_{VCO} are determined from (6). Based on that, the equivalent resistance $R = 1.14 \cdot 10^{-1}\ \Omega$ is calculated from the (11). Then, the equivalent capacitance $C = 1.4 \cdot 10^{-6}$ F is determined using (12). Finally, the digital loop filter parameters α and β have been determined from (17). For easy hardware implementation, the coefficients of the digital loop filter have to be approximated as power of two values:

- $\alpha = 1.09 \cdot 10^{-1} \cong 2^{-3}$;
- $\beta = 8.93 \cdot 10^{-3} \cong 2^{-7}$.

The above approximation affects the effective loop bandwidth and phase margin of the designed ADPLL. For the designed ADPLL, the effective phase margin is $PM = 50.3°$ and the effective unity gain bandwidth is $\mathrm{UGBW} = 1.01$ MHz.

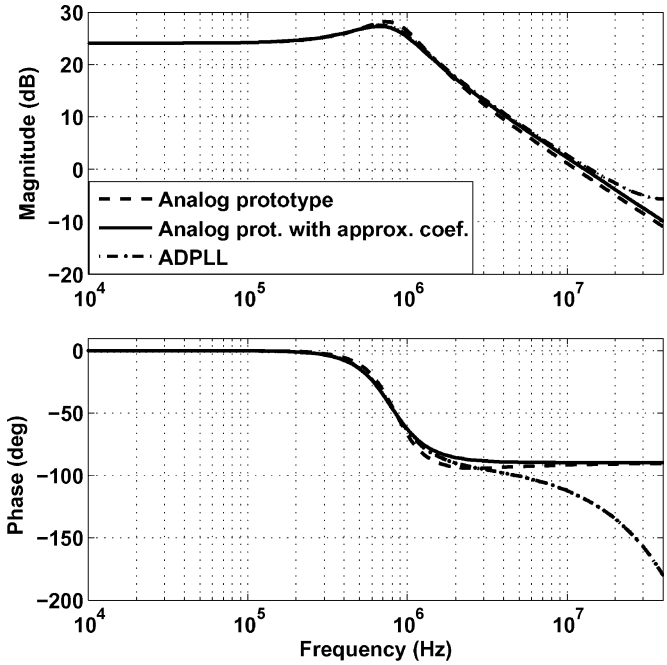

Fig. 8. Magnitude and phase responses of the ADPLL.

The magnitude and phase responses of the analog prototype, the analog prototype with coefficients approximated for the digital implementation, and the resulting ADPLL have been calculated and are shown in Fig. 8.

In Fig. 8, peaking of the magnitude responses is due to the low phase margin. An s-domain prototype inaccurately models an ADPLL at frequencies close to the Nyquist rate; thus, there are differences between the frequency responses at higher frequencies. Since the unity gain bandwidth of the ADPLL is a factor of 80 smaller than its reference frequency, the phase and frequency responses of the analog prototype and the ADPLL transfer functions are in good agreement in the band of interest.

The step response has been used to validate the design. Fig. 9(a) shows two step responses obtained in different ways. The dashed line represents the step response calculated in MATLAB from the s-domain transfer function using the "step" function. The solid line shows the step response obtained by a time-domain simulation of the designed all-digital PLL in Simulink. It can be seen that the plots are in good agreement. This demonstrates that the designed ADPLL behaves similar to the initial s-domain prototype. The results from the time-domain simulation of the CPPLL are not shown in this figure because of ripples. However, the filtered step response matches the s-domain calculations.

Two additional all-digital PLLs for a target $\mathrm{UGBW} = 1$ MHz and target phase margins of 20° and 80° have been designed.

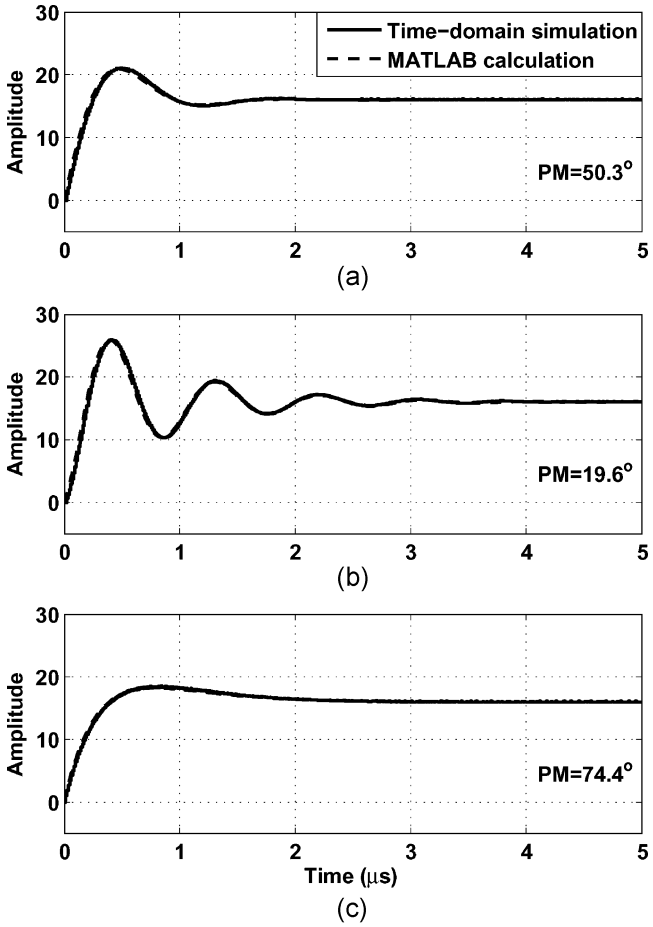

Fig. 9. Step response for an all-digital PLL. (a) $\mathrm{PM} = 50.3°$. (b) $\mathrm{PM} = 19.6°$. (c) $\mathrm{PM} = 74.4°$.

TABLE I
SUMMARY OF ADPLL DESIGNS

Target PM	α	β	$\frac{\alpha}{\beta}$	PM	UGBW, MHz
$20°$	2^{-4}	2^{-6}	4	$19.6°$	1.16
$45°$	2^{-3}	2^{-7}	16	$50.3°$	1.01
$80°$	2^{-3}	2^{-9}	64	$74.4°$	0.81

Their step responses are shown in Fig. 9(b) and (c). Once again, it is seen that the s-domain prototype and the ADPLL behave similarly. Table I summarizes the loop filter parameters and the effective PM and UGBW for all three ADPLL designs.

VI. CONCLUSION

In this brief, a simple and systematic procedure for the design of a second-order all-digital PLL has been presented. Closed-form expressions have been derived for the digital loop filter parameters. Based on this analysis, an ADPLL can be easily designed from specifications. The procedure presented in this brief has been used for the design of a oversampled ($F_{\mathrm{REF}} \gg F_{\mathrm{UGBW}}$) second-order all-digital PLL where the s-domain approximation has proven to be sufficiently accurate in the design of traditional/analog PLLs. A time-domain step response simulation is in good agreement with a calculation of the step response in MATLAB using the ADPLL transfer function.

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