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A digital noise and sine-wave generator

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A circuit is described that will digitally generate three kinds of signal useful in auditory research: broad-band pseudorandom noise, low-pass-filtered Gaussian noise, and low-distortion sine waves. This digital circuit has two advantages over its analog counterparts, ease of calibration and adaptation to computer control.

A shift register, clock, and "exclusive-or" feedback circuit are often used to generate broad-band pseudo-random binary sequence (PRBS) noise (Barnes, Gutmann, & Hodgson, 1974; Damashek, 1976; Feth, 1970). If a simple resistive weighting network (digital filter) is added to the standard PRBS circuit, it can also generate low-pass filtered noise with a Gaussian amplitude distribution. In addition, if the usual feedback arrangement is modified, the output becomes a low-distortion sinusoid. The schematic diagram of a simplified 32-bit PRBS generator that incorporates these two modifications is shown in Figure 1. (The parts list for this device is shown in Table 1).

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SOME PROPERTIES OF PRBS NOISE

The individual logic level pulses that make up the PRBS noise can be taken from the output of any stage of the shift register of Figure 1. The duration of these pulses appears to be random because the probability

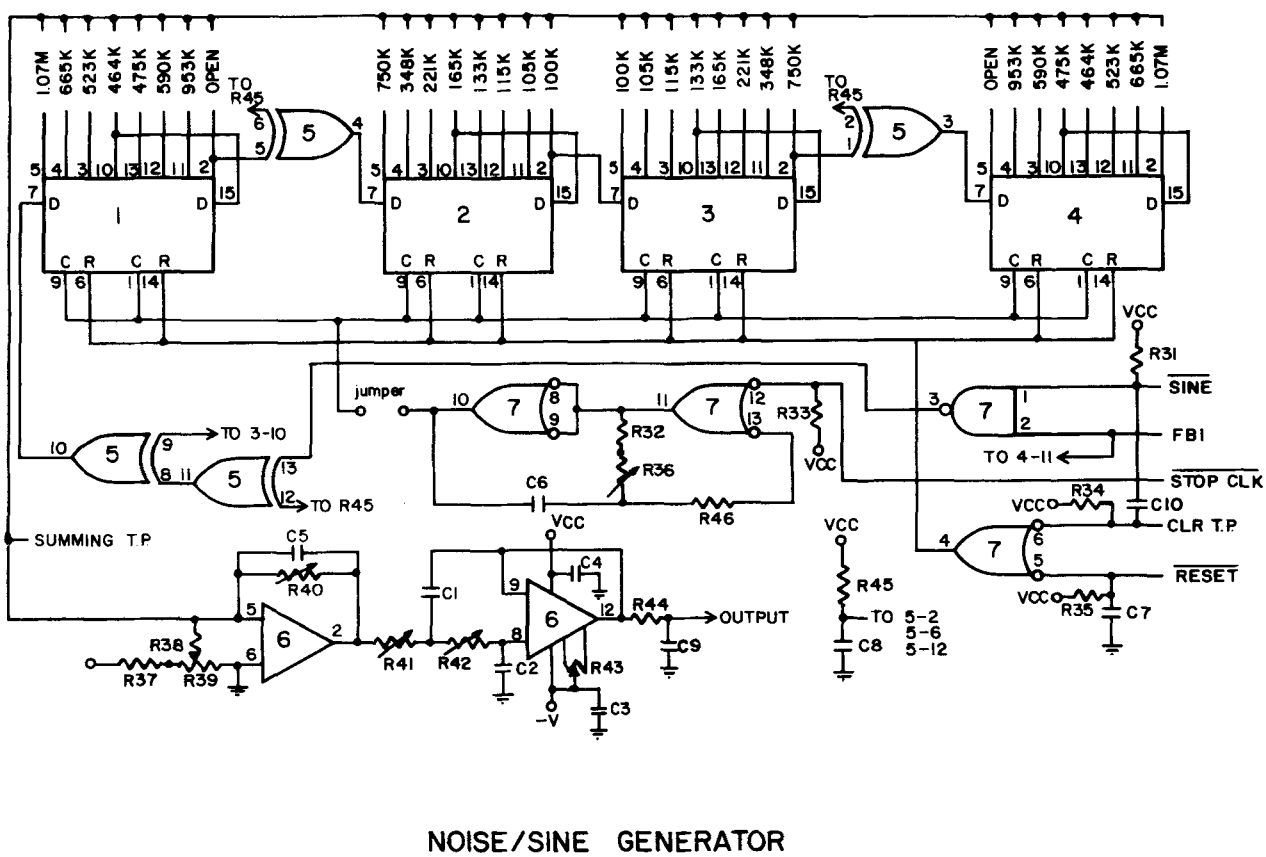

Figure 1. Schematic diagram of the digital noise/sine generator. The specific components are listed in Table 1.

Table 1
Parts List for Noise/Sine Generator

Resistors ¼ W, 1% Tolerance		Resistors ¼ W, 5% or 10% Tolerance	
1,30	1.07m	R31,33,34,35	100k
R2,29	665k	R32,38,45	10k
R3,28	523k	R37	1k
R4,27	464k	R44	470 Ω
R5,26	475k	R46	20k
R6,25	590k	Potentiometers ¼ W, 10 Turn	
R7,24	953k	R36,40	50k
R8,23	750k	R39,41,42,43	10k
R9,22	348k	Capacitors	
R10,21	221k	C1	.001 mFd, mylar
R11,20	165k	C2	.00047 mFd, mylar
R12,19	133k	C3,4,7,8,9,10	.01 mFd, disc
R13,18	115k	C5,6	100 pF, silver mica
R14,17	105k	Integrated Circuits	
R15,16	100k	IC1,2,3,4	MC14015*
		IC5	MC14507/4030*
		IC6	MC1458
		IC7	MC14011*

**or equivalent*

that the logic level will change state on any given clock pulse approaches .5. The power spectrum of the PRBS noise is a series of lines, spaced at intervals of the lower cut-off frequency and shaped by a $(\sin x/x)^2$ function. The −3-dB noise bandwidth is specified by:

$$1/(2^n - 1)\Delta t \leqslant F(\text{Hz}) \leqslant 1/2.25\Delta t,$$

where n is the maximum number of stages included in the feedback loop and Δt is the clock period.

The PRBS is a finite length sequence. The waveform, therefore, will repeat after a well-defined time interval, $(2^n - 1)\Delta t$. The "simplest case" maximal length sequence, for the circuit of Figure 1, occurs when shift register bits 3 and 31 are used in the feedback loop. With this feedback arrangement, and a clock frequency of 200 kHz ($\Delta t = 5 \times 10^{-6}$), the bandwidth of the unfiltered noise extends from .00009 Hz to 88.9 kHz, and the waveform will repeat every 2.98 h. Reducing the clock frequency shifts the bandwidth downward, reduces the spacing between spectral lines, and lengthens the time between repeating waveforms.

The circuit of Figure 1 uses bit 20 and bit 31 in the feedback loop for reasons to be explained later. This results in a less than maximal length sequence but does not significantly alter the bandwidth or statistical properties of the noise.

CONVERTING THE PRBS TO GAUSSIAN NOISE

The more familiar multilevel, or Gaussian, noise is generated when the PRBS is passed through a low-pass filter (Feth, 1970; Korn, 1966). In Figure 1, this filtering is done digitally by a resistive weighting network adapted from Anderson, Finnie, and Roberts (1967). This method applies the bit pattern represented by all 32 bits of the shift register to the resistive network. The values of these resistors are selected to approximate the inverse of a sin x/x function (re: 100 kΩ). Current from this network, along with an offset voltage, are added together at the inverting input of an operational amplifier, and appear at the output as a multilevel, biphasic noise voltage. The probability density function of this voltage is a good approximation to a bell-shaped Gaussian distribution.

The bandwidth of the low-pass filtered noise is nominally 1/20 of the clock frequency and, therefore, can be easily adjusted. The averaged rms output voltage from the digitally filtered noise will remain constant as the bandwidth changes because the spectrum level or power spectral density (V^2/Hz) of the underlying PRBS noise varies in inverse proportion to the clock frequency.

As with all digitally synthesized waveforms, the noise voltage is composed of many discrete steps. These steps result in unwanted "alias frequencies" around multiples of the clock frequency. The lowest alias of this digitally filtered PRBS (noise) occurs at 19/20 of the clock frequency and is −26 dB (re: V^2/Hz). This aliased signal can be reduced further without influencing the desired spectrum by analog filtering. Any low-pass cut-off frequency above 1/20 of the clock frequency can be used to reduce this aliased signal. A two-pole active low-pass filter is included in the circuit diagram of Figure 1. Amplitude spectra of PRBS and Gaussian noise for three different clock frequencies are shown in Figures 2, 3, and 4.

GENERATING SINE WAVES

The effect of the digital low-pass filter is most evident when a fixed pattern, containing an equal number of

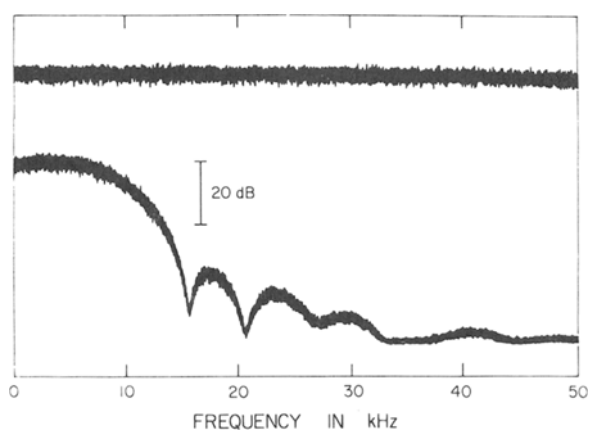

Figure 2. Amplitude spectrum plots of a PRBS and low-pass Gaussian noise generated by the circuit of Figure 1. The shift-register clock frequency was 200 kHz. The analog filter cut-off frequency was set at the digital low-pass filter cut-off, in this case, 10 kHz.

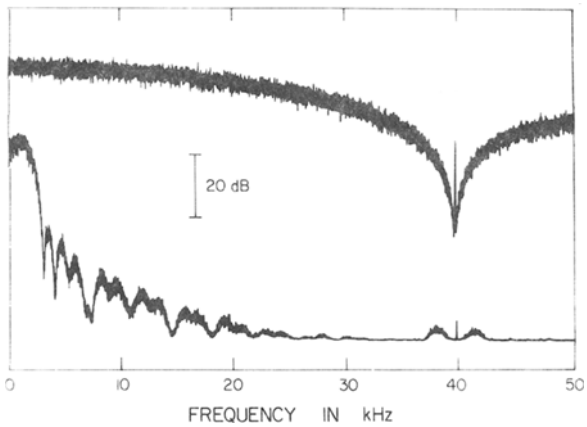

Figure 3. Amplitude spectrum plots of PRBS and low-pass filtered noise with a clock frequency of 40 kHz. The digital filter cut-off is now 2 kHz, and the analog filter was set at 10 kHz.

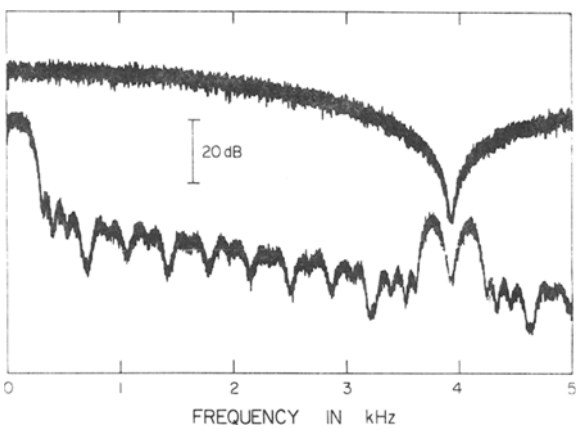

Figure 4. Amplitude spectrum plots of PRBS and low-pass filtered noise with the clock frequency adjusted to 4,000 Hz. The alias frequency components are much larger in this figure because they fall within the 10-kHz passband of the analog filter. The digital low-pass cut-off frequency was 200 Hz.

contiguous bits on and off, is propagated through the shift register; that is, when the output taken from a particular bit (bit 31, for example) is no longer a noisy rectangular-pulse train, but rather a 50% duty cycle square wave. The output of the generator now becomes a sine wave whose harmonic content is primarily determined by the length of the pattern passing through the shift register. In this case, the function of the weighting network is to remove harmonics from the "square-wave sequence."

An optimum sine wave (i.e., one having maximum amplitude and lowest total harmonic distortion) is generated when the frequency of the square-wave pattern is one-half the cut-off frequency of the filter, that is, 1/40 of the shift-register clock frequency.

A convenient means of switching the output of the generator from a low-pass filtered noise to a sine wave is included in the circuit of Figure 1. When the point labeled SINE is open, bits 20 and 31 are routed through an "exclusive-or" gate to the register data input and a Gaussian noise is generated. When SINE is grounded, only one bit, bit 20 inverted, is included in the feedback loop. With this arrangement, a sine wave is synthesized from 40 discrete amplitude levels, with typically less than 1% total harmonic distortion, disregarding aliases. This fixed number of points in the sine wave sets the lowest alias frequency at the 39th harmonic, more than five octaves above the fundamental.

MODIFICATIONS TO THE BASIC CIRCUIT

The circuit of Figure 1 can be modified easily to provide several functions beyond fixed-bandwidth low-pass noise and fixed frequency sine waves. For example, if the shift register is clocked from a crystal oscillator and digital divider, the noise bandwidth and sine-wave frequency can be set precisely from a remote source such as a computer. Care must be taken to insure that the alias frequencies do not occur in the output signal when the clock input is varied over a wide range. For the digitally filtered, low-pass noise, the aliased signal always will be at 19/20ths of the clock frequency and will be -26 dB (re: V^2/Hz); for the sine wave, the aliased signal always will be at 39/40ths of the clock frequency and will be -40 dB (re: V^2/Hz). They can be reduced further by changing the cut-off frequency of the analog filter in coarse steps as the clock frequency is changed.

Two or more generators can be phase locked by driving them from the same clock source. If one bit in the shift register of a reference sine-wave generator is gated with the clock source, the phase lock of one or more slave generators can be varied in 9-deg steps.

The output of one of these circuits, used as a variable low-pass noise source, can be multiplied by the output of another, used as a sine-wave generator, to produce narrow bands of noise at the sine-wave center frequency. The output from two of these narrow-band noise generators, with their sine-wave generators driven from the same clock and locked in quadrature phase, can be added together to simulate narrow-band noise produced by analog filtering (i.e., random phase and nonperiodic zero crossings).

In all cases, the noise or sine waves are repeatable from a fixed reset pattern. The circuit of Figure 1 was designed as a minimum configuration requiring only seven integrated circuits (ICs); therefore, the only initial pattern available is "all zeros." Other repeatable patterns can be generated by gating the generator output after a delay interval synchronized to the generator clock. Repeatable sequences can be generated from 65535 initial patterns, if the two 8-bit shift-register sections (IC-2 and IC-3) are replaced with four 4-bit shift registers that can be preset.

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