A Digital PLL with a Stochastic Time-to-Digital Converter

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Abstract

A new dual-loop digital PLL (DPLL) architecture is presented. It employs a stochastic time-to-digital converter (STDC) and a high frequency delta-sigma dithering to achieve a wide PLL bandwidth and low jitter at the same time. The test chip has been fabricated in a 0.13μm CMOS process. The DPLL features a 0.7-1.7 GHz oscillator tuning range, 6.9ps rms jitter and consumes 17mW while operating at 1.2GHz.

Introduction

A digital implementation of PLLs has several advantages in comparison to their analog counterparts: easy scalability with process shrink, eliminating the noise susceptible analog control for a voltage controlled oscillator (VCO) and the inherent noise immunity of digital circuits. Recently, several digital PLLs (DPLLs) have been reported [1, 2], which demonstrate the ability of a digital implementation to achieve the performance of analog PLLs. There are two types of phase/frequency detectors commonly used in a DPLL design. In the first approach, the phase detector is a time-to-digital converter (TDC) based on a chain of inverters [2]. The resolution of such a TDC is limited to a single inverter delay and is thus suitable only for low-bandwith DPLL designs. The second approach utilizes a binary (or bang-bang) phase/frequency detector, which results in an input signal dependent PLL bandwidth. In this paper, we present a new digital PLL architecture with a stochastic TDC, which overcomes this bandwidth limitation in DPLL designs.

Proposed Architecture

A block diagram of the proposed DPLL architecture is shown in Fig. 1. It consists of two loops: fine and coarse. On power up only the coarse loop is active. In the coarse loop the bang-bang PFD (!!PFD) senses only the sign of the phase and the frequency difference between the reference signal F_{REF} and the divided oscillator clock F_{CKV}. This information is filtered by the 12-bit digital loop filter (DLF1), truncated and passed to the 8-bit DAC. The DAC converts a digital word into a current value which controls the digitally-controlled analog oscillator (DCAO). The DCAO has two control inputs for the coarse and fine loops. The lock detector (LD) monitors the output of the bang-bang PFD and decides whether the coarse loop is in lock. If so, the LD freezes the coarse loop and activates the fine loop. The stochastic TDC (STDC) works as a phase detector (PD) in the fine loop. It measures the time difference between the rising edges of the reference signal F_{REF} and the divided oscillator clock F_{CKV}. The measured time difference has the phase information embedded in it. The 6-bit digital output of the STDC is filtered by a 14-bit digital loop filter (DLF2) and then given to the digital $\Delta\Sigma$ modulator (DSM). Since the resolution of the DCAO is limited, it cannot accommodate a high resolution signal from the loop filter. The purpose of the DSM is to re-quantize a low frequency high resolution digital signal into a high frequency low resolution one. In spite of the loss in resolution for a particular sample of the signal, the average resolution of the signal remains unchanged. The DSM is clocked at a frequency of $F_{DCAO}/4$. Both loop filters are proportional-integral controllers with 1/128 ratio between the integral and proportional paths.

Circuit Design

Fig. 2 demonstrates a simplified block diagram of the STDC. It consists of a set of latches called arbiters (ARBs) and an encoder. The STDC is based on the stochastic properties of a set of arbiters [3]. Each arbiter from the set, given the same input signals, F_{REF} and F_{CKV}, will react differently because they exhibit finite random mismatches resulting from process variations. Some of the arbiters output would yield 1's, and some of them 0's, even if the two input edges were lined up equally. Based on the number of ones and zeros, the time difference between the rising edges of signals is digitized. The digitized value is sufficiently linear due to the inherent statistical distribution of process variations. The improved linearity of the fine loop PD due to the STDC results in a DPLL bandwidth that is independent of input jitter amplitude. The digitally-controlled analog oscillator is a five-stage ring oscillator as shown in Fig. 3 with Lee-Kim delay cells. To achieve a low DCAO gain, needed for the digital PLL, only one of the five stages is controlled by the PLL. An additional NMOS latch is added to the controlled stage to futher reduce the DCAO gain. The rest of the stages are controlled from outside the chip (V_{EXT}) for testing purposes only. A frequency locked loop should be implemented to achieve a PLL locking range over the full oscillator tuning range. The most critical specification for the DAC is monotonicity, thus a thermometer architecture has been implemented. The DAC consists of 256 differential current sources and column and row decoders. The outputs of all current sources are summed and mirrored through a PMOS diode connected device to generate the coarse control voltage V_C for the controlled oscillator stage. The implemented DSM is a second order error-feedback structure with a three-level output. The output of the DSM controls two current sources similar to those in the DAC. The resulting current is steered through a PMOS diode connected device and the fine control voltage V_F is generated. The fine loop has 3 times more frequency range than the LSB of the coarse loop.

Experimental Results

The test chip has been fabricated using a 0.13μm CMOS process and occupies 0.6mm^2 of area. The output power spectral density (PSD) of the fine and coarse loops in lock at 1.2GHz is shown in Fig. 4. The right curve represents the fine loop PSD, and the left curve represents the coarse loop PSD shifted to the left in frequency for display purposes only. The coarse loop PSD has spurs at about 3MHz offset from the carrier which comes from the limit cycle behavior of the bang-bang PLL. The bandwith of the DPLL with the fine loop is about 4MHz. The jitter measured in the coarse and fine loops is shown in Figs. 5 and 6, respectively. The coarse loop has

23.6ps of rms jitter and the fine loop has 6.9ps of rms jitter. The chip micrograph is shown in Fig. 7.

Conclusions

A novel digital PLL with a stochastic TDC is presented. It allows for a low jitter DPLL design with a wide bandwidth that is independent of the input jitter amplitude.

Acknowledgements

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References

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[3] V. Gutnik and A. Chandrakasan, "On-chip picosecond time measurement," in *IEEE Symposium on VLSI Circuits. Dig. Tech. Papers*, Jun. 2000, pp. 52–53.

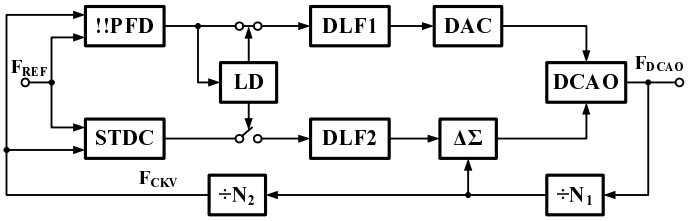

Figure 1: Block diagram of the proposed DPLL.

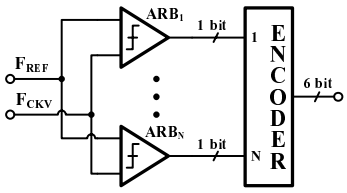

Figure 2: Fine time-to-digital converter.

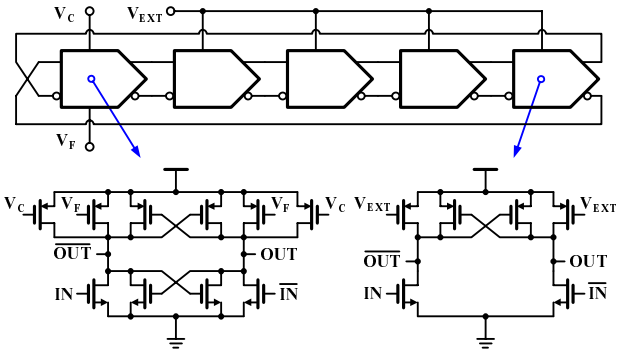

Figure 3: Digitally controlled analog oscillator.

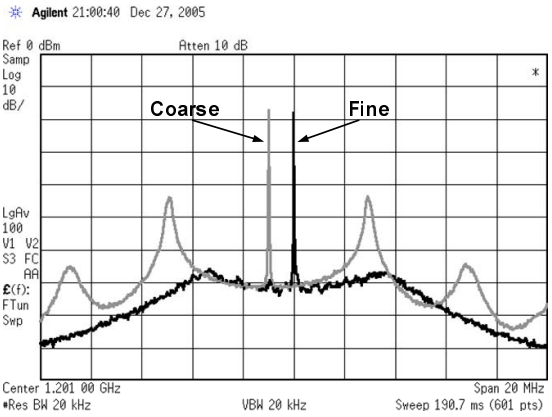

Figure 4: DPLL spectra.

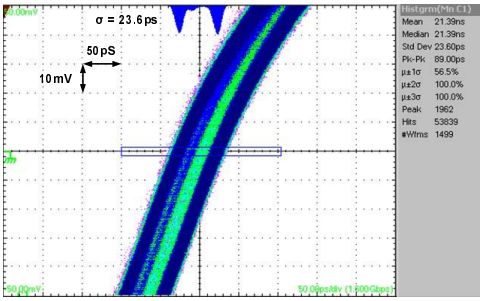

Figure 5: DPLL jitter with the coarse loop only.

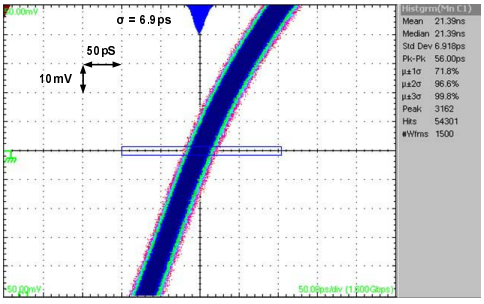

Figure 6: DPLL jitter with the fine loop.

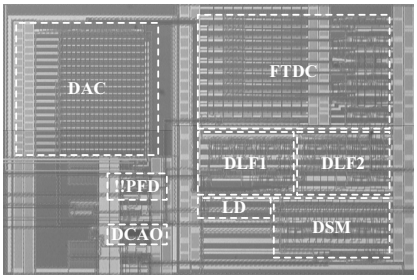

Figure 7: Chip micrograph.